



DI2CS

I²C Bus Interface - Slave

ver 3.02

OVERVIEW

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data transmission over a short distance between many devices. The DI2CS core provides an interface between a microprocessor /microcontroller and an I²C bus. It can work as a slave transmitter or slave receiver depending on working mode determined by a master device. The DI2CS core incorporates all features required by the latest I²C specification including clock synchronization, arbitration and High-speed transmission mode. The DI2CS supports all the transmission speed modes.

KEY FEATURES

- Conforms to v.2.1 of the I²C specification
- Slave operation
 - *Slave transmitter*
 - *Slave receiver*
- Supports 3 transmission speed modes
 - *Standard (up to 100 kb/s)*
 - *Fast (up to 400 kb/s)*
 - *High Speed (up to 3,4 Mb/s)*
- Allows operation from a wide range of input clock frequencies
- Simple interface allows easy connection to microprocessor/microcontroller devices
- Interrupt generation
- User-defined data setup time

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- Fully synthesizable
- Static synchronous design with positive edge clocking and synchronous reset
- No internal tri-states
- Scan test ready

APPLICATIONS

- Embedded microprocessor boards
- Consumer and professional audio/video
- Home and automotive radio
- Low-power applications
- Communication systems
- Cost-effective reliable automotive systems

DELIVERABLES

- ◆ Source code:
 - ◇ VHDL Source Code or/and
 - ◇ VERILOG Source Code or/and
 - ◇ Encrypted, or plain text EDIF netlist
- ◆ VHDL & VERILOG test bench environment
 - ◇ Active-HDL automatic simulation macros
 - ◇ ModelSim automatic simulation macros
 - ◇ Tests with reference responses
- ◆ Technical documentation
 - ◇ Installation notes
 - ◇ HDL core specification
 - ◇ Datasheet
- ◆ Synthesis scripts
- ◆ Example application
- ◆ Technical support

<http://www.DigitalCoreDesign.com>
<http://www.dcd.pl>

- ◇ IP Core implementation support
- ◇ 3 months maintenance
 - Delivery the IP Core updates, minor and major versions changes
 - Delivery the documentation updates
 - Phone & email support

LICENSING

Comprehensible and clearly defined licensing methods without royalty fees make using of IP Core easy and simply.

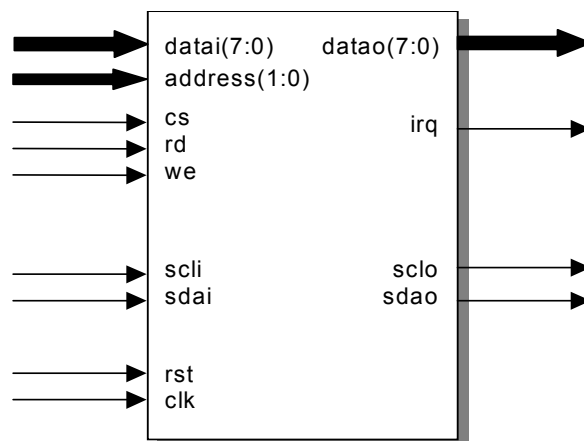
Single Design license allows use IP Core in single FPGA bitstream and ASIC implementation.

Unlimited Designs, One Year licenses allow use IP Core in unlimited number of FPGA bitstreams and ASIC implementations.

In all cases number of IP Core instantiations within a design, and number of manufactured chips are unlimited. There is no time restriction except One Year license where time of use is limited to 12 months.

- Single Design license for
 - VHDL, Verilog source code called HDL Source
 - Encrypted, or plain text EDIF called Netlist
- One Year license for
 - Encrypted Netlist only
- Unlimited Designs license for
 - HDL Source
 - Netlist
- Upgrade from
 - HDL Source to Netlist
 - Single Design to Unlimited Designs

SYMBOL

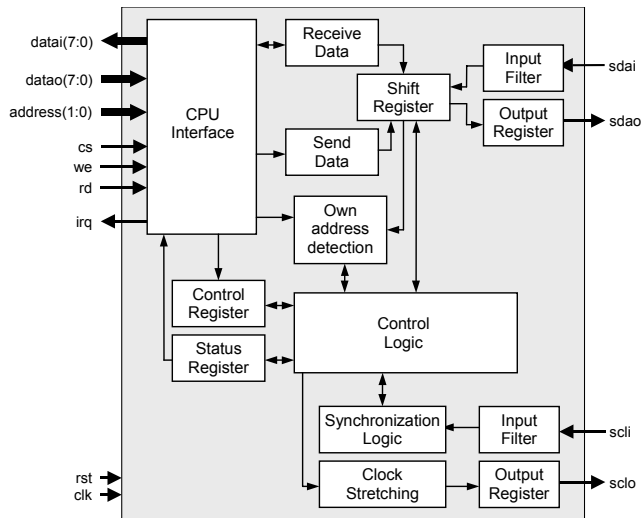


PINS DESCRIPTION

PIN	TYPE	DESCRIPTION
clk	input	Global clock
rst	input	Global reset
address(1:0)	input	Processor address lines
cs	input	Chip select
we	input	Processor write strobe
rd	input	Processor read strobe
scli	input	I ² C bus clock line (input)
sdai	input	I ² C bus data line (input)
datai(7:0)	input	Processor data bus (input)
datao(7:0)	output	Processor data bus (output)
sclo	output	I ² C bus clock line (output)
sdao	output	I ² C bus data line (output)
irq	output	Processor interrupt line

BLOCK DIAGRAM

Figure below shows the DI2CS IP Core block diagram.



CPU Interface – Performs the interface functions between DI2CS internal blocks and microprocessor. Allows easy connection of the core to a microprocessor/microcontroller system.

Control Logic – Manages execution of all commands sent via interface. Synchronizes internal data flow.

Shift Register – Controls SDA line, performs data and address shifts during the data transmission and reception.

Control Register – Contains five control bits used for performing all types of I²C Bus transmissions.

Status Register – Contains seven status bits that indicates state of the I²C Bus and the DI2CS core.

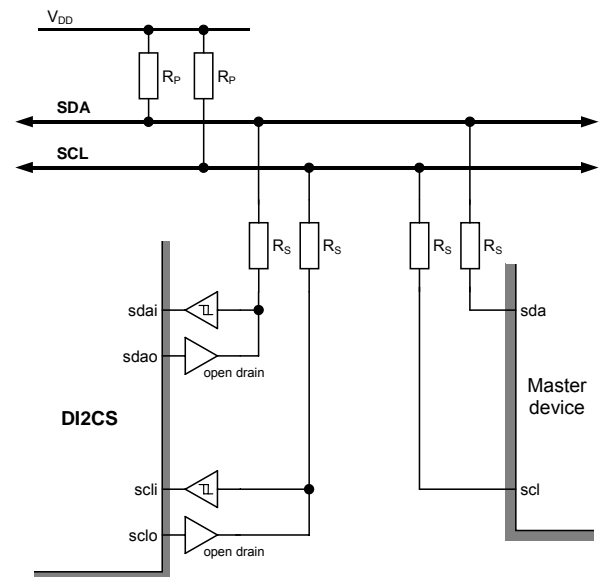
Input Filter – Performs spike filtering.

Synchronization Logic – Performs DI2CS core synchronization.

Clock Stretching – Performs I²C SCL clock stretching when DI2CS core is not ready for next transmission.

IMPLEMENTATION

Figure below show the typical DI2CS implementations in system with Standard/Fast and High-speed devices.



PERFORMANCE

The following table gives a survey about the Core area and performance in the ALTERA® devices after Place & Route (all key features have been included):

Device	Speed grade	Logic Cells	F _{max}
MERCURY	-5	170	250 MHz
STRATIX	-5	170	260 MHz
CYCLONE	-6	170	220 MHz
APEX II	-7	170	270 MHz
APEX20KC	-7	170	150 MHz
APEX20KE	-1	170	120 MHz
APEX20K	-1	170	90 MHz
ACEX1K	-1	170	107 MHz
FLEX10KE	-1	170	107 MHz
MAX 7000AE	-5	83	96 MHz
MAX 3000A	-5	83	104 MHz

Core performance in ALTERA® devices

The main features of each Digital Core Design I²C compliant cores have been summarized in table below. It gives a briefly member characterization helping user to select the most suitable IP Core for its application.

Design	I ² C specification version	Master operation	Slave operation	CPU interface	Passive device interface	Interrupt generation	Clock synchronization	Arbitration	7-bit addressing	10-bit addressing	Standard mode	Fast mode	High-speed mode	User defined timing	Spike filtering
DI2CM	3.0	✓	-	✓	-	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
DI2CS	2.1	-	✓	✓	-	✓	✓	-	✓	-	✓	✓	✓	✓	✓
DI2CSB	2.1	-	✓	-	✓	-	-	-	✓	-	✓	✓	✓	-	✓

I²C cores summary table

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