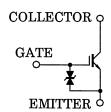
TOSHIBA INSULATED GATE BIPOLAR TRANSISTOR SILICON N CHANNEL IGBT

GT8G103

STROBE FLASH APPLICATIONS

- 3rd Generation
- Enhancement-Mode
- Low Saturation Voltage: $V_{CE (sat)} = 8 \text{ V (Max.)}$ (@IC = 150 A)
- 4.5 V Gate Drive



ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

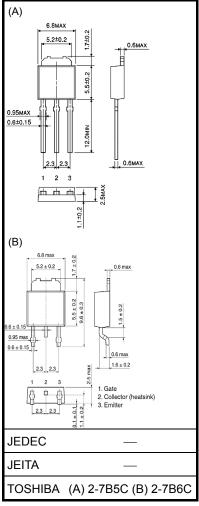
CHARACTERISTIC		SYMBOL	RATING	UNIT	
Collector-Emitter Voltage		V _{CES}	400	V	
Gate-Emitter Voltage	DC	V _{GES}	±6	V	
	Pulse	V _{GES}	±8	V	
Collector Current	DC	Ic	8	Α	
Collector Current	1 ms	I _{CP}	150	Α	
Collector Power Dissipation	Ta = 25°C	PC	1.3	W	
	Tc = 25°C	PC	20	W	
Junction Temperature		Tj	150	°C	
Storage Temperature Range		T _{stg}	-55~150	°C	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling

Precautions"/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Unit: mm

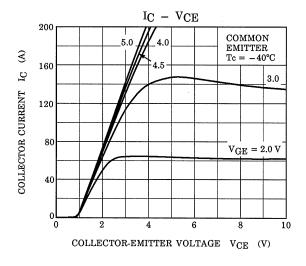


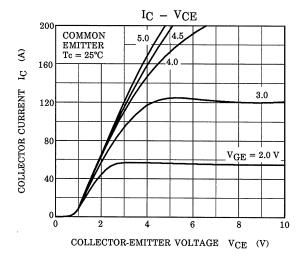
Weight: 0.36 g (typ.)

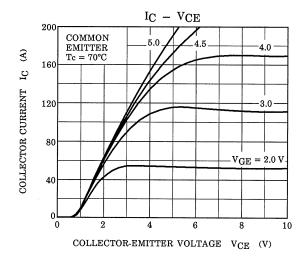
ELECTRICAL CHARACTERISTICS (Ta = 25°C)

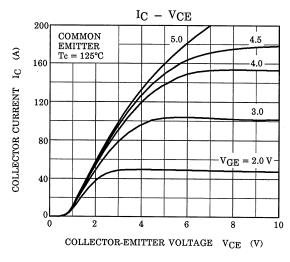
CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT
Gate Leakage Current		I _{GES}	V _{GE} = 6 V, V _{CE} = 0	_	_	10	μA
Collector Cut-off Current		I _{CES}	V _{CE} = 400 V, V _{GE} = 0	_	_	10	μA
Gate-Emitter Cut-off Voltage		V _{GE} (OFF)	I_C = 1 mA, V_{CE} = 5 V	0.5	_	1.2	V
Collector-Emitter Saturation Voltage		V _{CE (sat)}	I _C = 150 A, V _{GE} = 4.5 V (Pulsed)		5	8	V
Input Capacitance		C _{ies}	V _{CE} = 10 V, V _{GE} = 0, f = 1 MHz	-	1900	-	pF
Switching Time	Rise Time	t _r	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	-	1.2	_	μs
	Turn-on Time	ton		-	1.4	_	
	Fall Time	t _f		-	1.8	_	
	Turn-off Time	t _{off}		_	2.4	_	
Thermal Resistance		R _{th (j−c)}	_	_	_	6.25	°C/W

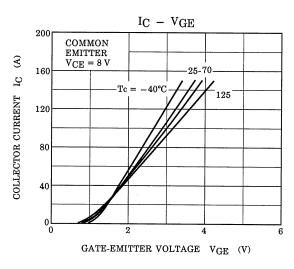
These devices are MOS type. Users should follow proper ESD Handling Procedures. Operating condition of turn-off dv / dt should be lower than 400 V / μs .

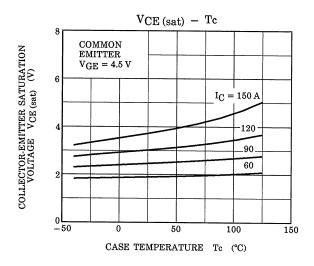


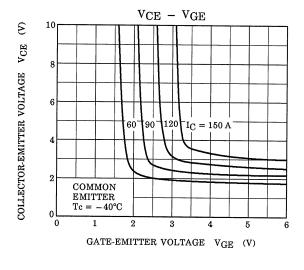


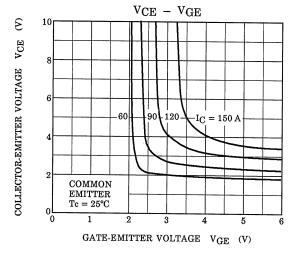


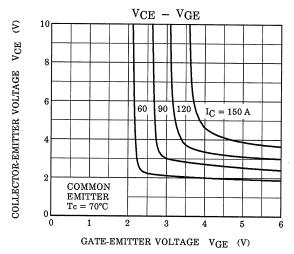


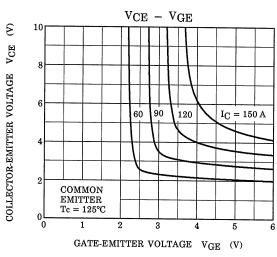


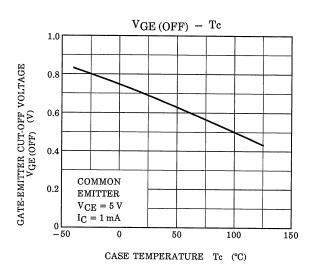


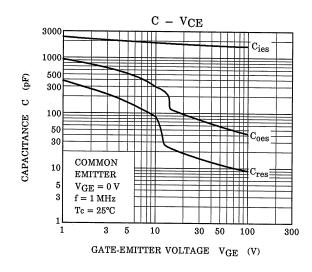




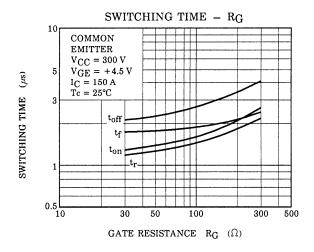


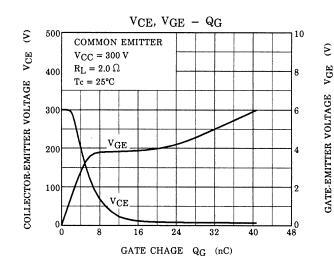


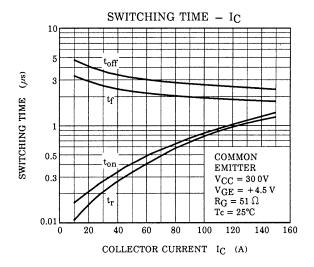


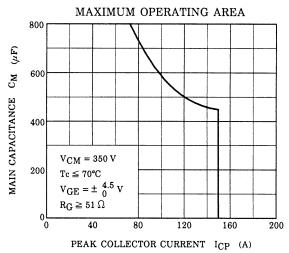


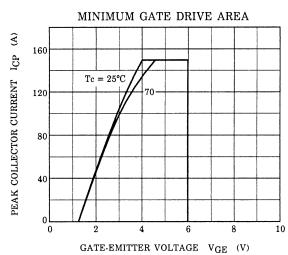
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