64-Channel Serial to Parallel Converter
with P-Channel Open Drain Controllable Output Current

Features

► HVCMOS® technology
► 5.0V CMOS Logic
► Output voltage up to -85V
► Output current source control
► 16MHz equivalent data rate
► Latched data outputs
► Foreward and reverse shifting options (DIR pin)
► Diode to VDD allows efficient power recovery

General Description

The HV570 is a low-voltage serial to high-voltage parallel converter with P-channel open drain outputs. This device has been designed for use as a driver for plasma panels.

The device has two parallel 32-bit shift registers, permitting data rates twice the speed of one (they are clocked together). There are also 64 latches and control logic to perform the blanking of the outputs. $HV_{OUT}1$ is connected to the first stage of the first shift register through the blanking logic. Data is shifted through the shift registers on the logic low to high transition of the clock. The DIR pin causes CCW shifting when connected to V_{SS}, and CW shifting when connected to V_{DD}. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register ($HV_{OUT}64$). Operation of the shift register is not affected by the $\overline{LE}$ (latch enable), or the $\overline{BL}$ (blanking) inputs. Transfer of data from the shift registers to latches occurs when the $\overline{LE}$ input is high. The data in the latches is stored when $\overline{LE}$ is low.

The HV570 has 64 channels of output constant current sourcing capability. They are adjustable from 0.1 to 2.0mA through one external resistor or a current source.

Functional Block Diagram
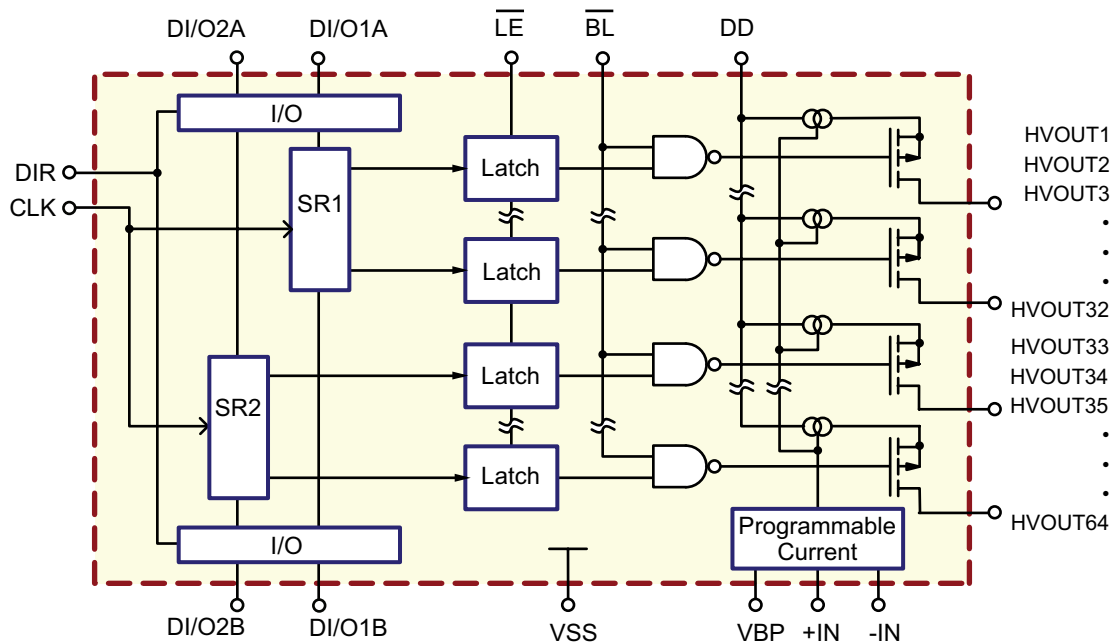
Note:
Each SR (shift register) provides 32 outputs. SR1 supplies outputs 1 to 32 and SR2 supplies outputs 33 to 64.

Ordering Information

Device	Package Options
	80-Lead PQFP
HV57009	HV57009PG-G

-G indicates package is RoHS compliant ('Green')

Absolute Maximum Ratings

Parameter	Value
Supply voltage, V_{DD}[1]	-0.5V to +7.5V
Output voltage , V_{PP}[1]	V_{DD} + 0.5V to -95V
Logic input levels[1]	-0.3V to V_{DD} + 0.3V
Ground current[2]	1.5A
Continuous total power dissipation[3]	1200mW
Operating temperature range	-40°C to +85°C
Storage temperature range	-65°C to +150°C
Lead temperature 1.6mm from case for 10 seconds	260°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability.
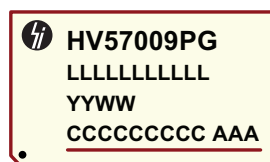
Notes:
1. All voltages are referenced to V_{SS}
2. Limited by the total dissipated in the package.
3. For operation above 25°C ambiant derate linearly to maximum operating temperature at 20mW/°C.

Pin Configuration

80-Lead PQFP (PG)
(top view)

Product Marking

HV57009PG
LLLLLLLLLLL
YYWW
CCCCCCCCC AAA
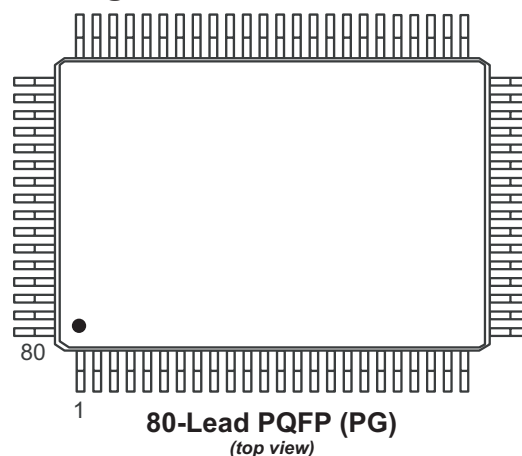
L = Lot Number
YY = Year Sealed
WW = Week Sealed
C = Country of Origin
A = Assembler ID
___ = "Green" Packaging

80-Lead PQFP (PG)

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{DD}	Logic supply voltage	4.5	5.5	V
HV_{OUT}	HV output off voltage	-85	V_{DD}	V
V_{IH}	High-level input voltage	V_{DD} - 1.2V	-	V
V_{IL}	Low-level input voltage	0	1.2	V
f_{CLK}	Clock frequency per register	DC	8.0	MHz
			4.5	
T_A	Operating free-air temperature	-40	+85	°C

Notes:
Power-up sequence should be the following:
1. Apply ground
2. Apply V_{DD}
3. Set all inputs (D_{IN}, CLK, $\overline{LE}$) to a known state

Power-down sequence should be the reverse of the above

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DC Electrical Characteristics *(All voltages are referenced to V_{SS}, $V_{SS} = 0$, $T_A = 25^OC$)*

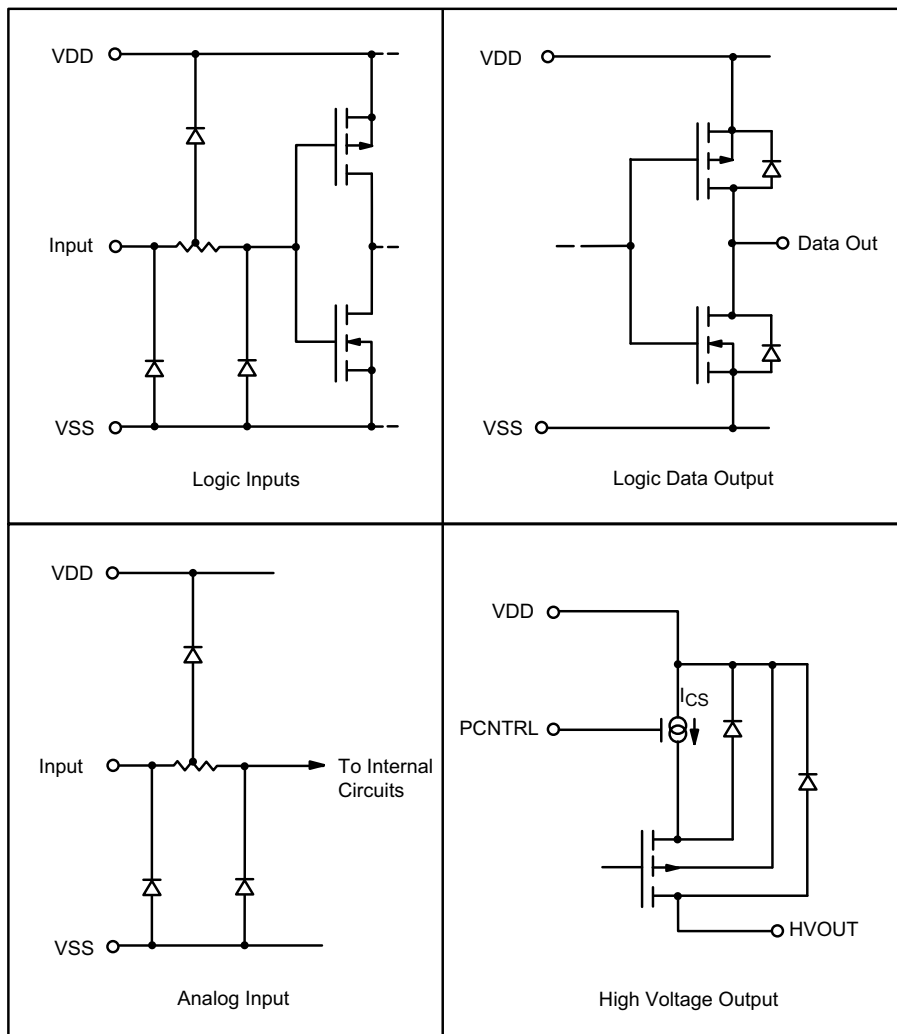| Symbol	Parameter		Min	Max	Units	Conditions
I_{DD}	V_{DD} supply current		-	15	mA	$V_{DD} = V_{DD}$ max, $f_{CLK} = 8.0$MHz
I_{NN}	High voltage supply current		-	-10	µA	Outputs off, $HV_{OUT} = -85$V (total of all outputs)
I_{DDQ}	Quiescent V_{DD} supply current		-	100	µA	All inputs = V_{DD}, except +IN = V_{SS} = GND
V_{OH}	High level output	Data Out	$V_{DD} - 0.5$V	-	V	$I_O = -100$µA
		HV_{OUT}	+1.0	V_{DD}	V	$I_O = -2.0$mA
V_{OL}	Low level output	Data Out	-	+0.5	V	$I_O = 100$µA
I_{IH}	High-level logic input current		-	1.0	µA	$V_{IH} = V_{DD}$
I_{IL}	Low-level logic input current		-	-1.0	µA	$V_{IL} = 0$V
I_{CS}	High output source current		-	-2.0	mA	$V_{REF} = 2.0$V, $R_{EXT} = 1$K, see Figures 1a and 1b
			-0.1	-	mA	$V_{REF} = 0.1$V, $R_{EXT} = 1$K, see Figures 1a and 1b
ΔI_{CS}	HV output source current for $I_{REF} = 2.0$mA		-	10	%	$V_{REF} = 2.0$V, $R_{EXT} = 1$K

Note:
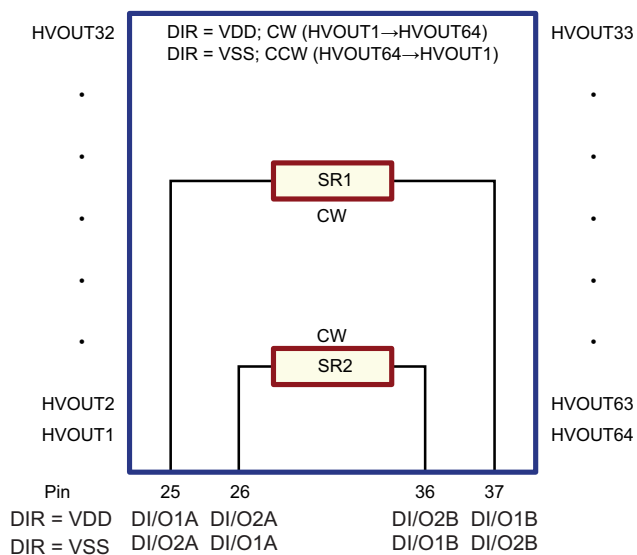*Current going out of the chip is considered negative.*

AC Electrical Characteristics *(Logic signal inputs and data inputs have t_r, $t_f \leq 5$ns [10% and 90% points] for measurements)*

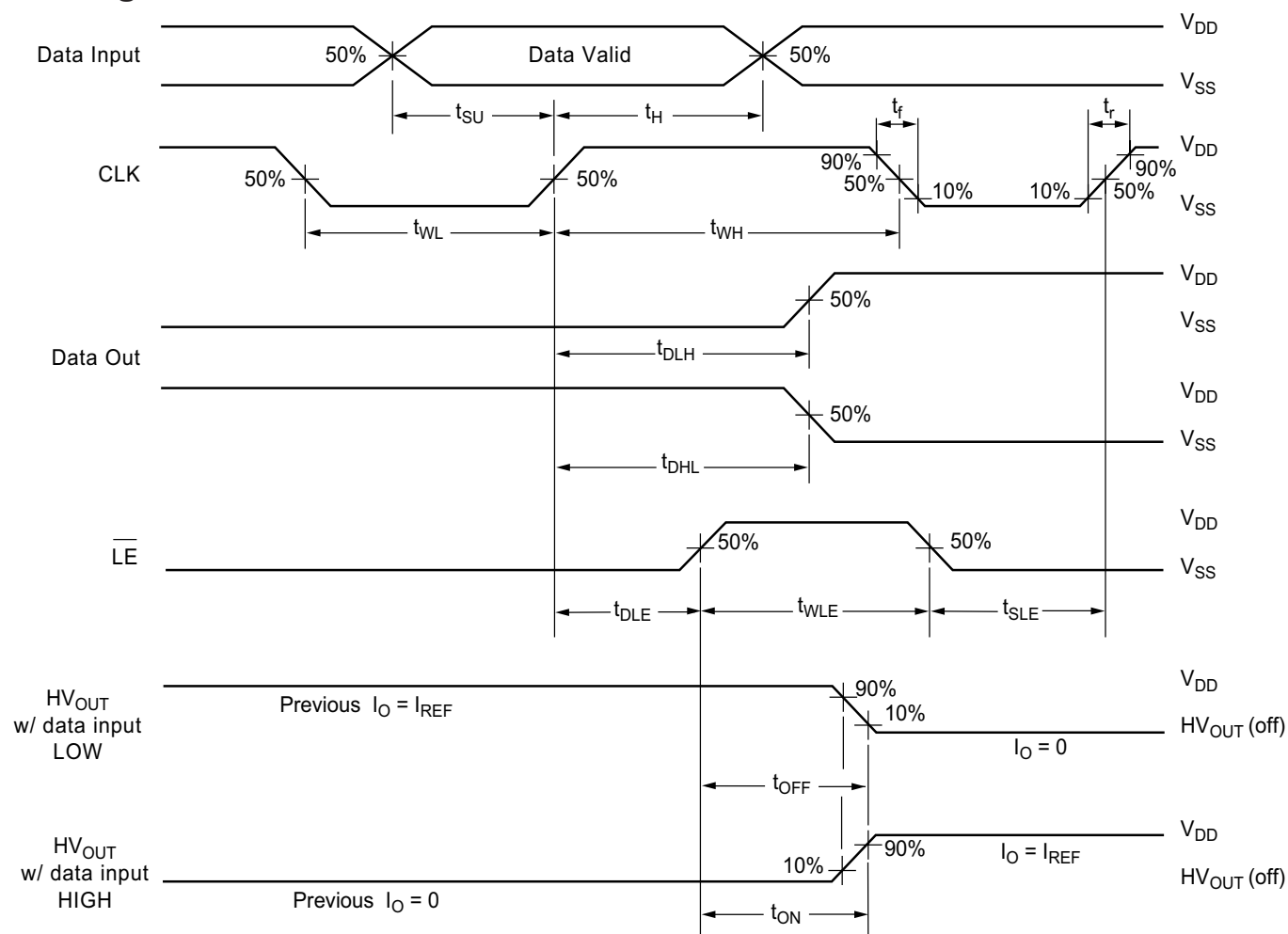| Symbol	Parameter	Min	Max	Units	Conditions
f_{CLK}	Clock frequency	DC	8.0	MHz	Per register
			4.5		When cascading devices
t_{WL}, t_{WH}	Clock width high or low	62	-	ns	---
t_{SU}	Data set-up time before clock rises	20	-	ns	---
t_H	Data hold time after clock rises	15	-	ns	---
t_{ON}, t_{OFF}	Time from latch enable to HV_{OUT}	-	500	ns	$C_L = 15$pF
t_{DHL}	Delay time clock to data high to low	-	150	ns	$C_L = 15$pF
t_{DLH}	Delay time clock to data low to high	-	150	ns	$C_L = 15$pF
t_{DLE}	Delay time clock to $\overline{LE}$ low to high	45	-	ns	---
t_{WLE}	$\overline{LE}$ pulse width	25	-	ns	---
t_{SLE}	$\overline{LE}$ set-up time before clock rises	0	-	ns	---
t_r, t_f	Max. allowable clock rise and fall time (10% and 90% points)	-	100	ns	---

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Input and Output Equivalent Circuits

Logic Inputs

Logic Data Output

Analog Input

High Voltage Output

Shift Register Operation

Pin	25	26	36	37
DIR = VDD	DI/O1A	DI/O2A	DI/O2B	DI/O1B
DIR = VSS	DI/O2A	DI/O1A	DI/O1B	DI/O2B

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Switching Waveforms

Function Table

Function	Inputs					Outputs		
	Data In	CLK	$\overline{LE}$	$\overline{BL}$	$\overline{DIR}$	Shift Reg	HV Outputs	Data Out
All O/P high	X	X	X	L	X	*	ON	*
Data falls through (latches transparent)	L	_↑‾	H	H	X	L.....L	ON	L
	H	_↑‾	H	H	X	H.....H	OFF	H
Data stored in latches	X	X	L	H	X	*	Inversion of stored data	*
I/O relation	DI/O1-2A	_↑‾	H	H	H	$Q_n{\rightarrow}Q_{n+1}$	New ON or OFF	DI/O1-2B
	DI/O1-2A	_↑‾	L	H	H	$Q_n{\rightarrow}Q_{n+1}$	Previous ON or OFF	DI/O1-2B
	DI/O1-2B	_↑‾	L	H	L	$Q_n{\rightarrow}Q_{n-1}$	Previous ON or OFF	DI/O1-2A
	DI/O1-2B	_↑‾	H	H	L	$Q_n{\rightarrow}Q_{n-1}$	New ON or OFF	DI/O1-2A

Note:
* = dependent on previous stage's state. See Figure 7 for DIN and DOUT pin designation for CW and CCW shift.
$H = V_{DD}$ (Logic)/V_{NN} (HV Outputs)
$L = V_{SS}$

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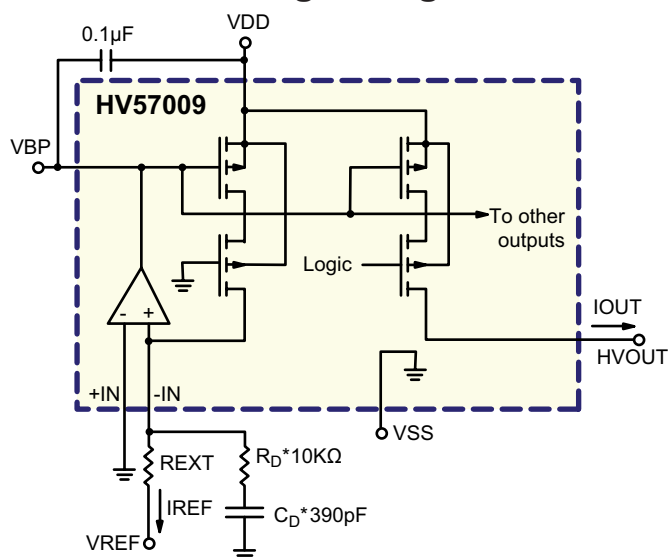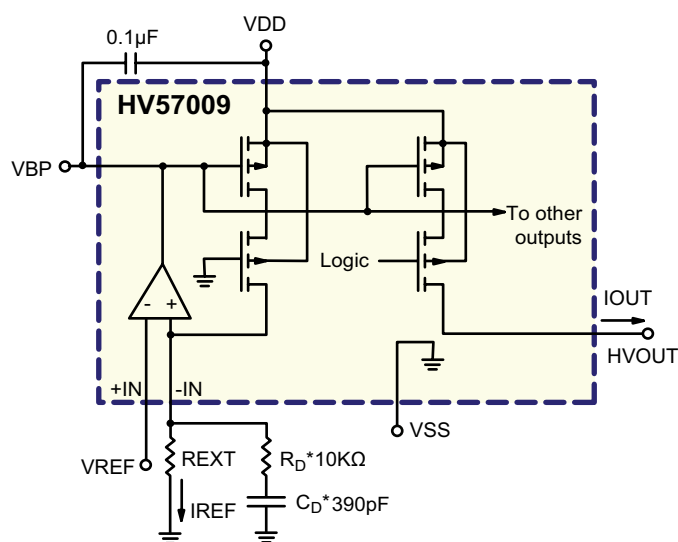## Typical Current Programing Circuits

Figure 1a: Negative Control

Figure 1b: Positive Control

*Required if $R_{EXT} > 10K\Omega$ or R_{EXT} is replaced by a constant current source.

Since $I_{OUT} = I_{REF} = \dfrac{|V_{REF}|}{R_{EXT}}$

Therefore:

If $I_{OUT} = 2.0mA$ and $V_{REF} = -5.0V \rightarrow R_{EXT} = 2.5K\Omega$.
If $I_{OUT} = 1.0mA$ and $R_{EXT} = 1.0K\Omega \rightarrow V_{REF} = -1.0V$.

If $R_{EXT} > 10K\Omega$, add series network R_D and C_D to ground for stability as shown.

This control method behaves linearly as long as the operational amplifier is not saturated. However, it requires a negative power source and needs to provide a current $I_{REF} = I_{OUT}$ for each HV570 chip being controlled.

If $HV_{OUT} \geq +1.0V$, the HV_{OUT} cascode may no longer operate as a perfect current source, and the output current will diminish. This effect depends on the magnitude of the output current.
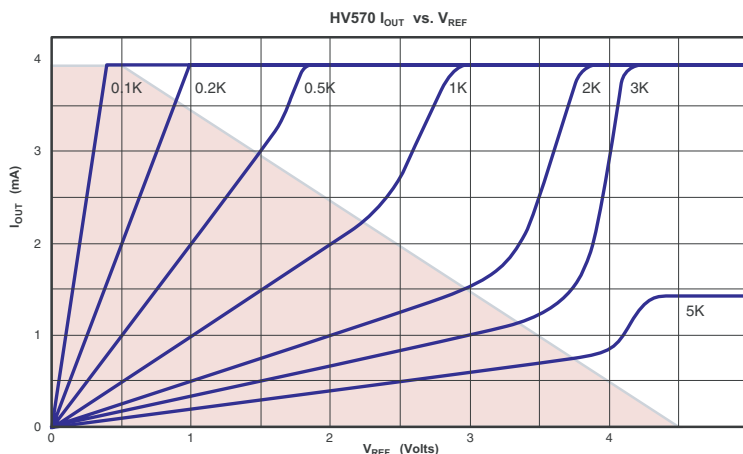
Given I_{OUT} and V_{REF}, the R_{EXT} can be calculated by using:

$$R_{EXT} = \frac{V_{REF}}{I_{REF}} = \frac{V_{REF}}{I_{OUT}}$$

The intersection of a set of I_{OUT} and V_{REF} values can be located in the graph shown below. The value picked for R_{EXT} must always be in the shaded area for linear operation. This control method has the advantage that V_{REF} is positive, and draws only leakage current. If $R_{EXT} > 10K\Omega$, add series network R_D and C_D to ground for stability as shown.

Note:
Lower reference current I_{REF} results in higher distortion, ΔI_{CS}, on the output.

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Pin Function

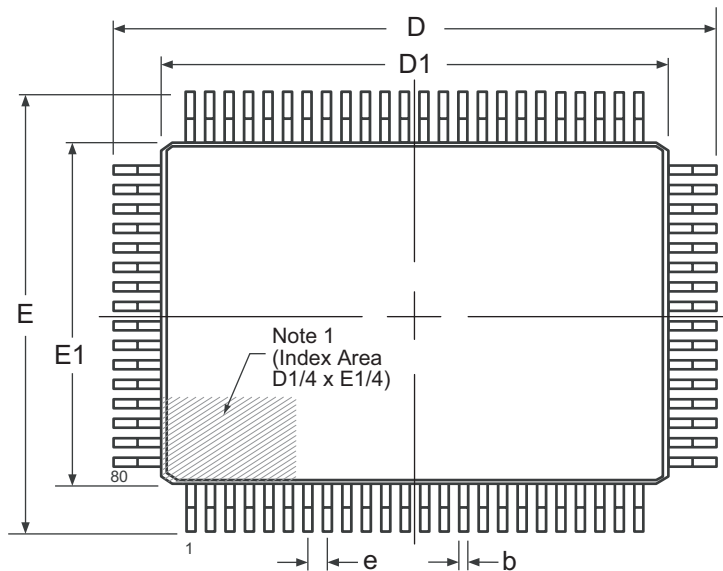| Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	HVOUT24	21	HVOUT4	41	HVOUT64	61	HVOUT44
2	HVOUT23	22	HVOUT3	42	HVOUT63	62	HVOUT43
3	HVOUT22	23	HVOUT2	43	HVOUT62	63	HVOUT42
4	HVOUT21	24	HVOUT1	44	HVOUT61	64	HVOUT41
5	HVOUT20	25	DIO/1A	45	HVOUT60	65	HVOUT40
6	HVOUT29	26	DI/O2A	46	HVOUT59	66	HVOUT39
7	HVOUT18	27	NC	47	HVOUT58	67	HVOUT38
8	HVOUT17	28	NC	48	HVOUT57	68	HVOUT37
9	HVOUT16	29	$\overline{LE}$	49	HVOUT56	69	HVOUT36
10	HVOUT15	30	CLK	50	HVOUT55	70	HVOUT35
11	HVOUT14	31	$\overline{BL}$	51	HVOUT54	71	HVOUT34
12	HVOUT13	32	VSS	52	HVOUT53	72	HVOUT33
13	HVOUT12	33	DIR	53	HVOUT52	73	HVOUT32
14	HVOUT11	34	VDD	54	HVOUT51	74	HVOUT31
15	HVOUT10	35	-IN	55	HVOUT50	75	HVOUT30
16	HVOUT9	36	DI/O2B	56	HVOUT49	76	HVOUT29
17	HVOUT8	37	DI/O1B	57	HVOUT48	77	HVOUT28
18	HVOUT7	37	NC	58	HVOUT47	78	HVOUT27
19	HVOUT6	39	+IN	59	HVOUT46	79	HVOUT26
20	HVOUT5	40	VBP	60	HVOUT45	80	HVOUT25

Note:
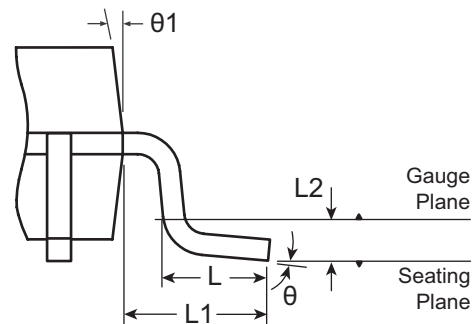*Pin designation for DIR = V_{DD}.*
A 0.1µF capacitor is needed between V_{DD} and V_{BP} (pin 40) for better output current stability and to prevent transient cross-coupling between outputs.
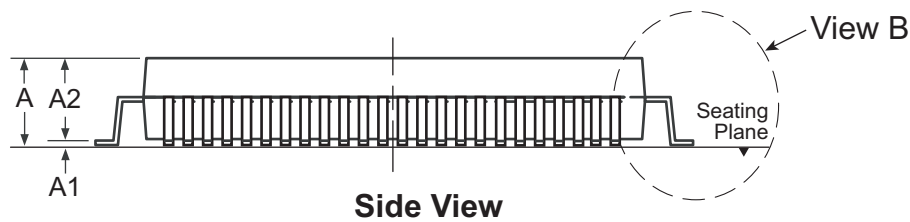*See Fig. 1a and 1b.*

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80-Lead PQFP Package Outline (PG)
20x14mm body, 0.80mm pitch

Top View

Side View

View B

Note 1:
   A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier may be either a mold, or an embedded metal or marked feature.

Symbol		A	A1	A2	b	D	D1	E	E1	e	L	L1	L2	θ	θ1
Dimension (mm)	MIN	2.80	0.25	2.55	0.30	23.65	19.80	17.65	13.80	0.80 BSC	0.73	1.95 REF	0.25 BSC	0°	5°
	NOM	-	-	2.80	-	23.90	20.00	17.90	14.00		0.88			3.5°	-
	MAX	3.40	-	3.05	0.45	24.15	20.20	18.15	14.20		1.03			7°	16°

   JEDEC Registration MO-112, Variation CB-1, Issue B, Sept.1995.

   Drawings not to scale.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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