TOSHIBA CMOS Digital Integrated Circuits Silicon Monolithic

JBT6L77-AS

Source Driver for TFT LCD Panels

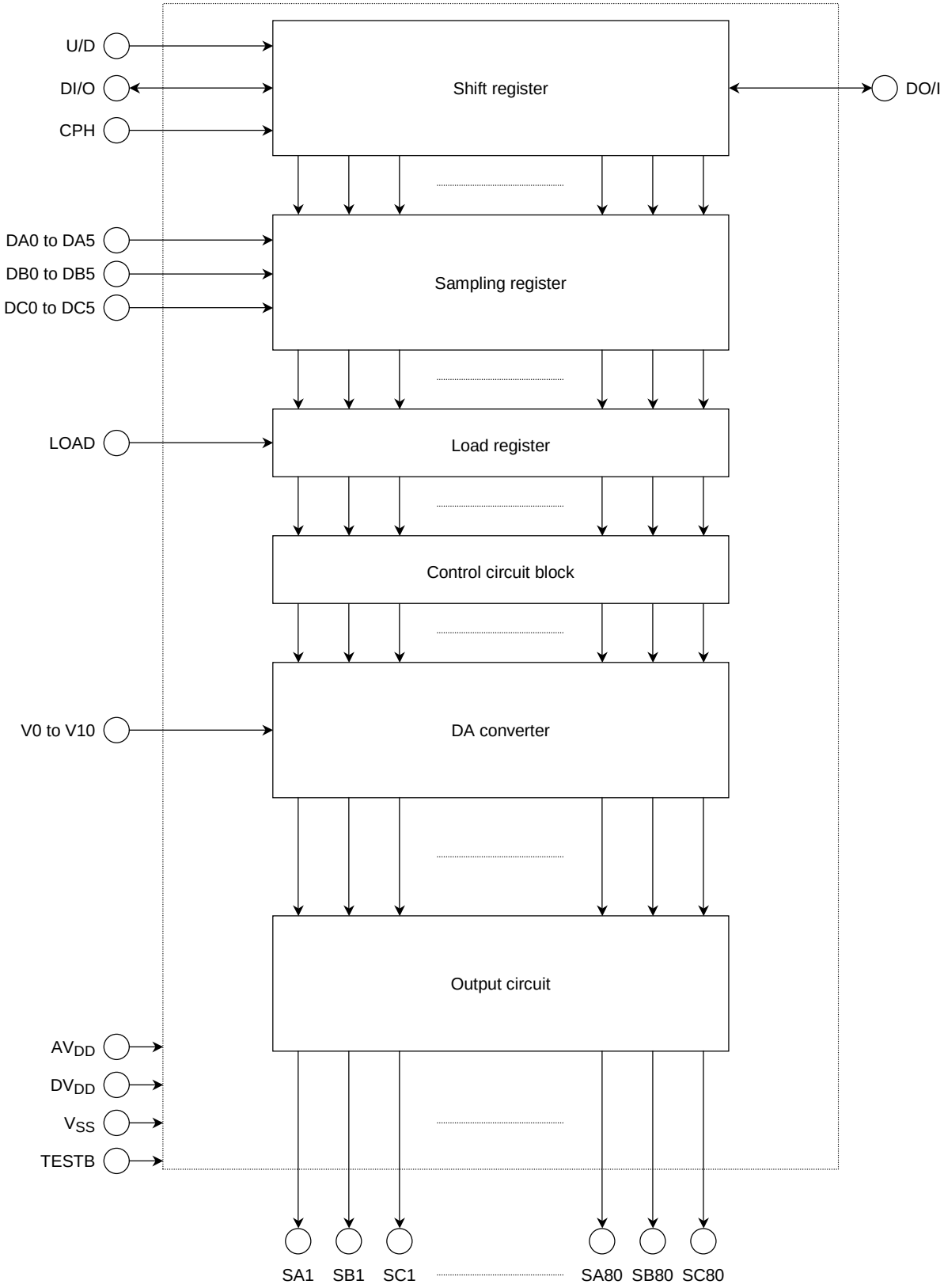
The JBT6L77-AS is a 64 gray-level and 240-channel-output source driver for TFT LCD panels. Grayscale data accepts 6-bit digital data inputs, which combined with the internal DA converter and 11 external power supplies, allows display of up to 260,000 colors.

Based on high-speed CMOS, the JBT6L77-AS offers both low power consumption and high-speed operation.

Features

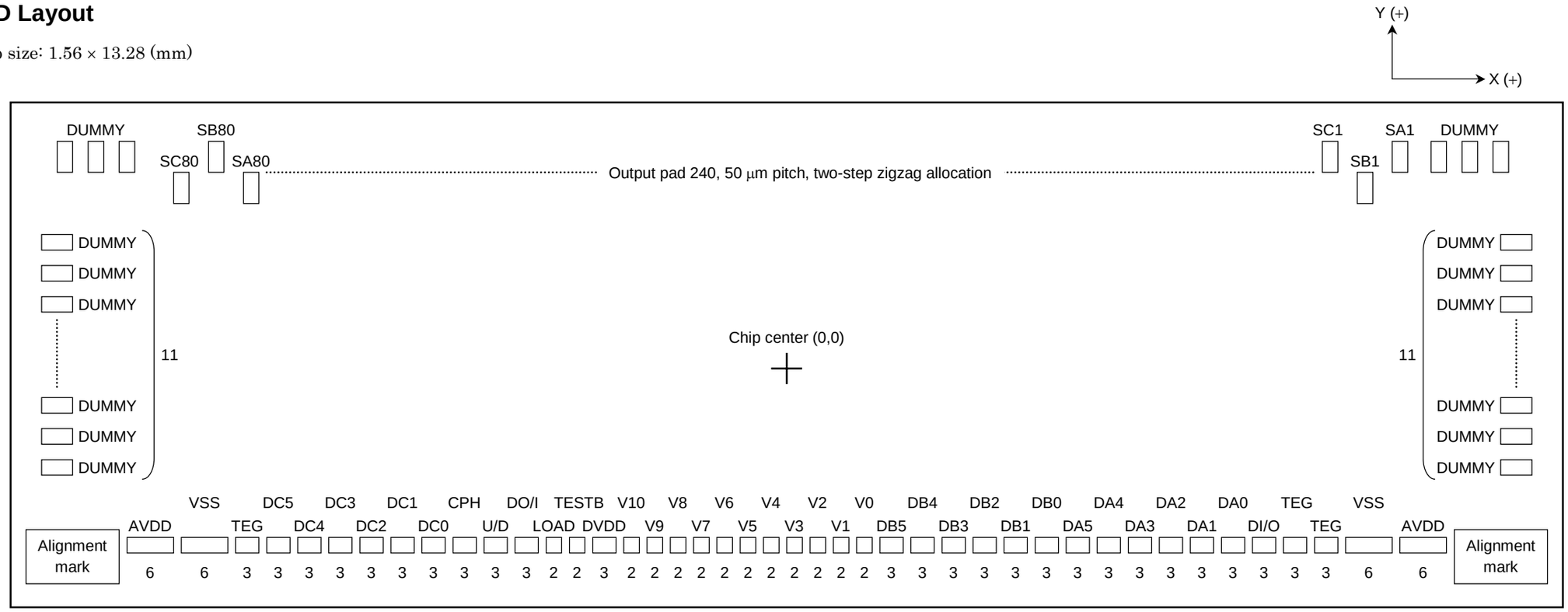
- Grayscale data : 18-bit digital (3 outputs × 6 bits) parallel transfer method, selectable write direction
- Panel drive outputs : 240 outputs, 64 gray levels, DAC system, reference analog voltage inputs
- High-speed operation : 30 MHz (max)
- Power supply voltage : Digital power supply voltage … 2.5 to 3.6 V
  Analog power supply voltage … 5.0 ± 0.5 V
- Operating temperature : −20 to 75°C
- Gate driver for TFT LCD panel : JBT6L78-AS
- Cascading multiple devices

Block Diagram

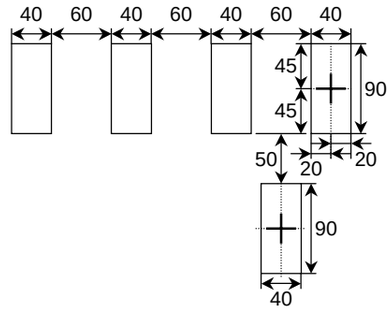


PAD Layout

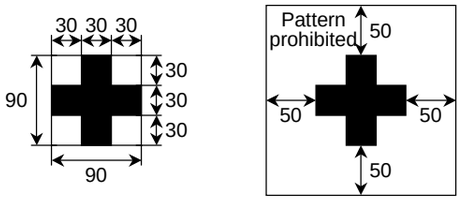
Chip size: 1.56 × 13.28 (mm)



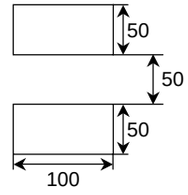
◆ Output side dummy ◆ Output pins (SA1 to SC80)



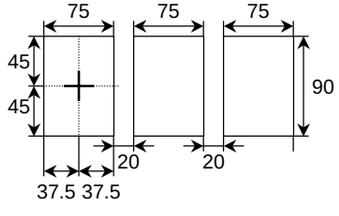
◆ Alignment mark



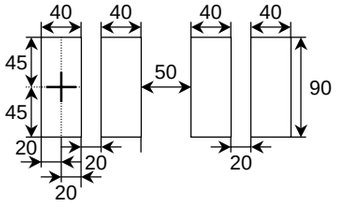
◆ Short-side dummy pins



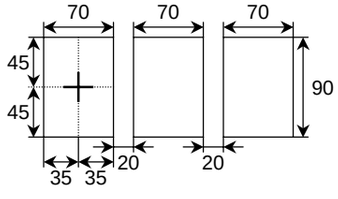
◆ Input pins (AVDD, VSS)



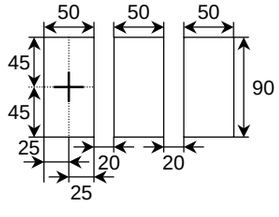
◆ Input pins (V0 to V10, LOAD, TESTB)



◆ Input pins (DVDD)



◆ Input pins (others)



【Unit: μm】

PAD Coordinates

Chip size: 13.28 × 1.56 (mm)
Number of PAD: 396

[Unit: μm]

No.	Name	X Point	Y Point
1	AV_{DD}	−6307.5	−606
2	AV_{DD}	−6212.5	−606
3	AV_{DD}	−6117.5	−606
4	AV_{DD}	−6022.5	−606
5	AV_{DD}	−5927.5	−606
6	AV_{DD}	−5832.5	−606
7	V_{SS}	−5657.5	−606
8	V_{SS}	−5562.5	−606
9	V_{SS}	−5467.5	−606
10	V_{SS}	−5372.5	−606
11	V_{SS}	−5277.5	−606
12	V_{SS}	−5182.5	-606
13	TEG1	−5035.0	-606
14	TEG2	−4965.0	−606
15	TEG3	−4895.0	−606
16	DC5	−4735.0	−606
17	DC5	−4665.0	−606
18	DC5	−4595.0	−606
19	DC4	−4435.0	−606
20	DC4	−4365.0	−606
21	DC4	−4295.0	−606
22	DC3	−4135.0	−606
23	DC3	−4065.0	−606
24	DC3	−3995.0	−606
25	DC2	−3835.0	−606
26	DC2	−3765.0	−606
27	DC2	−3695.0	−606
28	DC1	−3535.0	−606
29	DC1	−3465.0	−606
30	DC1	−3395.0	−606
31	DC0	−3235.0	−606
32	DC0	−3165.0	−606
33	DC0	−3095.0	−606
34	CPH	−2935.0	−606
35	CPH	−2865.0	−606
36	CPH	−2795.0	−606
37	U/D	−2635.0	−606
38	U/D	−2565.0	−606
39	U/D	−2495.0	−606
40	DO/I	−2335.0	−606
41	DO/I	−2265.0	−606
42	DO/I	−2195.0	−606
43	LOAD	−2050.0	−606
44	LOAD	−1990.0	−606
45	TESTB	−1900.0	−606
46	TESTB	−1840.0	−606
47	DV_{DD}	−1715.0	−606
48	DV_{DD}	−1625.0	−606
49	DV_{DD}	−1535.0	−606
50	V10	−1260.0	−606
51	V10	−1200.0	−606
52	V9	−1060.0	−606
53	V9	−1000.0	−606
54	V8	−910.0	−606
55	V8	−850.0	−606
56	V7	−710.0	−606
57	V7	−650.0	−606
58	V6	−560.0	−606
59	V6	−500.0	−606
60	V5	−360.0	-606
61	V5	−300.0	−606
62	V4	−210.0	−606
63	V4	−150.0	−606
64	V3	−10.0	−606
65	V3	50.0	−606
66	V2	140.0	−606
67	V2	200.0	−606
68	V1	340.0	−606
69	V1	400.0	−606
70	V0	490.0	−606
71	V0	550.0	−606
72	DB5	695.0	−606
73	DB5	765.0	−606
74	DB5	835.0	−606
75	DB4	995.0	−606
76	DB4	1065.0	−606
77	DB4	1135.0	−606
78	DB3	1295.0	−606
79	DB3	1365.0	−606
80	DB3	1435.0	−606
81	DB2	1595.0	−606
82	DB2	1665.0	−606
83	DB2	1735.0	−606
84	DB1	1895.0	−606
85	DB1	1965.0	−606
86	DB1	2035.0	−606
87	DB0	2195.0	−606
88	DB0	2265.0	−606
89	DB0	2335.0	−606
90	DA5	2495.0	−606
91	DA5	2565.0	−606
92	DA5	2635.0	−606
93	DA4	2795.0	−606
94	DA4	2865.0	−606
95	DA4	2935.0	−606
96	DA3	3095.0	−606
97	DA3	3165.0	−606
98	DA3	3235.0	−606
99	DA2	3395.0	−606
100	DA2	3465.0	−606
101	DA2	3535.0	−606
102	DA1	3695.0	−606
103	DA1	3765.0	−606
104	DA1	3835.0	−606
105	DA0	3995.0	−606
106	DA0	4065.0	−606
107	DA0	4135.0	−606
108	DI/O	4295.0	−606
109	DI/O	4365.0	−606
110	DI/O	4435.0	−606
111	TEG4	4595.0	−606
112	TEG5	4665.0	−606
113	TEG6	4735.0	−606
114	TEG7	4895.0	−606

[Unit: μm]

No.	Name	X Point	Y Point
115	TEG8	4965.0	−606
116	TEG9	5035.0	−606
117	V_{SS}	5182.5	−606
118	V_{SS}	5277.5	−606
119	V_{SS}	5372.5	−606
120	V_{SS}	5467.5	−606
121	V_{SS}	5562.5	−606
122	V_{SS}	5657.5	−606
123	AV_{DD}	5832.5	−606
124	AV_{DD}	5927.5	−606
125	AV_{DD}	6022.5	−606
126	AV_{DD}	6117.5	−606
127	AV_{DD}	6212.5	−606
128	AV_{DD}	6307.5	−606
129	DUMMY	6488.5	−439
130	DUMMY	6488.5	−339
131	DUMMY	6488.5	−239
132	DUMMY	6488.5	−139
133	DUMMY	6488.5	−39
134	DUMMY	6488.5	61
135	DUMMY	6488.5	161
136	DUMMY	6488.5	261
137	DUMMY	6488.5	361
138	DUMMY	6488.5	461
139	DUMMY	6488.5	561
140	DUMMY	6276.0	621
141	DUMMY	6176.0	621
142	DUMMY	6076.0	621
143	SA1	5976.0	621
144	SB1	5926.0	481
145	SC1	5876.0	621
146	SA2	5826.0	481
147	SB2	5776.0	621
148	SC2	5726.0	481
149	SA3	5676.0	621
150	SB3	5626.0	481
151	SC3	5576.0	621
152	SA4	5526.0	481
153	SB4	5476.0	621
154	SC4	5426.0	481
155	SA5	5376.0	621

No.	Name	X Point	Y Point
156	SB5	5326.0	481
157	SC5	5276.0	621
158	SA6	5226.0	481
159	SB6	5176.0	621
160	SC6	5126.0	481
161	SA7	5076.0	621
162	SB7	5026.0	481
163	SC7	4976.0	621
164	SA8	4926.0	481
165	SB8	4876.0	621
166	SC8	4826.0	481
167	SA9	4776.0	621
168	SB9	4726.0	481
169	SC9	4676.0	621
170	SA10	4626.0	481
171	SB10	4576.0	621
172	SC10	4526.0	481
173	SA11	4476.0	621
174	SB11	4426.0	481
175	SC11	4376.0	621
176	SA12	4326.0	481
177	SB12	4276.0	621
178	SC12	4226.0	481
179	SA13	4176.0	621
180	SB13	4126.0	481
181	SC13	4076.0	621
182	SA14	4026.0	481
183	SB14	3976.0	621
184	SC14	3926.0	481
185	SA15	3876.0	621
186	SB15	3826.0	481
187	SC15	3776.0	621
188	SA16	3726.0	481
189	SB16	3676.0	621
190	SC16	3626.0	481
191	SA17	3576.0	621
192	SB17	3526.0	481
193	SC17	3476.0	621
194	SA18	3426.0	481
195	SB18	3376.0	621
196	SC18	3326.0	481

No.	Name	X Point	Y Point
197	SA19	3276.0	621
198	SB19	3226.0	481
199	SC19	3176.0	621
200	SA20	3126.0	481
201	SB20	3076.0	621
202	SC20	3026.0	481
203	SA21	2976.0	621
204	SB21	2926.0	481
205	SC21	2876.0	621
206	SA22	2826.0	481
207	SB22	2776.0	621
208	SC22	2726.0	481
209	SA23	2676.0	621
210	SB23	2626.0	481
211	SC23	2576.0	621
212	SA24	2526.0	481
213	SB24	2476.0	621
214	SC24	2426.0	481
215	SA25	2376.0	621
216	SB25	2326.0	481
217	SC25	2276.0	621
218	SA26	2226.0	481
219	SB26	2176.0	621
220	SC26	2126.0	481
221	SA27	2076.0	621
222	SB27	2026.0	481
223	SC27	1976.0	621
224	SA28	1926.0	481
225	SB28	1876.0	621
226	SC28	1826.0	481
227	SA29	1776.0	621
228	SB29	1726.0	481
229	SC29	1676.0	621
230	SA30	1626.0	481
231	SB30	1576.0	621
232	SC30	1526.0	481
233	SA31	1476.0	621
234	SB31	1426.0	481
235	SC31	1376.0	621
236	SA32	1326.0	481
237	SB32	1276.0	621

[Unit: μm]

No.	Name	X Point	Y Point
238	SC32	1226.0	481
239	SA33	1176.0	621
240	SB33	1126.0	481
241	SC33	1076.0	621
242	SA34	1026.0	481
243	SB34	976.0	621
244	SC34	926.0	481
245	SA35	876.0	621
246	SB35	826.0	481
247	SC35	776.0	621
248	SA36	726.0	481
249	SB36	676.0	621
250	SC36	626.0	481
251	SA37	576.0	621
252	SB37	526.0	481
253	SC37	476.0	621
254	SA38	426.0	481
255	SB38	376.0	621
256	SC38	326.0	481
257	SA39	276.0	621
258	SB39	226.0	481
259	SC39	176.0	621
260	SA40	126.0	481
261	SB40	76.0	621
262	SC40	26.0	481
263	SA41	−24.0	621
264	SB41	−74.0	481
265	SC41	−124.0	621
266	SA42	−174.0	481
267	SB42	−224.0	621
268	SC42	−274.0	481
269	SA43	−324.0	621
270	SB43	−374.0	481
271	SC43	−424.0	621
272	SA44	−474.0	481
273	SB44	−524.0	621
274	SC44	−574.0	481
275	SA45	−624.0	621
276	SB45	−674.0	481
277	SC45	−724.0	621
278	SA46	−774.0	481
279	SB46	−824.0	621
280	SC46	−874.0	481
281	SA47	−924.0	621
282	SB47	−974.0	481
283	SC47	−1024.0	621
284	SA48	−1074.0	481
285	SB48	−1124.0	621
286	SC48	−1174.0	481
287	SA49	−1224.0	621
288	SB49	−1274.0	481
289	SC49	−1324.0	621
290	SA50	−1374.0	481
291	SB50	−1424.0	621
292	SC50	−1474.0	481
293	SA51	−1524.0	621
294	SB51	−1574.0	481
295	SC51	−1624.0	621
296	SA52	−1674.0	481
297	SB52	−1724.0	621
298	SC52	−1774.0	481
299	SA53	−1824.0	621
300	SB53	−1874.0	481
301	SC53	−1924.0	621
302	SA54	−1974.0	481
303	SB54	−2024.0	621
304	SC54	−2074.0	481
305	SA55	−2124.0	621
306	SB55	−2174.0	481
307	SC55	−2224.0	621
308	SA56	−2274.0	481
309	SB56	−2324.0	621
310	SC56	−2374.0	481
311	SA57	−2424.0	621
312	SB57	−2474.0	481
313	SC57	−2524.0	621
314	SA58	−2574.0	481
315	SB58	−2624.0	621
316	SC58	−2674.0	481
317	SA59	−2724.0	621
318	SB59	−2774.0	481
319	SC59	−2824.0	621
320	SA60	−2874.0	481
321	SB60	−2924.0	621
322	SC60	−2974.0	481
323	SA61	−3024.0	621
324	SB61	−3074.0	481
325	SC61	−3124.0	621
326	SA62	−3174.0	481
327	SB62	−3224.0	621
328	SC62	−3274.0	481
329	SA63	−3324.0	621
330	SB63	−3374.0	481
331	SC63	−3424.0	621
332	SA64	−3474.0	481
333	SB64	-3524.0	621
334	SC64	−3574.0	481
335	SA65	−3624.0	621
336	SB65	−3674.0	481
337	SC65	−3724.0	621
338	SA66	−3774.0	481
339	SB66	−3824.0	621
340	SC66	-3874.0	481
341	SA67	-3924.0	621
342	SB67	−3974.0	481
343	SC67	−4024.0	621
344	SA68	−4074.0	481
345	SB68	−4124.0	621
346	SC68	−4174.0	481
347	SA69	−4224.0	621
348	SB69	−4274.0	481
349	SC69	−4324.0	621
350	SA70	−4374.0	481
351	SB70	−4424.0	621
352	SC70	−4474.0	481
353	SA71	−4524.0	621
354	SB71	−4574.0	481
355	SC71	−4624.0	621
356	SA72	−4674.0	481
357	SB72	−4724.0	621
358	SC72	−4774.0	481
359	SA73	−4824.0	621
360	SB73	−4874.0	481

[Unit: μm]

No.	Name	X Point	Y Point
361	SC73	−4924.0	621
362	SA74	−4974.0	481
363	SB74	−5024.0	621
364	SC74	−5074.0	481
365	SA75	−5124.0	621
366	SB75	−5174.0	481
367	SC75	−5224.0	621
368	SA76	−5274.0	481
369	SB76	−5324.0	621
370	SC76	−5374.0	481
371	SA77	−5424.0	621
372	SB77	−5474.0	481
373	SC77	−5524.0	621
374	SA78	−5574.0	481
375	SB78	−5624.0	621
376	SC78	−5674.0	481
377	SA79	−5724.0	621
378	SB79	−5774.0	481
379	SC79	−5824.0	621
380	SA80	−5874.0	481
381	SB80	−5924.0	621
382	SC80	−5974.0	481
383	DUMMY	−6024.0	621
384	DUMMY	−6124.0	481
385	DUMMY	−6224.0	621
386	DUMMY	−6488.5	561
387	DUMMY	−6488.5	461
388	DUMMY	−6488.5	361
389	DUMMY	−6488.5	261
390	DUMMY	−6488.5	161
391	DUMMY	−6488.5	61
392	DUMMY	−6488.5	−39
393	DUMMY	−6488.5	−139
394	DUMMY	−6488.5	−239
395	DUMMY	−6488.5	−339
396	DUMMY	−6488.5	−439
—	Aligment mark	6464.0	−605
—	Aligment mark	−6464.0	−605

Pin Function

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th></tr>
<tr><td>DI/O
DO/I</td><td>I/O</td><td>Data transfer enable pin
These pins are used to input/output grayscale data.
Input and output are switched as shown below according to the setting of the U/D pin.
<table><tr><th>U/D</th><th>DI/O</th><th>DO/I</th></tr><tr><td>H</td><td>Input</td><td>Output</td></tr><tr><td>L</td><td>Output</td><td>Input</td></tr></table>When set for input
A high on DI/O or DO/I is latched into the internal logic synchronously with the rising edge of CPH. When the internal circuit is in standby state, the device is ready to transfer data.
The grayscale data is latched in sequentially, starting at the next rise of CPH.
When set for output
The pin is used to transfer the enable signal to the JBT6L77-AS at the next stage of the LCD driver.
The pin enters standby state after outputting a high.</td></tr>
<tr><td>U/D</td><td>I</td><td>Transfer direction select pin
This pin controls the direction in which the data is transferred into the sampling register.
Data is transferred synchronously with each rising edge of CPH in one of the following sequences:
When U/D is high, data is transferred in the order SA1 to SC1, SA2 to SC2, SA3 to SC3, …
When U/D is low, the direction is reversed to give SA80 to SC80, SA79 to SC79, SA78 to SC78, …
The voltage applied to this pin must be a DC-level voltage that is either high or low.</td></tr>
<tr><td>CPH</td><td>I</td><td>Sampling clock input
This clock input is used to transfer grayscale data.
In sync with the rising edge of CPH, writes grayscale data bus data to the sampling register.</td></tr>
<tr><td>DA0 to DA5
DB0 to DB5
DC0 to DC5</td><td>I</td><td>Grayscale data bus
The data inputs consist of 6-bit word for each three channel that are transferred in parallel at the rising edge of CPH. The relationship between the grayscale data and the weight of each bit is as follows:
Grayscale data = 32 × Dw5 + 16 × Dw4 + 8 × Dw3 + 4 × Dw2 + 2 × Dw1 + Dw0
(*) w = A, B, C</td></tr>
<tr><td>LOAD</td><td>I</td><td>Data load input pin
When a high voltage supplys to the load input, the data is transferred from the Sampling register to the Load register synchronously at the rising edge of CPH.
(Note) After High level is input to this pin (LOAD), input CPH for at least three cycles in the same cycle as that for sampling.
• When LOAD = Low level, output is at high impedance.
• When LOAD = High level, output corresponds to grayscale data.</td></tr>
<tr><td>V0 to V10</td><td>I</td><td>Reference analog input pins
These pins are used to input the voltage used for the DAC.
$V_{SS} < V0 \leqq V1 \leqq \ldots \leqq V9 \leqq V10 <$ AVDD or AVDD $> V0 \geqq V1 \geqq \ldots \geqq V9 \geqq V10 > V_{SS}$</td></tr>
<tr><td>TESTB</td><td>I</td><td>Test pin
Leave this pin open or V_{DD} level.</td></tr>
<tr><td>SA1 to SA80
SB1 to SB80
SC1 to SC80</td><td>O</td><td>LCD panel drive pins</td></tr>
<tr><td>AV_{DD}</td><td></td><td>Analog power supply pin</td></tr>
<tr><td>DV_{DD}</td><td></td><td>Digital power supply pin.</td></tr>
<tr><td>V_{SS}</td><td></td><td>GND pin</td></tr>
</table>

Device Operation

(1) Starting data transfer

A high input to the data transfer enable pin (DI/O or DO/I) is latched into the internal logic synchronously with the rising edge of CPH, setting the device ready to transfer data. Data transfer starts at the next rise of CPH (see Timing diagram 1 and 2).

(2) Data transfer method

The data is latched in from the grayscale bus to the sampling register synchronously with each rising edge of CPH.
Grayscale data for three outputs are latched into the device simultaneously in one transfer.
Grayscale data are written as three outputs in parallel during one transfer. Data transfer completes after 80 transfers. Then the device enters Standby mode.
Data written to the sampling register are the operation result of the grayscale data bus.

(3) Terminating data transfer

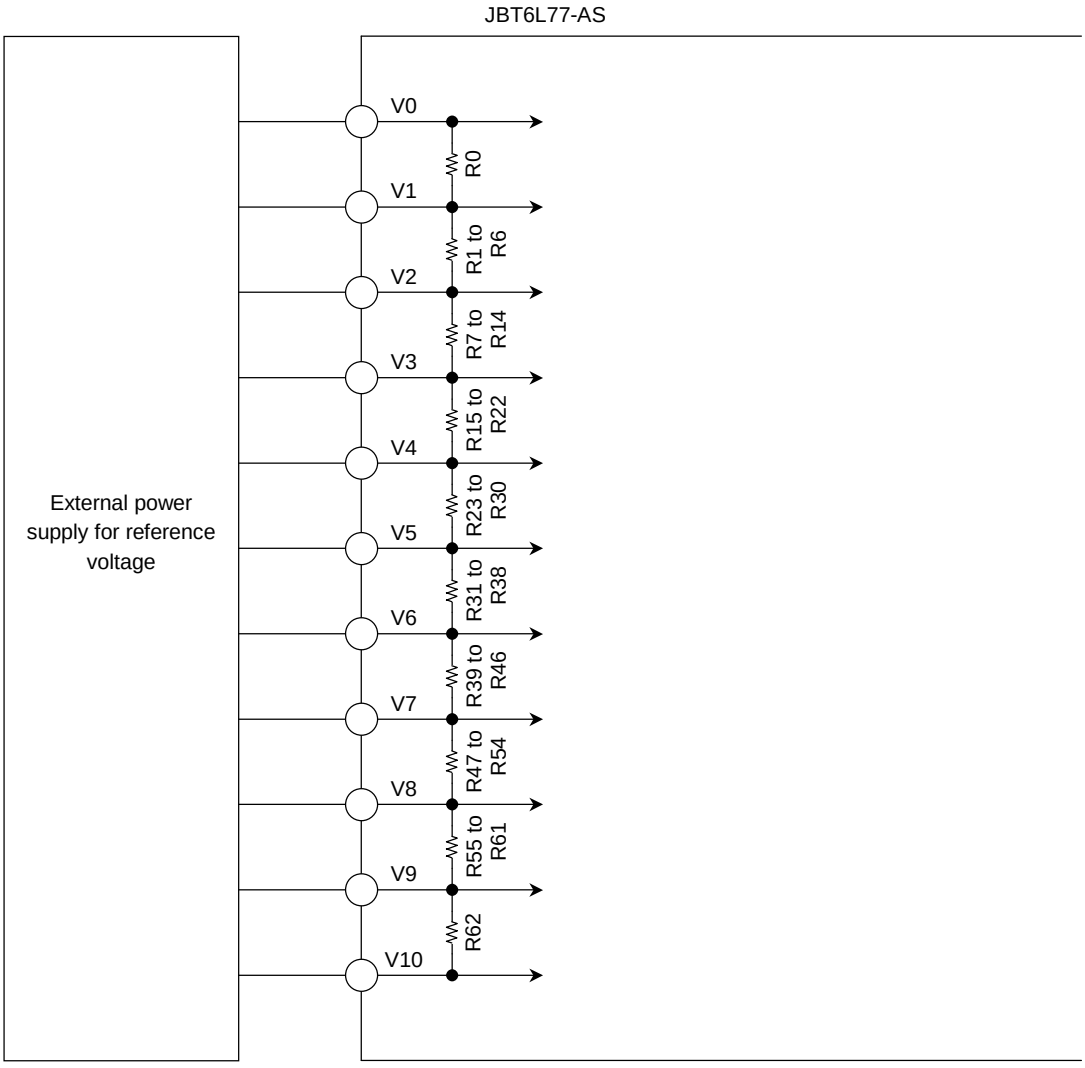
The data transfer enable pin (DO/I or DI/O) output goes high synchronously with the rising edge of CPH one clock period before the last data is latched in. It is held high until the next rise of CPH (see Timing diagram 1 and 2).
The output from this pin can be connected directly as input to the data transfer enable pin (DI/O or DO/I) of the next stage LCD driver. In this way, multiple devices can be easily cascaded to drive a large screen.

(4) Panel drive output

When a high voltage supplies to the load input, the data in the sampling register is transferred to the load register and the device starts updating output to the LCD panel drive pins.

(5) Reference power supply circuit

The connection between the device and the external reference power supply for Reference analog supply is configured with 1, 7 or 8 resistors in series (total of 63 resistor ladders).

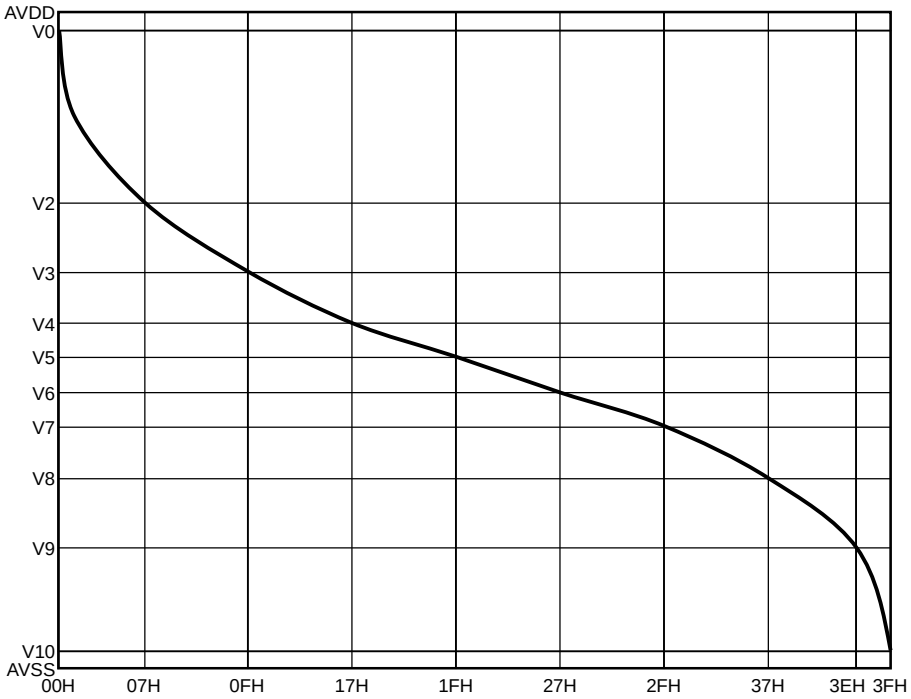


Resistor Name	Resistance Value (Ω)	Resistor Name	Resistance Value (Ω)
R0	6247	R32	62
R1	2186	R33	125
R2	1312	R34	125
R3	875	R35	125
R4	687	R36	187
R5	625	R37	62
R6	500	R38	125
R7	375	R39	125
R8	375	R40	125
R9	312	R41	125
R10	250	R42	125
R11	312	R43	125
R12	312	R44	187
R13	187	R45	125
R14	187	R46	125
R15	250	R47	125
R16	187	R48	187
R17	187	R49	125
R18	187	R50	187
R19	187	R51	125
R20	187	R52	187
R21	125	R53	187
R22	187	R54	187
R23	125	R55	250
R24	125	R56	187
R25	125	R57	312
R26	187	R58	312
R27	125	R59	375
R28	125	R60	437
R29	125	R61	687
R30	125	R62	6746
R31	187		

(6) Grayscale data and output voltages

The LCD drive output voltages are determined by the grayscale values and the 11 reverence analog inputs line voltages (V0 to V11).

- **Schematic representation of reference analog voltage inputs**



- **Grayscale data and output voltages**

  (Input voltage: V0 = 4.90 V, V10 = 0.10 V)

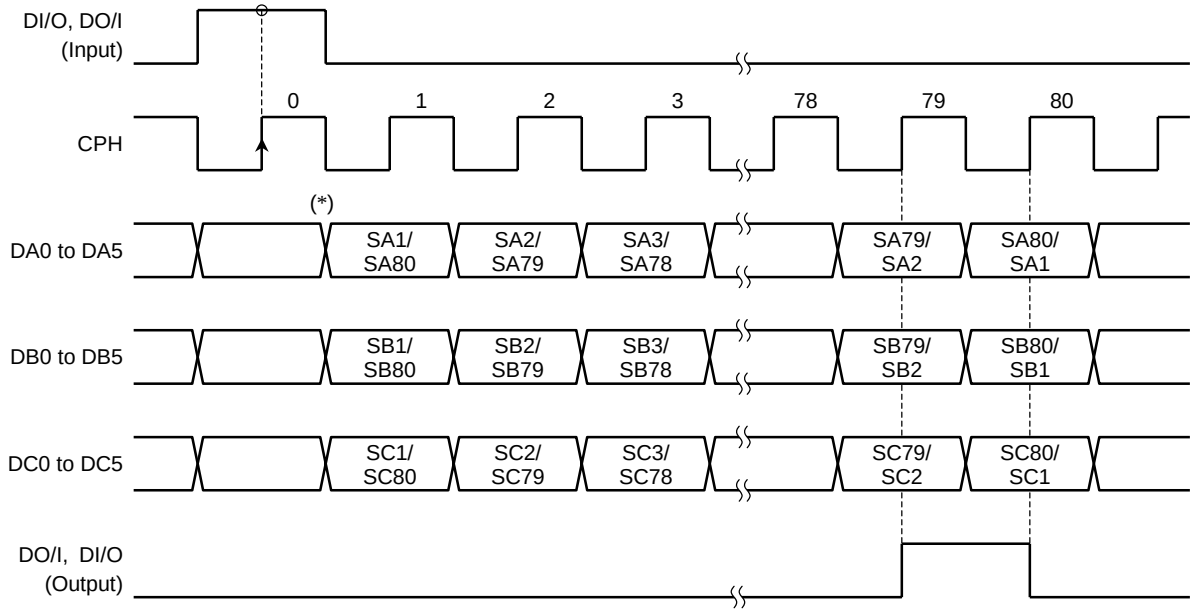
(*) w = A, B, C

Grayscale Data	Dw5	Dw4	Dw3	Dw2	Dw1	Dw0	Output Voltage		
00H	0	0	0	0	0	0	V00H	V0	4.90
01H	0	0	0	0	0	1	V01H		3.90
02H	0	0	0	0	1	0	V02H		3.55
03H	0	0	0	0	1	1	V03H		3.34
04H	0	0	0	1	0	0	V04H		3.20
05H	0	0	0	1	0	1	V05H		3.09
06H	0	0	0	1	1	0	V06H		2.99
07H	0	0	0	1	1	1	V07H	V2	2.91
08H	0	0	1	0	0	0	V08H		2.85
09H	0	0	1	0	0	1	V09H		2.79
0AH	0	0	1	0	1	0	V0AH		2.74
0BH	0	0	1	0	1	1	V0BH		2.70
0CH	0	0	1	1	0	0	V0CH		2.65
0DH	0	0	1	1	0	1	V0DH		2.60
0EH	0	0	1	1	1	0	V0EH		2.57
0FH	0	0	1	1	1	1	V0FH	V3	2.54
10H	0	1	0	0	0	0	V10H		2.50
11H	0	1	0	0	0	1	V11H		2.47
12H	0	1	0	0	1	0	V12H		2.44
13H	0	1	0	0	1	1	V13H		2.41
14H	0	1	0	1	0	0	V14H		2.38
15H	0	1	0	1	0	1	V15H		2.35
16H	0	1	0	1	1	0	V16H		2.33
17H	0	1	0	1	1	1	V17H	V4	2.30
18H	0	1	1	0	0	0	V18H		2.28
19H	0	1	1	0	0	1	V19H		2.26
1AH	0	1	1	0	1	0	V1AH		2.24
1BH	0	1	1	0	1	1	V1BH		2.21
1CH	0	1	1	1	0	0	V1CH		2.19
1DH	0	1	1	1	0	1	V1DH		2.17
1EH	0	1	1	1	1	0	V1EH		2.15
1FH	0	1	1	1	1	1	V1FH	V5	2.13

(*) w = A, B, C

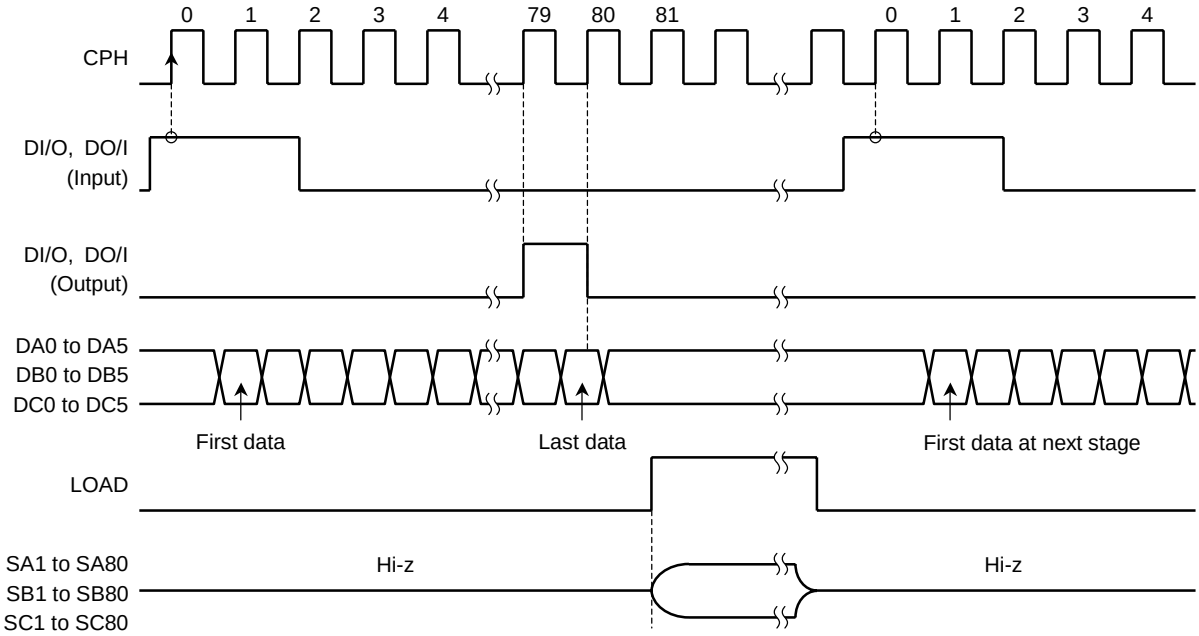
Grayscale Data	Dw5	Dw4	Dw3	Dw2	Dw1	Dw0	Output Voltage		
20H	1	0	0	0	0	0	V20H		2.10
21H	1	0	0	0	0	1	V21H		2.09
22H	1	0	0	0	1	0	V22H		2.07
23H	1	0	0	0	1	1	V23H		2.05
24H	1	0	0	1	0	0	V24H		2.03
25H	1	0	0	1	0	1	V25H		2.00
26H	1	0	0	1	1	0	V26H		1.99
27H	1	0	0	1	1	1	V27H	V6	1.97
28H	1	0	1	0	0	0	V28H		1.95
29H	1	0	1	0	0	1	V29H		1.93
2AH	1	0	1	0	1	0	V2AH		1.91
2BH	1	0	1	0	1	1	V2BH		1.89
2CH	1	0	1	1	0	0	V2CH		1.87
2DH	1	0	1	1	0	1	V2DH		1.84
2EH	1	0	1	1	1	0	V2EH		1.82
2FH	1	0	1	1	1	1	V2FH	V7	1.80
30H	1	1	0	0	0	0	V30H		1.78
31H	1	1	0	0	0	1	V31H		1.75
32H	1	1	0	0	1	0	V32H		1.73
33H	1	1	0	0	1	1	V33H		1.70
34H	1	1	0	1	0	0	V34H		1.68
35H	1	1	0	1	0	1	V35H		1.65
36H	1	1	0	1	1	0	V36H		1.62
37H	1	1	0	1	1	1	V37H	V8	1.59
38H	1	1	1	0	0	0	V38H		1.55
39H	1	1	1	0	0	1	V39H		1.52
3AH	1	1	1	0	1	0	V3AH		1.47
3BH	1	1	1	0	1	1	V3BH		1.42
3CH	1	1	1	1	0	0	V3CH		1.36
3DH	1	1	1	1	0	1	V3DH		1.29
3EH	1	1	1	1	1	0	V3EH	V9	1.18
3FH	1	1	1	1	1	1	V3FH	V10	0.10

Timing Diagrams 1



(*) Upper stage: SA1 → U/D = High
Lower stage: SA80 → U/D = Low

Timing Diagrams 2



Absolute Maximum Ratings (V_{SS} = 0 V)

Characteristics	Symbol	Rating	Unit	Relevant Pin
Analog supply voltage	DV_{DD}	−0.3 to 6.5	V	
Digital supply voltage	AV_{DD}	−0.3 to 6.5	V	
Input voltage	V_{IN}	−0.3 to DV_{DD} + 0.3	V	
Reference analog voltage	V (0:10)	−0.3 to AV_{DD} + 0.3	V	V0 to V10
Storage temperature	Tstg	−55 to 125	°C	

Recommended Operating Conditions (V_{SS} = 0 V)

Characteristics	Symbol	Test Condition	Rating	Unit	Relevant Pin
Digital supply voltage	DV_{DD}	—	2.5 to 3.6	V	
Analog supply voltage	AV_{DD}	—	4.5 to 5.5	V	
Reference analog voltage-1 (Note 1)	V0 to V10	—	0.1 to AV_{DD} − 0.1	V	
Operating temperature	Topr	—	−20 to 75	°C	
Operating frequency	f_{CPH}	—	DC to 30	MHz	CPH
Output load capacitance	C_L	—	100 (max)	pF/ PIN	SA1 to SA80 SB1 to SB80 SC1 to SC80

Note 1: The following shows the relative magnitude of each reference analog voltage:

$V_{SS} = V0 < V1 \leqq V2 \leqq V3 \leqq V4 \leqq V5 \leqq V6 \leqq V7 \leqq V8 \leqq V9 < V10 < AV_{DD}$

or

$V_{SS} = V10 < V9 \leqq V8 \leqq V7 \leqq V6 \leqq V5 \leqq V4 \leqq V3 \leqq V2 \leqq V1 < V0 < AV_{DD}$

Electrical Characteristics

DC Characteristics (V_{SS} = 0 V, DV_{DD} = 2.5 to 3.6 V, AV_{DD} = 4.5 V to 5.5 V, Ta = −20 to 75°C)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit	Relevant Pin
Input current	Low level	I_{ILL1}	—	—	—	—	10	μA	(Note 2)
		I_{ILL2}		—	—	—	400		TESTB
	High level	I_{IH}		—	—	—	10		(Note 3)
Input voltage	Low level	V_{IL}	—	—	0	—	0.2 × DV_{DD}	V	(Note 4)
	High level	V_{IH}		—	0.8 × DV_{DD}	—	DV_{DD}		
Output voltage	Low level	V_{OL}	—	I_{OL} = 0.1 mA	0	—	0.5	V	DI/O, DO/I
	High level	V_{OH}		I_{OH} = −0.1 mA	DV_{DD} − 0.5	—	DV_{DD}		
Output off current		I_{OFF}	—	(Note 7)	—	—	10	μA	SA1 to SA80 SB1 to SB80 SC1 to SC80
Output voltage range		V_{OUT}		—	0.1	—	AV_{DD} − 0.1		
Output voltage deviation		V_{DO1}	—	0.1 ≦ Reference analog voltage ≦ 1.2	−40	—	40	mV	
		V_{DO2}		1.2 < Reference analog voltage ≦ 4.9	−30	—	30		
Current consumption (1)		DI_{DD}	—	During operations (Note 5)	—	—	4	mA	DV_{DD}
				When no, operations (Note 6)	—	—	3		
Current consumption (2)		AI_{DD}	—	During operations (Note 5)	—	—	8	mA	AV_{DD}
				When no, operations (Note 6)	—	—	8		
				LOAD = Low (Note 7)	—	—	100	μA	

Note 2: DA0 to DA5, DB0 to DB5, DC0 to DC5, DI/O, DO/I, CPH, LOAD, U/D

Note 3: DA0 to DA5, DB0 to DB5, DC0 to DC5, DI/O, DO/I, CPH, LOAD, U/D, TESTB

Note 4: DA0 to DA5, DB0 to DB5, DC0 to DC5, DI/O, DO/I, CPH, LOAD

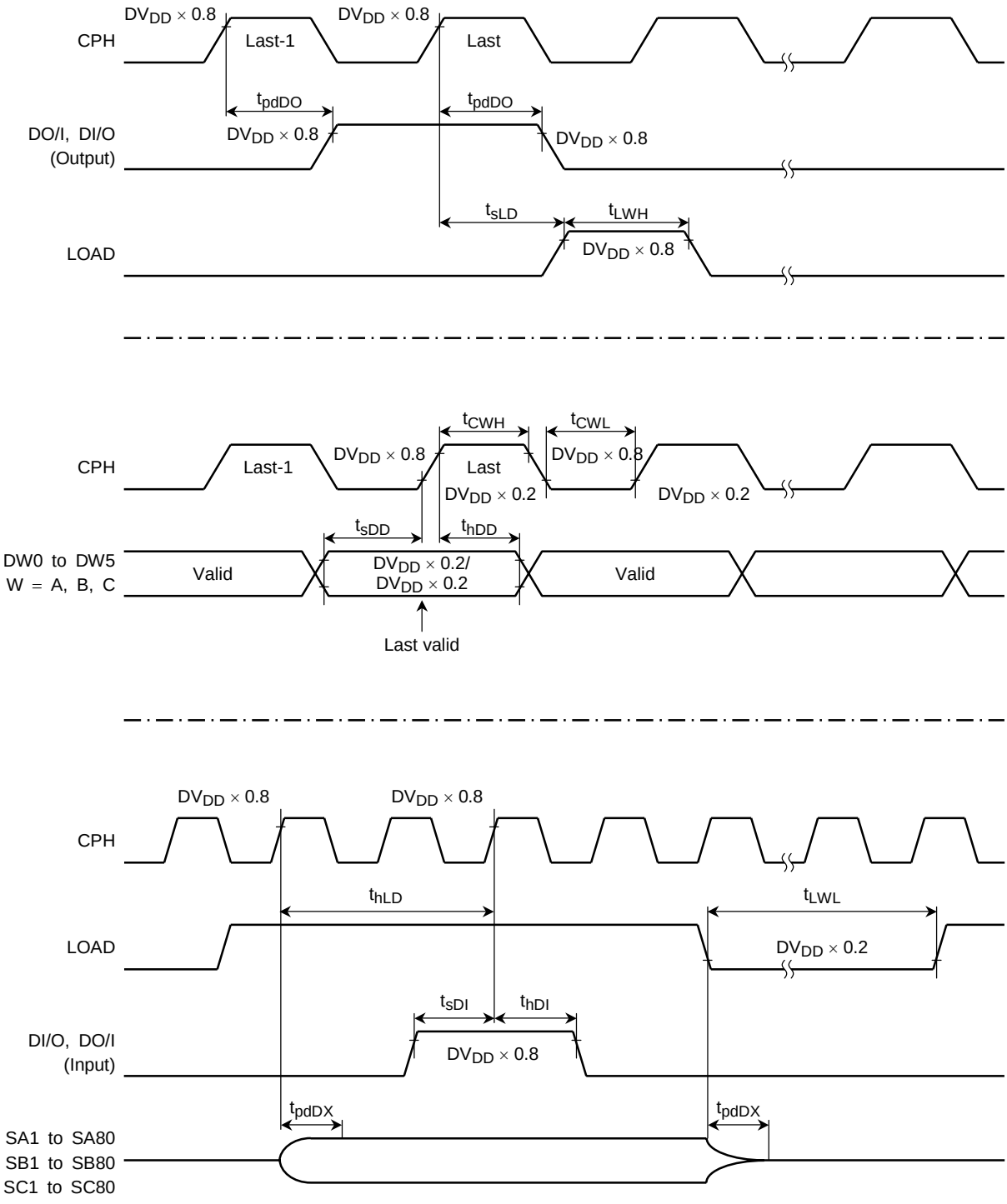
Note 5: DV_{DD} = 3.6 V, AV_{DD} = 5.5 V, f_{CPH} = 30 MHz, 1H = 100 μs, no load, checkerboard pattern, LOAD = 1 μs at low level, typical value

Note 6: AV_{DD} = 5.5 V, f_{CPH} = 30 MHz, 1H = 100 μs, DI/O: Fixed low

Note 7: AV_{DD} = 5.5 V, Standby at LOAD = Low, f_{CPH} = 30 MHz, DI/O: Fixed low

AC Characteristics (V_{SS} = 0 V, DV_{DD} = 2.5 to 3.6 V, AV_{DD} = 4.5 V to 5.5 V, Ta = –20 to 75°C)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
CPH pulse width H	t_{CWH}	—	—	4	—	—	ns
CPH pulse width L	t_{CWL}	—	—	4	—	—	ns
Enable setup time	t_{sDI}	—	—	4	—	—	ns
Enable hold time	t_{hDI}	—	—	0	—	—	ns
Data setup time	t_{sDD}	—	—	4	—	—	ns
Data hold time	t_{hDD}	—	—	0	—	—	ns
LOAD setup time	t_{sLD}	—	—	1	—	—	CPH
LOAD hold time	t_{hLD}	—	—	2	—	—	CPH
LOAD pulse width H	t_{LWH}	—	—	10	—	—	μs
LOAD pulse width L	t_{LWL}	—	—	1	—	—	μs
Output delay time 1	t_{pdDO}	—	C_L = 15 pF	—	—	15	ns
Output delay time 2	t_{pdDX}	—	C_L = 100 pF	—	—	10	μs


CPH
DVDD × 0.8
Last-1
DVDD × 0.8
Last
tpdDO
tpdDO
DO/I, DI/O
(Output)
DVDD × 0.8
DVDD × 0.8
tsLD
tLWH
LOAD
DVDD × 0.8
tCWH
tCWL
CPH
Last-1
DVDD × 0.8
Last
DVDD × 0.8
DVDD × 0.2
DVDD × 0.2
tsDD
thDD
DW0 to DW5
W = A, B, C
Valid
DVDD × 0.2/
DVDD × 0.2
Valid
Last valid
DVDD × 0.8
DVDD × 0.8
CPH
thLD
tLWL
LOAD
DVDD × 0.2
tsDI
thDI
DI/O, DO/I
(Input)
DVDD × 0.8
tpdDX
tpdDX
SA1 to SA80
SB1 to SB80
SC1 to SC80

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