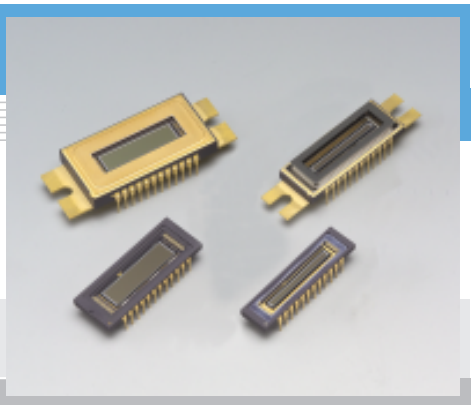
NEW

IMAGE SENSOR



CCD area image sensor
S9972/S9973 series

Front-illuminated FFT-CCD, high IR sensitivity

S9972/S9973 series are families of FFT-CCD image sensors specifically designed for low-light-level detection in scientific applications. By using the binning operation, S9972/S9973 series can be used as a linear image sensor having a long aperture in the direction of the device length. This makes S9972/S9973 series ideally suited for use in spectrophotometry. The binning operation offers significant improvement in S/N and signal processing speed compared with conventional methods by which signals are digitally added by an external circuit. S9972/S9973 series also feature low noise and low dark signal (MPP mode operation). This enables low-light-level detection and long integration time, thus achieving a wide dynamic range.
S9972/S9973 series have an effective pixel size of 24 × 24 µm and are available in image areas of 24.576 (H) × 2.976 (V) mm^2 (1024 × 124 pixels) and 24.576 (H) × 6.048 (V) mm^2 (1024 × 252 pixels). S9972/S9973 series are pin compatible with S9970/S9971 series. (Operating conditions and characteristics are a little bit different from S9970/S9971 series.)

Features

- 1024 (H) × 124 (V) and 1024 (H) × 252 (V) pixel format
- Pixel size: 24 × 24 µm
- Line/pixel binning
- 100 % fill factor
- Wide dynamic range
- Low dark signal
- Low readout noise
- MPP operation
- High IR sensitivity

Applications

- Fluorescence spectrometer, ICP
- Raman spectrometer
- Industrial inspection requiring
- Semiconductor inspection
- DNA sequencer
- Low-light-level detection

■ Selection guide

Type No.	Cooling	Number of total pixels	Number of active pixels	Active area [mm (H) × mm (V)]
S9972-1007	Non-cooled	1044 × 128	1024 × 124	24.576 × 2.976
S9972-1008		1044 × 256	1024 × 252	24.576 × 6.048
S9973-1007	One-stage TE-cooled	1044 × 128	1024 × 124	24.576 × 2.976
S9973-1008		1044 × 256	1024 × 252	24.576 × 6.048

■ General ratings

Parameter	Specification
Pixel size	24 (H) × 24 (V) µm
Vertical clock phase	2 phase
Horizontal clock phase	2 phase
Output circuit	One-stage MOSFET source follower
Package	24 pin ceramic DIP (refer to dimensional outlines)
Window *1	S9972 series: quartz glass S9973 series: sapphire glass

*1: Temporary window type and UV coat type are available upon request.
(Temporary window is fixed by tape to protect the CCD chip and wire bonding.)
Temporary window type: expressed by “N” ex. S9972-1007N
UV coat type: expressed by “UV” ex. S9972-1007UV

PRELIMINARY DATA
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SOLID STATE DIVISION

■ Absolute maximum ratings (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating temperature	Topr	-50	-	+30	°C
Storage temperature	Tstg	-50	-	+70	°C
OD voltage	V_{OD}	-0.5	-	+25	V
RD voltage	V_{RD}	-0.5	-	+18	V
ISV voltage	V_{ISV}	-0.5	-	+18	V
ISH voltage	V_{ISH}	-0.5	-	+18	V
IGV voltage	V_{IG1V}, V_{IG2V}	-15	-	+15	V
IGH voltage	V_{IG1H}, V_{IG2H}	-15	-	+15	V
SG voltage	V_{SG}	-15	-	+15	V
OG voltage	V_{OG}	-15	-	+15	V
RG voltage	V_{RG}	-15	-	+15	V
TG voltage	V_{TG}	-15	-	+15	V
Vertical clock voltage	V_{P1V}, V_{P2V}	-15	-	+15	V
Horizontal clock voltage	V_{P1H}, V_{P2H}	-15	-	+15	V

■ Operating conditions (MPP mode, Ta=25 °C)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Output transistor drain voltage		V_{OD}	18	20	22	V
Reset drain voltage		V_{RD}	12	13	14	V
Output gate voltage		V_{OG}	-0.5	0	2	V
Substrate voltage		V_{SS}	-	0	-	V
Test point (vertical input source)		V_{ISV}	-	V_{RD}	-	V
Test point (horizontal input source)		V_{ISH}	-	V_{RD}	-	V
Test point (vertical input gate)		V_{IG1V}, V_{IG2V}	-8	0	-	V
Test point (horizontal input gate)		V_{IG1H}, V_{IG2H}	-8	0	-	V
Vertical shift register clock voltage	High	V_{P1VH}, V_{P2VH}	0	4	6	V
	Low	V_{P1VL}, V_{P2VL}	-9	-8	-7	
Horizontal shift register clock voltage	High	V_{P1HH}, V_{P2HH}	0	4	6	V
	Low	V_{P1HL}, V_{P2HL}	-9	-8	-7	
Summing gate voltage	High	V_{SGH}	0	4	6	V
	Low	V_{SGL}	-9	-8	-7	
Reset gate voltage	High	V_{RGH}	0	4	6	V
	Low	V_{RGL}	-9	-8	-7	
Transfer gate voltage	High	V_{TGH}	0	4	6	V
	Low	V_{TGL}	-9	-8	-7	

■ Electrical characteristics (Ta=25 °C)

Parameter		Symbol	Remark	Min.	Typ.	Max.	Unit
Signal output frequency		fc	-	-	0.1	1	MHz
Vertical shift register capacitance	S9972/S9973-1007	C_{P1V}, C_{P2V}	-	-	1600		pF
	S9972/S9973-1008		-	-	3200		
Horizontal shift register capacitance		C_{P1H}, C_{P2H}	-	-	180		pF
Summing gate capacitance		C_{SG}	-	-	7	-	pF
Reset gate capacitance		C_{RG}	-	-	7	-	pF
Transfer gate capacitance		C_{TG}	-	-	100		pF
Transfer efficiency		CTE	*2	0.99995	0.99999	-	-
DC output level		Vout	*3	12	15	18	V
Output impedance		Zo	*3	-	3	-	kΩ
Power dissipation		P	*3, *4	-	15	-	mW

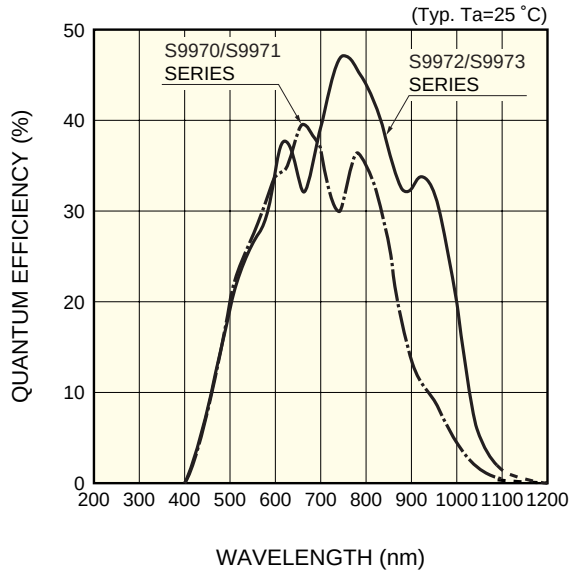
*2: Charge transfer efficiency per pixel, measured at half of the full well capacity.
*3: The values depend on the load resistance. (V_{OD}=20 V, Load resistance=10 kΩ)
*4: Power dissipation of the on-chip amplifier.

■ Electrical and optical characteristics (Ta=25 °C, unless otherwise noted)

Parameter		Symbol	Remark	Min.	Typ.	Max.	Unit
Saturation output voltage		Vsat	-	-	Fw × Sv	-	V
Full well capacity	Vertical	Fw	-	120	240	-	ke⁻
	Horizontal			240	480	-	
CCD node sensitivity		Sv	*5	-	2.8	-	μV/e⁻
Dark current (MPP mode)	+25 °C	DS	*6	-	2000	30000	e⁻/pixel/s
	0 °C			-	100	1500	
Readout noise		Nr	*7	-	4	18	e⁻rms
Dynamic range	Line binning	-	*8	13333	120000	-	-
	Area scanning			6667	60000	-	
Spectral response range		λ	-	-	400 to 1100	-	nm
Photo response non-uniformity		PRNU	*9	-	-	±10	%
Blemish	Point defects	-	*10	-	-	0	-
	Cluster defects		*11	-	-	0	
	Column defects		*12	-	-	0	

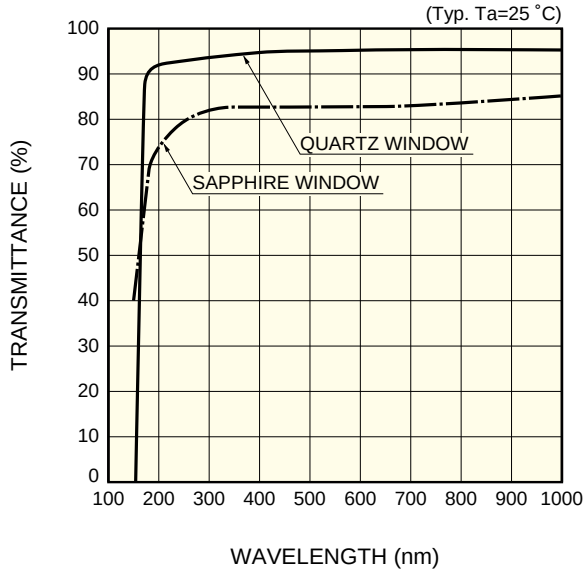
*5: V_{OD}=20 V , Load resistance=10 kΩ
*6: Dark current nearly doubles for every 5 to 7 °C increase in temperature.
*7: -40 °C, operating frequency is 80 kHz.
*8: DR = Fw / Nr
*9: Measured at half of the full well capacity. PRNU = noise / signal × 100 [%], noise: fixed pattern noise (peak to peak)
*10: White spots > 3 % of full well at 0 °C after Ts=1 s
Black spots
Pixels whose sensitivity is lower than one-half of the average pixel output (Measured with uniform light producing one-half of the saturation charge)
*11: 2 to 9 contiguous defective pixels
*12: 10 or more contiguous defective pixels

■ Spectral response (without window)



KMPDB0257EC

■ Spectral transmittance characteristics



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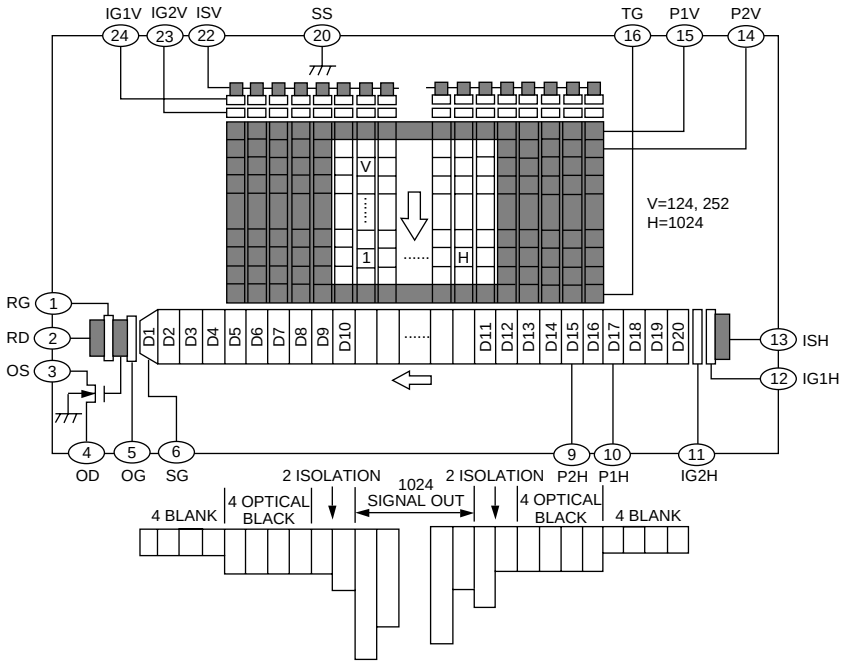
■ Device structure, line output format



KMPDC0237EA

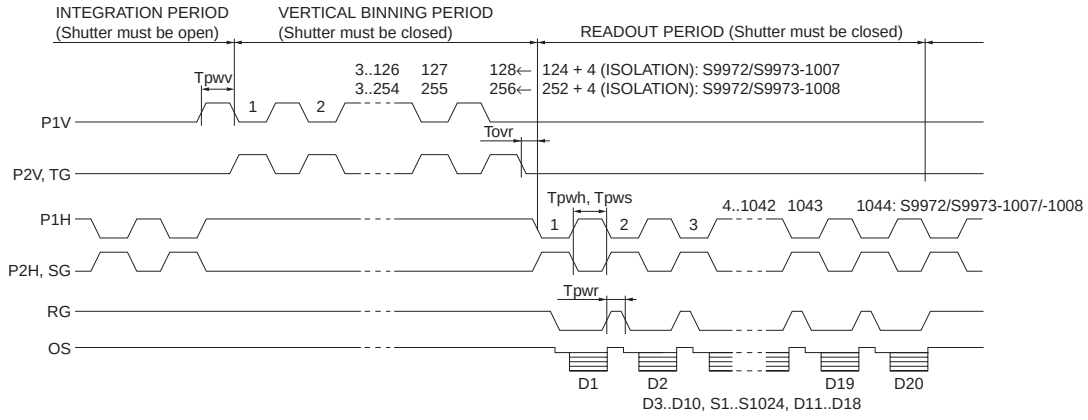
Pixel format

Left ← Horizontal Direction → Right						
Blank	Optical Black	Isolation	Effective	Isolation	Optical Black	Blank
4	4	2	1024	2	4	4

Top ← Vertical Direction → Bottom		
Isolation	Effective	Isolation
2	124 or 252	2

■ Timing chart

Line binning



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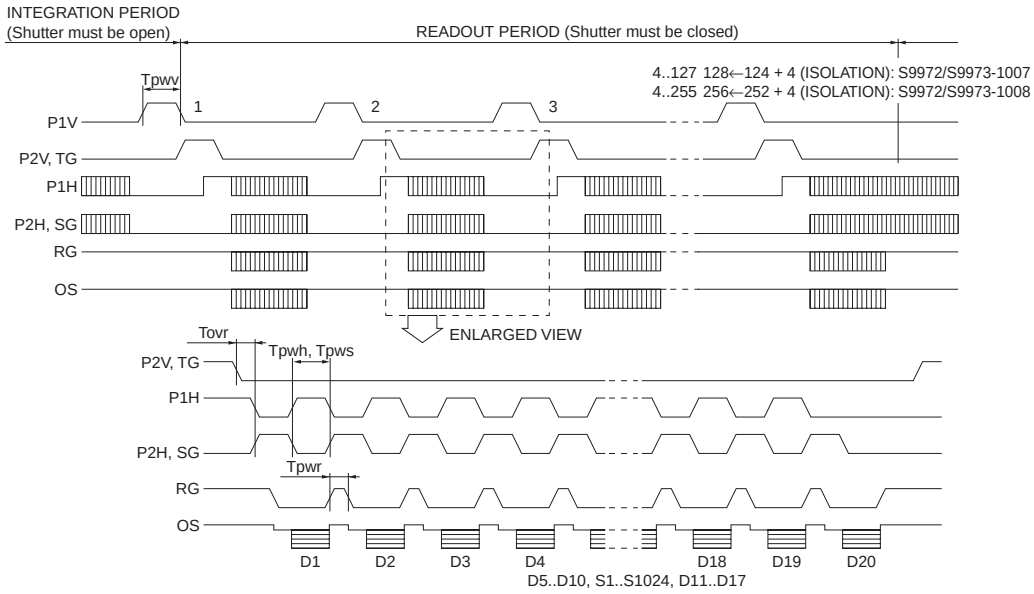
Area scanning 1: low dark current mode



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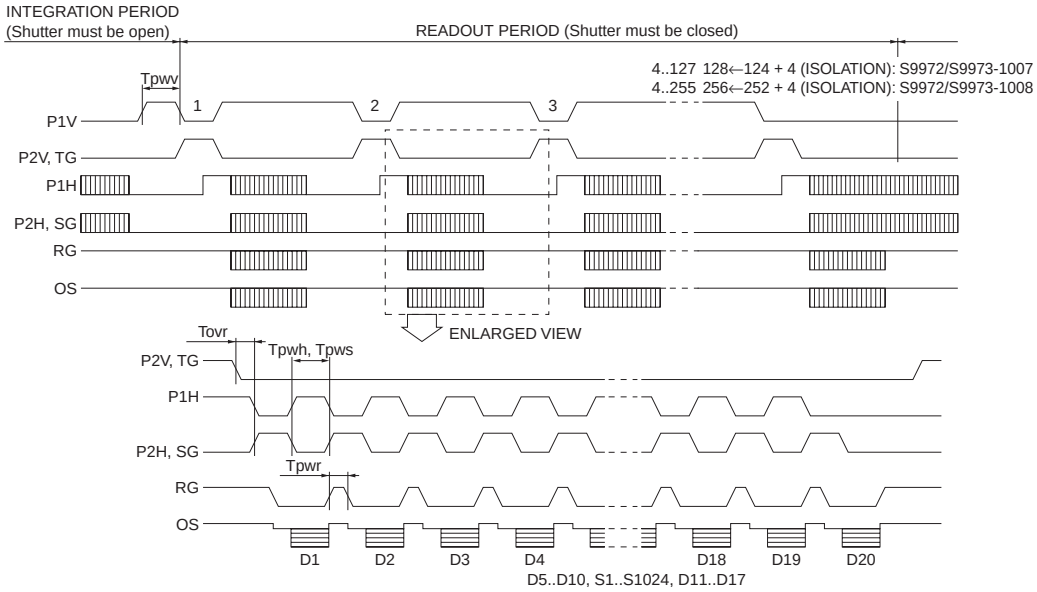
Area scanning 2: large full well mode



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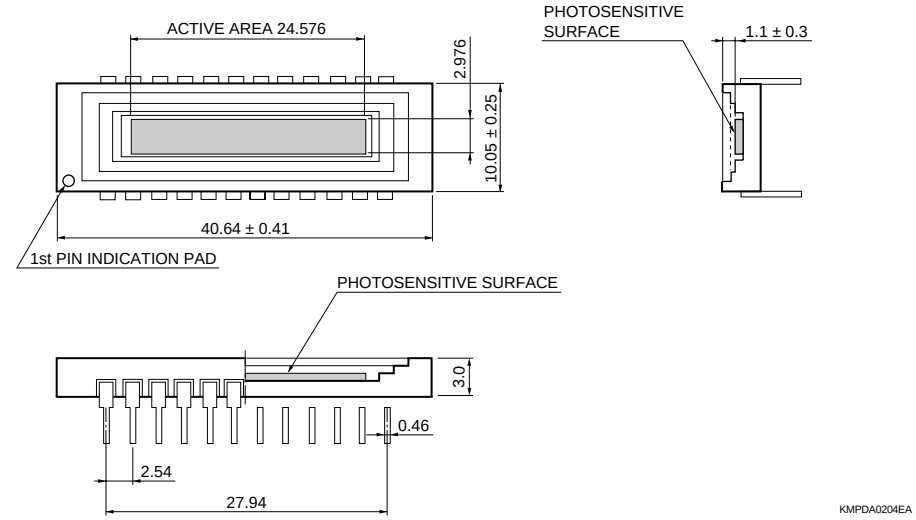
Parameter			Symbol	Remark	Min.	Typ.	Max.	Unit
P1V, P2V, TG	Pulse width	S9972/S9973-1007	Tpwv	*13	6.0	18	-	µs
		S9972/S9973-1008			12	36	-	
	Rise and fall time		Tprv, Tpfv	-	200	-	-	ns
P1H, P2H	Pulse width		Tpwh	-	500	5000	-	ns
	Rise and fall time		Tprh, Tpfh	*13	10	-	-	ns
	Duty ratio		-	-	-	50	-	%
SG	Pulse width		Tpws	*14	500	5000	-	ns
	Rise and fall time		Tprs, Tpfs	-	10	-	-	ns
	Duty ratio		-	-	-	50	-	%
RG	Pulse width		Tpwr	-	100	500	-	ns
	Rise and fall time		Tprr, Tpfr		5	-	-	ns
TG - P1H	Overlap time		Tovr	-	3	6	-	µs

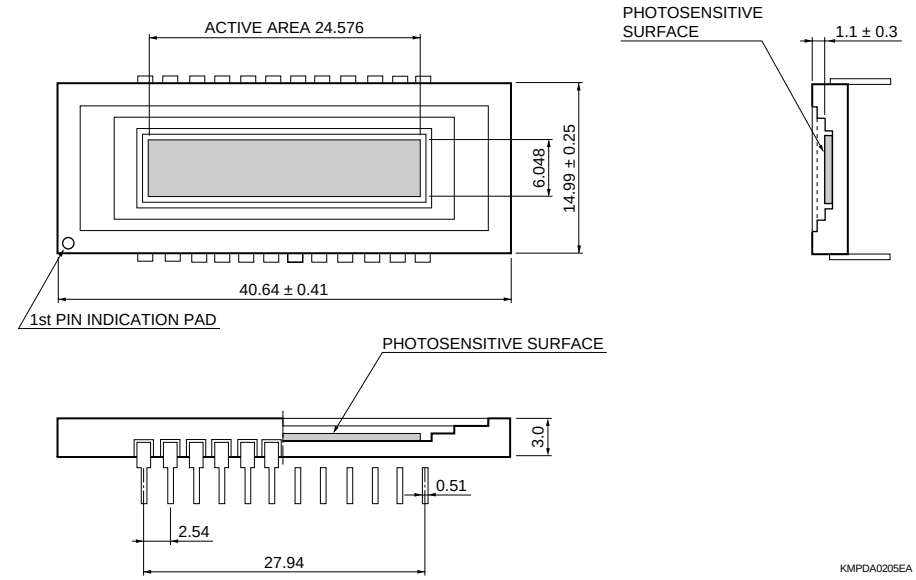
*13: The clock pulses should be overlapped at 50 % of clock pulse amplitude.
*14: P2H and SG should have the same electrical specifications.

■ Dimensional outlines (unit: mm)

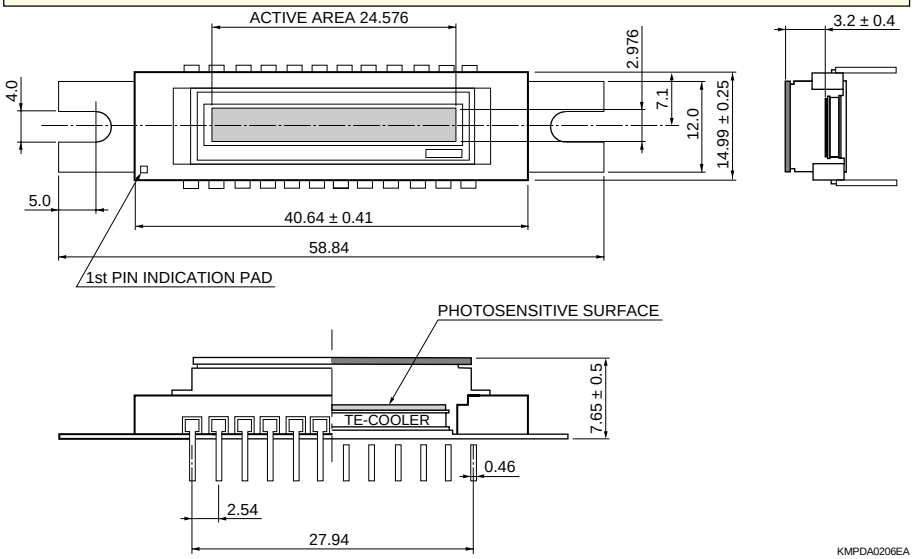
S9972-1007



S9972-1008



S9973-1007



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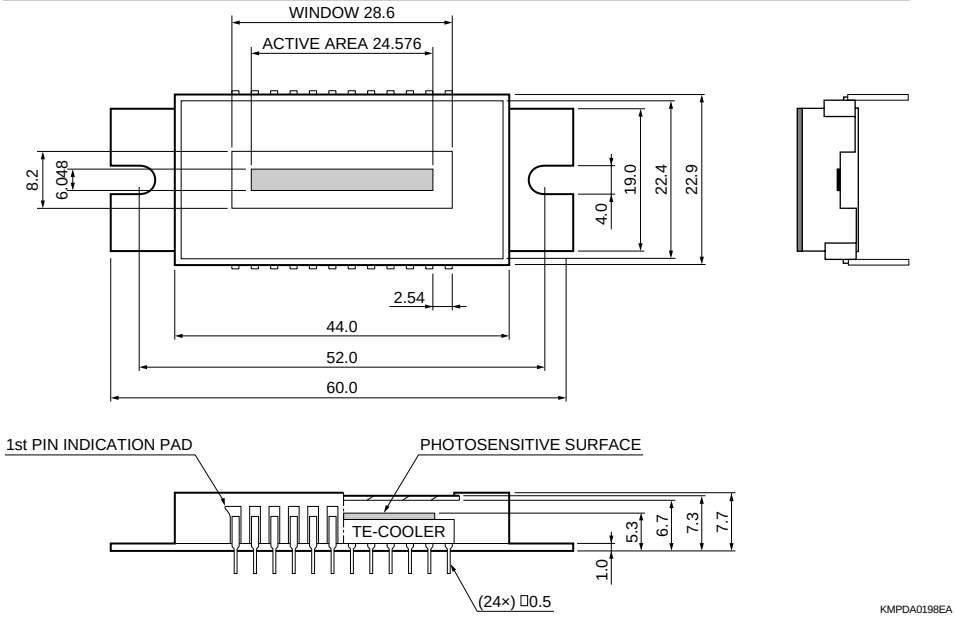


■ Pin connections

Pin No.	S9972 series		S9973 series		Remark
	Symbol	Description	Symbol	Description	
1	RG	Reset gate	RG	Reset gate	
2	RD	Reset drain	RD	Reset drain	
3	OS	Output transistor source	OS	Output transistor source	
4	OD	Output transistor drain	OD	Output transistor drain	
5	OG	Output gate	OG	Output gate	
6	SG	Summing gate	SG	Summing gate	Same timing as P2H
7	NC		Th1	Thermistor	
8	NC		Th2	Thermistor	
9	P2H	CCD horizontal register clock-2	P2H	CCD horizontal register clock-2	
10	P1H	CCD horizontal register clock-1	P1H	CCD horizontal register clock-1	
11	IG2H	Test point (horizontal input gate-2)	IG2H	Test point (horizontal input gate-2)	Shorted to GND
12	IG1H	Test point (horizontal input gate-1)	IG1H	Test point (horizontal input gate-1)	Shorted to GND
13	ISH	Test point (horizontal input source)	ISH	Test point (horizontal input source)	Shorted to RD
14	P2V	CCD vertical register clock-2	P2V	CCD vertical register clock-2	
15	P1V	CCD vertical register clock-1	P1V	CCD vertical register clock-1	
16	TG *15	Transfer gate	TG *15	Transfer gate	Same timing as P2V
17	NC		NC		
18	NC		P-	TE-cooler-	
19	NC		P+	TE-cooler+	
20	SS	Substrate (GND)	SS	Substrate (GND)	
21	NC		NC		
22	ISV	Test point (vertical input source)	ISV	Test point (vertical input source)	Shorted to RD
23	IG2V	Test point (vertical input gate-2)	IG2V	Test point (vertical input gate-2)	Shorted to GND
24	IG1V	Test point (vertical input gate-1)	IG1V	Test point (vertical input gate-1)	Shorted to GND

*15: TG is an isolation gate between vertical register and horizontal register. In standard operation, the same pulse as P2V should be applied to TG.

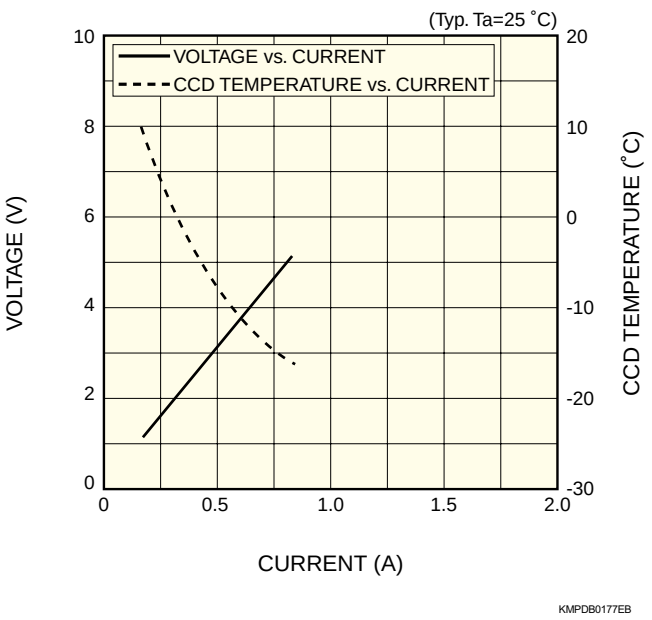
■ Specifications of built-in TE-cooler (Typ.)

Parameter	Symbol	Condition	S9973-1007	S9973-1008	Unit
Internal resistance	Rint	Ta=25 °C	6.0	1.2	Ω
Maximum current *16	Imax	Tc *17=Th *18=25 °C	1.5	3.0	A
Maximum voltage	Vmax	Tc *17=Th *18=25 °C	8.8	3.6	V
Maximum heat absorption *19	Qmax		6.7	5.1	W
Maximum temperature of hot side	-		70		°C

*16: Maximum current Imax:
If the current is greater than Imax, the heat absorption begins to decrease due to the Joule heat. It should be noted that this value is not a damage threshold. To protect the thermoelectric cooler and maintain stable operation, the supply current should be less than 60 % of this maximum current.
*17: Temperature of cool side of thermoelectric cooler
*18: Temperature of hot side of thermoelectric cooler
*19: Maximum heat absorption Qmax
This is a heat absorption when the maximum current is supplied to the TE-cooler.

■ TE-cooler characteristics

S9973-1007



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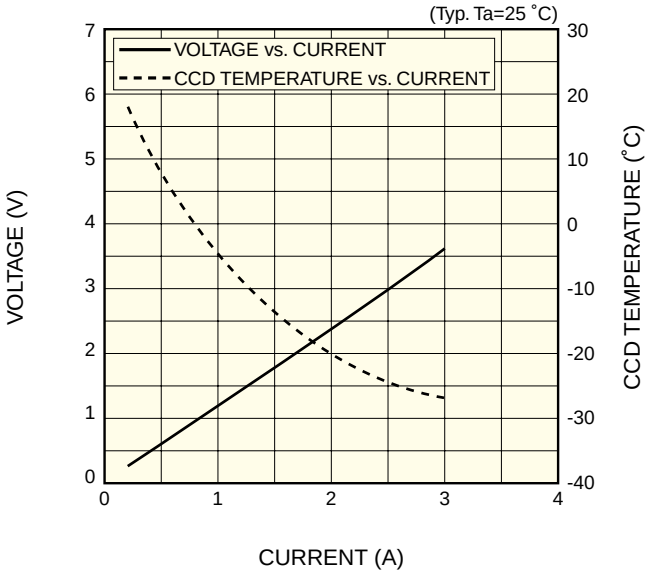
S9973-1008



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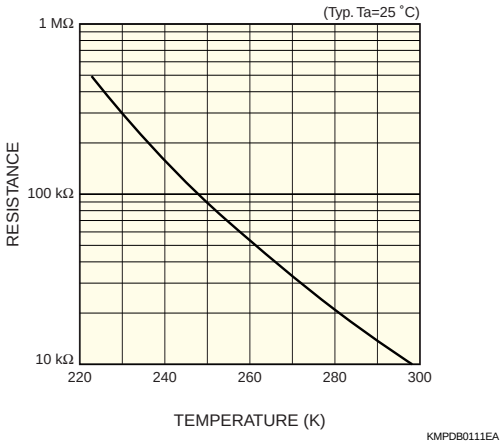
■ Specifications of built-in temperature sensor

A chip thermistor is built in the same package with a CCD chip, and the CCD chip temperature can be monitored with it. A relation between the thermistor resistance and absolute temperature is expressed by the following equation.

R1 = R2 × expB (1 / T1 - 1 / T2)
where R1 is the resistance at absolute temperature T1 (K)
R2 is the resistance at absolute temperature T2 (K)
B is so-called the B constant (K)

The characteristics of the thermistor used are as follows.
R (298K) = 10 kΩ
B (298K / 323K) = 3450 K



■ Precaution for use (Electrostatic countermeasures)

- Handle these sensors with bare hands or wearing cotton gloves. In addition, wear anti-static clothing or use a wrist strap, in order to prevent electrostatic damage due to electrical charges from friction.
- Avoid directly placing these sensors on a work-desk or work-bench that may carry an electrostatic charge.
- Provide ground lines or ground connection with the work-floor, work-desk and work-bench to allow static electricity to discharge.
- Ground the tools used to handle these sensors, such as tweezers and soldering irons.

It is not always necessary to provide all the electrostatic measures stated above. Implement these measures according to the amount of damage that occurs.

■ Element cooling/heating temperature incline rate

When cooling the CCD by an externally attached cooler, set the cooler operation so that the temperature gradient (rate of temperature change) for cooling or allowing the CCD to warm back is less than 5 K/minute.

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