DF6805

8-bit FAST Microcontrollers Family

ver 1.04

OVERVIEW

Document contains brief description of DF6805 core functionality. The DF6805 is a advanced 8-bit MCU IP Core with highly sophisticated, on chip peripheral capabilities. DF6805 soft core is binary-compatible with the industry standard 68HC05 8-bit microcontroller and can achieve a performance **45-100 million instructions** per second. There are two configurations of DF6805: **Harvard** where data and program buses are separated, and **von Neumann** with common program and data bus DF6805 has FAST architecture that is 4.1 times faster compared to original implementation. Core in standard configuration has integrated on chip major peripheral function.

The DF6805 Microcontroller Core contains full-duplex UART (Asynchronous serial communications interface (SCI), and can also be equipped with the Synchronous Serial Peripheral Interface SPI.

The main 16-bit, free-running timer system has implemented two input capture lines and two output-compare lines.

Self-monitoring circuitry is included on-chip to protect against system errors. A computer operating properly (COP) watchdog system protects against software failures. An illegal opcode detection circuit provides a non-maskable interrupt if illegal opcode is detected.

Two software-controlled power-saving modes, WAIT and STOP, are available to conserve additional power. These modes make the DF6805 IP Core especially attractive for automotive and battery-driven applications.

DF6805 is **fully customizable**, which means it is delivered in the exact configuration to meet users requirements. *There is no need to pay extra for not used features and wasted silicon.* It includes **fully automated testbench** with **complete set of tests** allowing easy package validation at each stage of SoC design flow.

CPU FEATURES

- FAST architecture, 4.1 times faster than the original implementation
- Software compatible with industry standard 68HC05
- Configurable Harvard or Von Neumann architectures
- 64 bytes of System Function Registers space (SFRs)
- Up to 64k bytes of Program Memory
- Up to 64k bytes of Data Memory
- De-multiplexed Address/Data Bus to allow easy connection to memory
- Two power saving modes: STOP, WAI
- Ready pin allows Core to operate with slow program and data memories
- Fully synthesizable, static synchronous design with no internal tri-states

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- No internal reset generator or gated clock
- Scan test ready
- Technology independent HDL source code
- Core can be fully customized
- 1 GHz virtual clock frequency compared to original implementation

DESIGN FEATURES

♦ ONE GLOBAL SYSTEM CLOCK

♦ SYNCHRONOUS RESET

♦ ALL ASYNCHRONOUS INPUT SIGNALS ARE SYNCHRONIZED BEFORE INTERNAL USE

✓ DATA MEMORY:

The DF6805 can address up to 64K bytes of Data Memory. The lowest 64 Bytes is reserved for Special Function Registers area. Data Memory can be implemented as synchronous or asynchronous RAM

✓ SYSTEM FUNCTION REGISTERS:

Up to 64 System Function Registers(SFRs) may be implemented in the DF6805 design.

✓ PROGRAM MEMORY:

Up to 64kB of Program Memory may be implemented to the DF6805 design. Program Memory can be implemented as synchronous or asynchronous ROM.

✓ ALL CORE IS DESIGNED AS SYNCHRONOUS LOGIC WITHOUT ANY MICROCODE.

PERIPHERALS

The peripherals listed below are implemented in standard configuration of DF6805.

- DoCD™ on Chip Debugger
  - *Processor execution control*
  - *Read, write all processor contents*
  - *Hardware execution breakpoints*
  - *Three wire communication interface*
- Four 8-bit I/O Ports
- Interrupt Controller
  - *7 interrupt sources*
  - *7 priority levels*
  - *Dedicated Interrupt vector for each interrupt source*
- Main16-bit timer/counter system
  - *16 bit free running counter*
  - *Timer clocked by internal source*
- 16-bit Compare/Capture Unit
  - *Two independent input-capture functions*
  - *Two output-compare channels*
  - *Events capturing*
  - *Pulses generation*
  - *Digital signals generation*
  - *Gated timers*
  - *Sophisticated comparator*
  - *Pulse width modulation*
  - *Pulse width measuring*
- Full-duplex UART - SCI
  - *Standard Nonreturn to Zero format (NRZ)*
  - *8 or 9 bit data transfer*
  - *Integrated baud rate generator*
  - *Noise, Overrun and Framing error detection*
  - *IDLE and BREAK characters generation*
  - *Wake-up block to recognize UART wake-up from IDLE condition*
  - *Three SCI related interrupts*

DELIVERABLES

- ♦ Source code:
  - ◊ VHDL Source Code or/and
  - ◊ VERILOG Source Code or/and
  - ◊ Encrypted, or plain text EDIF
- ♦ VHDL & VERILOG test bench environment
  - ◊ Active-HDL automatic simulation macros
  - ◊ ModelSim automatic simulation macros
  - ◊ Tests with reference responses
- ♦ Technical documentation
  - ◊ Installation notes
  - ◊ HDL core specification
  - ◊ Datasheet
- ♦ Synthesis scripts
- ♦ Example application
- ♦ Technical support
  - ◊ IP Core implementation support
  - ◊ 3 months maintenance
    - Delivery the IP Core updates, minor and major versions changes
    - Delivery the documentation updates
  - ○ *Phone & email support*

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CONFIGURATION

The following parameters of the DF6805 core can be easy adjusted to requirements of dedicated application and technology. Configuration of the core can be prepared by effortless changing appropriate constants in package file. There is no need to change any parts of the code.

- DoCD™ Hardware Debugger
  - used
  - unused
- Architecture type
  - Harvard
  - Von Neumann
- Memories type
  - Synchronous
  - Asynchronou
- Data Memory wait-states
  - used
  - unused
- Power saving STOP mode
  - used
  - unused
- WATCHDOG Timer
  - used
  - unused
- Timer system
  - used
  - unused
- Compare Capture channels
  - used
  - unused
- PORTS A, B, C, D
  - used
  - unused
- SCI – UART Interface
  - used
  - unused
- Support for MUL Instruction
  - used
  - unused

LICENSING

Comprehensible and clearly defined licensing methods without royalty fees make using of IP Core easy and simply.

Single Design license allows use IP Core in single FPGA bitstream and ASIC implementation.

Unlimited Designs, *One Year* licenses allow use IP Core in unlimited number of FPGA bitstreams and ASIC implementations.

In all cases number of IP Core instantiations within a design, and number of manufactured chips are unlimited. There is no time restriction except *One Year* license where time of use is limited to 12 months.

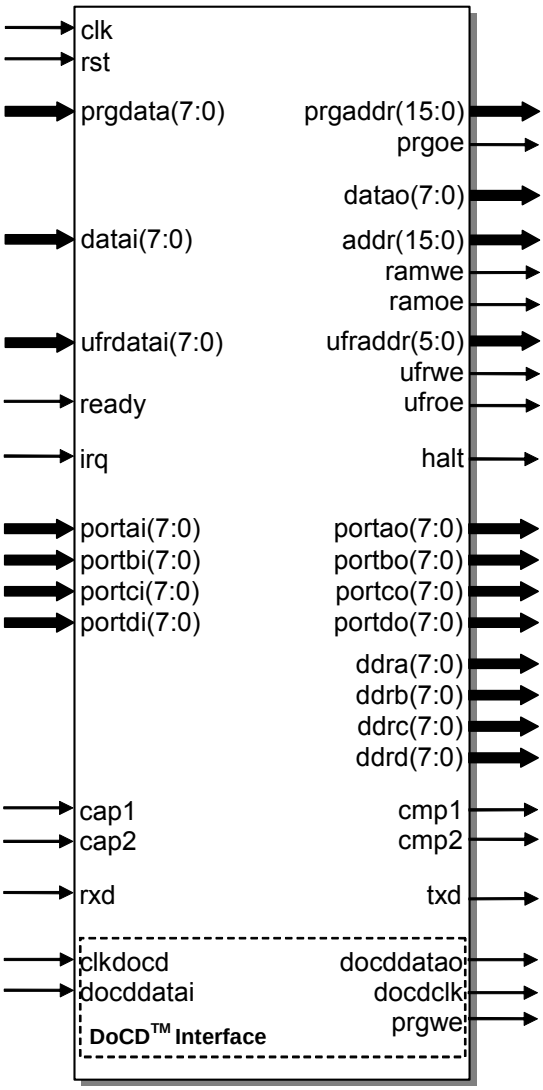
- Single Design license for
  - *VHDL, Verilog source code called HDL Source*
  - *Encrypted, or plain text EDIF called Netlist*
- One Year license for
  - *Encrypted Netlist only*
- Unlimited Designs license for
  - *HDL Source*
  - *Netlist*
- Upgrade from
  - *HDL Source to Netlist*
  - *Single Design to Unlimited Designs*

PINS DESCRIPTION

PIN	ACTIVE	TYPE	DESCRIPTION
clk	-	input	Global system clock
rst	Low	input	Global system reset
prgdata[7:0]	-	input	Program memory bus input
datai[7:0]	-	input	Memory bus input
ufrdatai[7:0]	-	input	UFRs data bus input
ready	Low	input	Code and Data memory Ready
irq	*	input	Interrupt input
portai[7:0]	-	input	Port A input
portbi[7:0]	-	input	Port B input
portci[7:0]	-	input	Port C input
portdi[7:0]	-	input	Port D input
cap1,2	Low	input	Capture inputs
rxd	Low	input	SCI receiver data input
clkdocd	-	input	DoCD™ clock input
docddatai	-	input	DoCD™ serial Data input
prgaddr[15:0]	-	output	Program memory address bus
prgoe	-	output	Program memory output enable
datao[7:0]	-	output	Data memory & UFR bus output
addr[15:0]	-	output	Data memory address bus
ramwe	Low	output	Data memory write enable
ramoe	Low	output	Data memory output enable
ufraddr[5:0]	-	output	UFR's address bus
ufrwe	Low	output	UFRs write enable
ufroe	Low	output	UFRs output enable
halt	High	output	Halt clock system (STOP inst.)
portao[7:0]	-	output	Port A output
portbo[7:0]	-	output	Port B output
portco[7:0]	-	output	Port C output
portdo[7:0]	-	output	Port D output
ddra[7:0]	-	output	Port A data direction control
ddrb[7:0]	-	output	Port B data direction control
ddrc[7:0]	-	output	Port C data direction control
ddrd[7:0]	-	output	Port D data direction control
cmp1,2	*	output	Compare outputs
txd	Low	output	SCI transmitter data output
docddatao	-	output	DoCD™ Serial Data Output
docdclk	-	output	DoCD™ Serial Clock Output
prgwe	-	output	DoCD™ Program Memory Write

** Kind of activity is configurable*

SYMBOL



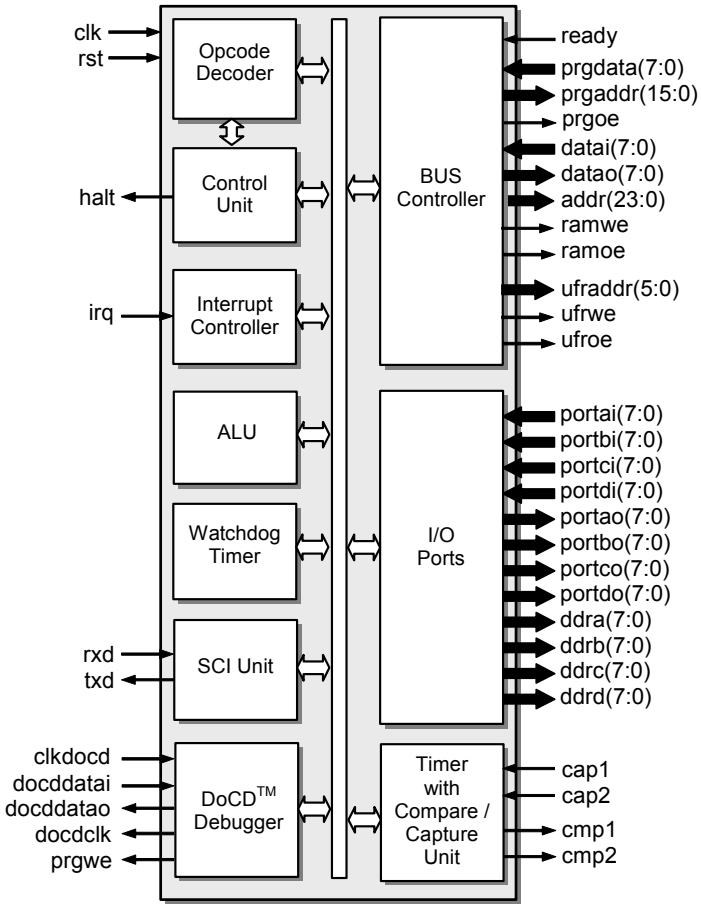
BLOCK DIAGRAM

Control Unit - Performs the core synchronization and data flow control. This module manages execution of all instructions. The Control Unit also manages execution of STOP instruction and wakes-up the processor from the STOP mode.

Opcode Decoder - Performs an instruction opcode decoding and the control functions for all other blocks**.**

ALU - Arithmetic Logic Unit performs the arithmetic and logic operations during execution of an instruction. It contains accumulator (A), Condition Code Register (CCREG), Index registers (X) and related logic like arithmetic unit, logic unit and multiplier.

Bus Controller – Program Memory, Data Memory & SFR's (Special Function Register) interface controls access into the program and data memories and special registers. It contains Program Counter (PC), Stack Pointer (SP) register, and related logic.



Interrupt Controller - DF6805 extended IC has implemented 7-level interrupt priority control. The interrupt requests may come from external pin (IRQ) as well as from particular peripherals. The DF6805 peripheral systems generate maskable interrupts, which are recognized only if the global interrupt mask bit (I) in the CCR is cleared. Maskable interrupts are prioritized according to default arrangement established during reset. When interrupt condition occurs, an interrupt status flag is set to indicate the condition.

I/O Ports - All ports are 8-bit general-purpose bi-directional I/O system. The PORTA, PORTB, PORTC, PORTD data registers have their corresponding data direction registers DDRA, DDRB, DDRC, DDRD to control ports data flow. It assures that all DF6805's ports have full I/O selectable registers. Writes to any ports pins cause data to be stored in the data registers. If any port pins are configured as output then data registers are driven out of those pins. Reads from port pins configured as input causes that input pin is read. If port pins is configured as output, during read data register is read. Writes to any ports pins not configured as outputs do not cause data to be driven out of those pins, but the data is stored in the output registers. Thus, if the pins later become outputs, the last data written to port will be driven out the port pins.

Timer & Compare - The programmable timer is based on free-running 16-bit counter with a fixed divide by four prescaler. plus input capture/output compare circuitry. The timer can be used for many purposes including measuring pulse length of two input signals and generating two output signals. The timer has 16-bit architecture, hence each specific functional segment is represented by two 8-bit registers. These registers contains the high and low byte of that functional block. Accessing the low byte of a specific timer function allows full control of that function, however, an access of the high byte inhibits that specific timer function until the byte is also accessed.
Each of the input-capture channel has its own 16-bit time capture latch (input-capture register) and each of the output-compare channel has its own 16-bit compare register. Additional control bits permit software to control the edge(s) that trigger each input-capture function and the automatic actions that result from output-compare functions. Although hardwired logic is included to automate many timer activities, this timer architecture is essentially a software-oriented system. This structure is easily adaptable to a very wide range of applications although it is not as efficient as dedicated hardware for some specific timing applications.

Watchdog Timer - The Watchdog Timer consist of a free running Timer CLK/2^{13} , plus control logic. The Watchdog Timer can be enabled by software by writing '1' to the WDOG bit in MISC register ($000C). Once enabled the WDT Timer cannot be disabled by software. In addition the WDOG bit acts as a reset mechanism for the WDT Timer. Writing logic one '1' to the WDOG bit clears Watchdog counter and inhibits Watchdog timeout

SCI - The SCI is a full-duplex UART type asynchronous system, using standard non return to zero (NRZ) format : 1 start bit, 8 or 9 data bits and a 1 stop bit. The DF6805 resynchronizes the receiver bit clock on all one to zero transitions in the bit stream. Therefore differences in baud rate between the sending device and the SCI are not as likely to cause reception errors. Three logic samples are taken near the middle of data bit time, and majority logic decides the sense for the bit. For the start and stop bits seven logic samples are taken. Even if noise causes one of these samples to be incorrect, the bit will still be received correctly. The receiver also has the ability to enter a temporary standby mode (called receiver wakeup) to ignore messages intended for a different receiver. Logic automatically wakes up the receiver in time to see the first character of the next message. This wakeup feature greatly reduces CPU overhead in multi-drop SCI networks. The SCI transmitter can produce queued characters of idle (whole characters of all logic 1) and break (whole characters of all logic 0). In addition to the usual transmit data register empty (TDRE) status flag, this SCI also provides a transmit complete (TC) indication that can be used in applications with a modem.

DoCD™ - Debug Unit – it's a real-time hardware debugger provides debugging capability of a whole SoC system. In contrast to other on-chip debuggers DoCD™ provides non-intrusive debugging of running application. It can halt, run, step into or skip an instruction, read/write any contents of microcontroller including all registers, internal, external, program memories, all SFRs including user defined peripherals. Hardware breakpoints can be set and controlled on program memory, internal and external data memories, as well as on SFRs. Hardware breakpoint is executed if any write/read occurred at particular address with certain data pattern or without pattern. The DoCD™ system includes three-wire interface and complete set of tools to communicate and work with core in real time debugging. It is built as scalable unit and some features can be turned off to save silicon and reduce power consumption. A special care on power consumption has been taken, and when debugger is not used it is automatically switched in power save mode. Finally whole debugger is turned off when debug option is no longer used.

OPTIONAL PERIPHERALS

There are also available an optional peripherals, not included in presented DF6805 Microcontroller Core. The optional peripherals, can be implemented in microcontroller core upon customer request.

- SPI – Master and Slave Serial Peripheral Interface
  - *Supports speeds up ¼ of system clock*
    - *Mode fault error*
    - *Write collision error*
  - *Software selectable polarity and phase of serial clock SCK*
  - *System errors detection*
  - *Allows operation from a wide range of system clock frequencies (build-in 5-bit timer)*
  - *Interrupt generation*
- I2C bus controller - Master
  - *7-bit and 10-bit addressing modes*
  - *NORMAL, FAST, HIGH speeds*
  - *Multi-master systems supported*
  - *Clock arbitration and synchronization*
  - *User defined timings on I2C lines*
  - *Wide range of system clock frequencies*
  - *Interrupt generation*
- I2C bus controller - Slave
  - *NORMAL speed 100 kbs*
  - *FAST speed 400 kbs*
  - *HIGH speed 3400 kbs*
  - *Wide range of system clock frequencies*
  - *User defined data setup time on I2C lines*
  - *Interrupt generation*
- PWM – Pulse Width Modulation Timer
- Fixed-Point arithmetic coprocessor
- Floating-Point arithmetic coprocessor IEEE-754 standard single precision
- Floating-Point math coprocessor - IEEE-754 standard single precision real, word and short integers

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PERFORMANCE

The following table gives a survey about the Core area and performance in the ALTERA® devices after Place & Route:

Device	Speed grade	Logic Cells	F_{max}
CYCLONE	-6	1689	79 MHz
STRATIX	-5	1690	83 MHz
MERCURY	-5	1671	85 MHz
APEX II	-7	1850	63 MHz
APEX20KC	-7	1698	55 MHz
APEX20KE	-1	1698	47 MHz
ACEX1K	-1	1739	41 MHz
FLEX10KE	-1	1739	41 MHz

Core performance in ALTERA® devices

Area utilized by the each unit of DF6805 core in vendor specific technologies is summarized in table below.

Component	Area	
	[LC]	[FFs]
CPU*	1134	153
Main Timer	110	55
COM/CAP	150	60
Watchdog	29	14
UART - SCI	272	124
I/O Ports	161	64
Total area	1856	470

*CPU – consisted of ALU, Control Unit and Instruction Decoder, Bus Controller with support for 64KB RAM, External IRQ pin Interrupt Controller

Core components area utilization

IMPROVEMENT

For user the most important is application speed improvement. The most commonly used arithmetic functions and theirs improvement are shown in table below. Improvement was computed as {M68HC04 clock periods} divided by {DF6805 clock periods} required to execute an identical function. More details are available in core documentation

Function	Improvement
8-bit addition (*immediate data*)	**4**
8-bit addition (*direct addressing*)	**4**
8-bit addition (*indirect addressing*)	**3,6**
8-bit subtraction (*immediate data*)	**4**
8-bit subtraction (*direct addressing*)	**4**
8-bit subtraction (*indirect addressing*)	**3,6**
16-bit addition (*immediate data*)	**4**
16-bit addition (*direct addressing*)	**4**
16-bit addition (*indirect addressing*	**3,6**
16-bit subtraction (*immediate data*)	**4**
16-bit subtraction (*direct addressing*)	**4**
16-bit subtraction (*indirect addressing*	**3,6**
Multiplication	**5**
Division	**5**

DF68XX FAMILY OVERVIEW

The main features of each DF68XX family member have been summarized in table below. It gives a briefly member characterization helping user to select the most suitable IP Core for its application. User can specify its own peripheral set (including listed below and the others) and requests the core modifications.

Design	Physical Linear memory space	Paged Data Memory space	Motorola Memory Expansion Logic	Interrupt sources	Interrupt levels	Real Time Interrupt	Data Pointers	READY for Pro. and Data mem.	Compare\Capture	Main Timer System	SCI (UART)	I\O Ports	SPI M/S Interface	Watchdog Timer	Pulse accumulator	Interface for additional SFRs	DoCD Debugger	Size – ASIC gates
DF6805	64k	64k	-	7	7	-	-	*	2/2*	1*	✓*	4	+	✓*	-	✓	✓	6 700
DF6808	64k	64k	-	7	7	-	-	*	22*	1*	✓*	4	✓	✓*	-	✓	✓	8 900
DF6811	64k	16M	-	20	17	✓	1*	*	5/3*	1*	✓*	4	✓*	✓*	✓*	✓	✓	12 000
DF6811CPU	64k	16M	-	3	3	+	1*	*	+	+	+	+	+	+	+	✓	✓	6 500

DF68XX family of High Performance Microcontroller Cores

\+ optional

* configurable

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