



Product List

SM8051L25, 25 MHz 4KB internal ROM MCU
SM8052L25, 25 MHz 8KB internal ROM MCU
SM8051C25, 25 MHz 4KB internal ROM MCU
SM8052C25, 25 MHz 8KB internal ROM MCU
SM8051C40, 40 MHz 4KB internal ROM MCU
SM8052C40, 40 MHz 8KB internal ROM MCU

Description

The SM8051/8052 series product is an 8 - bit single chip micro controller with 4/8 KB ROM embedded. It provides hardware features and a powerful instruction set, necessary to make it a versatile and cost effective controller for those applications demand up to 32 I/O pins or need up to 4/8 KB ROM memory either for program or for data or mixed.

Ordering Information

yywww
SM8051/8052ihhk

yy: year, ww:month
v: version identifier { , A, B, ...}
i: process identifier {L=3.0V ~ 3.6V, C=4.5V ~ 5.5V}
hh: working clock in MHz {25, 40}
k: package type postfix {as below table}

Features

- Working voltage: 3.0V ~ 3.6V For L Version
4.5V ~ 5.5V For C Version
- General 8051/8052 family compatible
- 12 clocks per machine cycle
- 4/8 KB internal ROM memory
- 128/256 bytes data RAM
- 2/3 16 bit timers/counters
- Four 8-bit I/O ports
- Full duplex serial channel
- Bit operation instruction
- Page free jumps
- 8-bit unsigned division
- 8-bit unsigned multiply
- BCD arithmetic
- Direct addressing
- Indirect addressing
- Nested interrupt
- Two priority level interrupt
- A serial I/O port
- Power save modes:
Idle mode and power down mode
- Code protection function
- One watch dog timer (WDT)
- Low EMI (inhibit ALE)

Postfix	Package	Pin/Pad Configuration	Dimension
P	40L PDIP	page 2	page 13
J	44L PLCC	page 2	page 14
Q	44L QFP/TQFP	page 2	page 15/16

Taiwan
4F, No. 1 Creation Road 1,
Science-based Industrial Park,
Hsinchu, Taiwan 30077

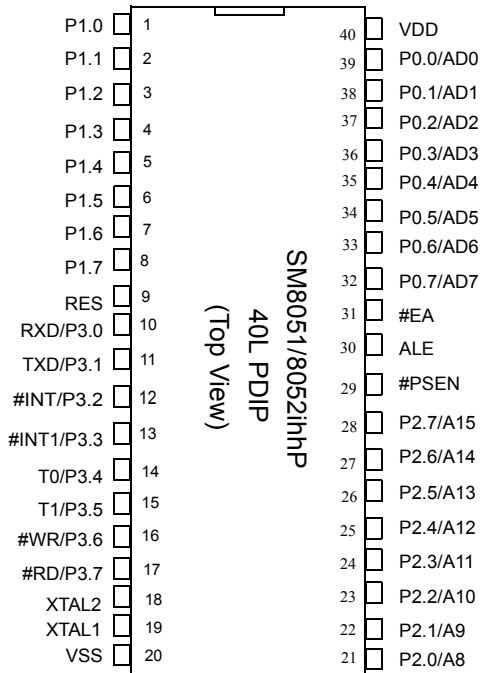
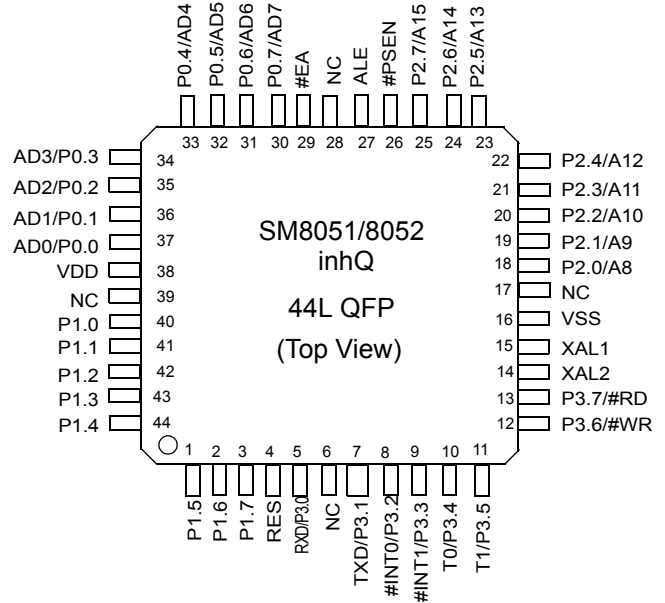
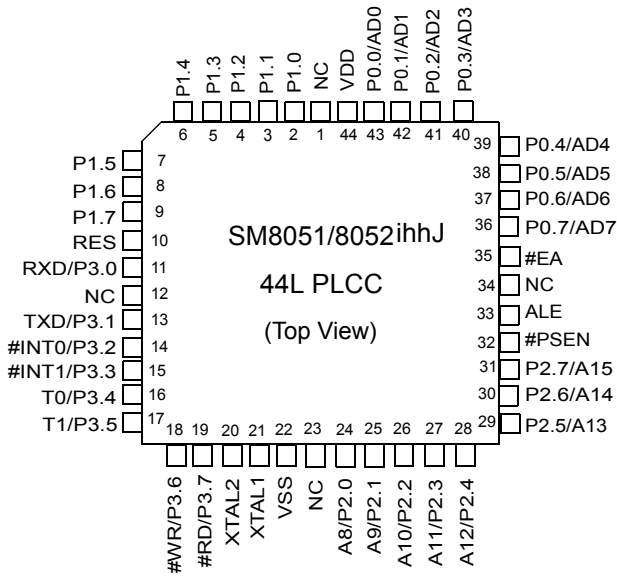
TEL: 886-3-579-2926
886-3-579-2988
FAX: 886-3-579-2960
886-3-578-0493

Specifications subject to change without notice,contact your sales representatives for the most recent information.



May 2001

Pin Configurations

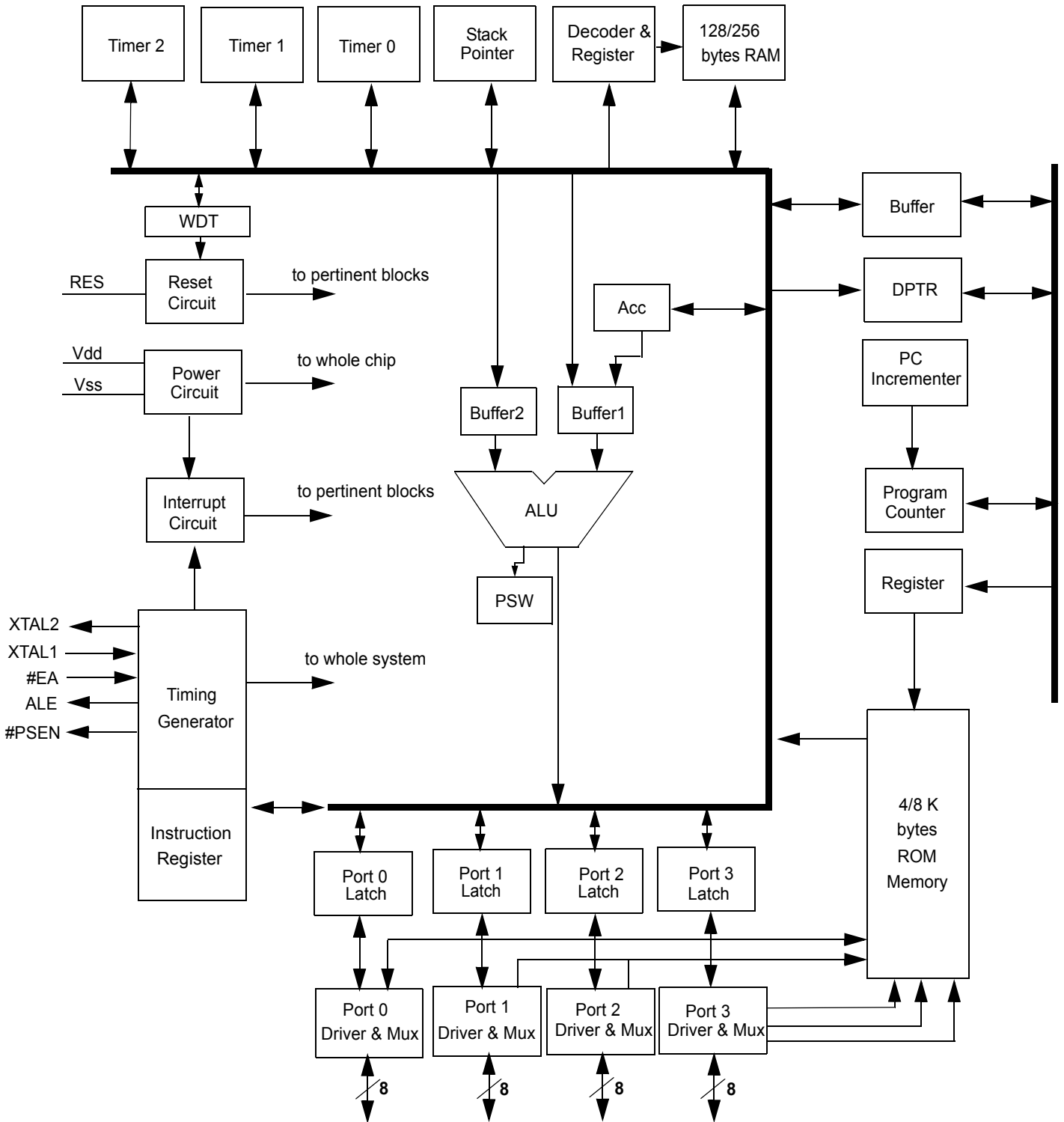


Specifications subject to change without notice, contact your sales representatives for the most recent information.



May 2001

Block Diagram



Specifications subject to change without notice, contact your sales representatives for the most recent information.



May 2001

Pin Descriptions

40L PDIP Pin#	44L QFP Pin#	44L PLCC Pin#	Symbol	Active	I/O	Names
1	40	2	P1.0		i/o	bit 0 of port 1
2	41	3	P1.1		i/o	bit 1 of port 1
3	42	4	P1.2		i/o	bit 2 of port 1
4	43	5	P1.3		i/o	bit 3 of port 1
5	44	6	P1.4		i/o	bit 4 of port 1
6	1	7	P1.5		i/o	bit 5 of port 1
7	2	8	P1.6		i/o	bit 6 of port 1
8	3	9	P1.7		i/o	bit 7 of port 1
9	4	10	RES	H	i	Reset
10	5	11	RXD/P3.0		i/o	Receive data & bit 0 of port 3
11	7	13	TXD/P3.1		i/o	Transmit data & bit 1 of port 3
12	8	14	#INT0/P3.2	L/ -	i/o	low true interrupt 0 & bit 2 of port 3
13	9	15	#INT1/P3.3	L/ -	i/o	low true interrupt 1 & bit 3 of port 3
14	10	16	T0/P3.4		i/o	Timer 0 & bit 4 of port 3
15	11	17	T1/P3.5		i/o	Timer 1 & bit 5 of port 3
16	12	18	#WR/P3.6	L/ -	i/o	external memory write & bit 6 of port 3
17	13	19	#RD/P3.7	L/ -	i/o	external memory read & bit 7 of port 3
18	14	20	XTAL2		o	Crystal out
19	15	21	XTAL1		i	Crystal in
20	16	22	VSS			Sink Voltage, Ground
21	18	24	P2.0/A8		i/o	bit 0 of port 2 & bit 8 of external memory address
22	19	25	P2.1/A9		i/o	bit 1 of port 2 & bit 9 of external memory address
23	20	26	P2.2/A10		i/o	bit 2 of port 2 & bit 10 of external memory address
24	21	27	P2.3/A11		i/o	bit 3 of port 2 & bit 11 of external memory address
25	22	28	P2.4/A12		i/o	bit 4 of port 2 & bit 12 of external memory address
26	23	29	P2.5/A13		i/o	bit 5 of port 2 & bit 13 of external memory address
27	24	30	P2.6/A14		i/o	bit 6 of port 2 & bit 14 of external memory address
28	25	31	P2.7/A15		i/o	bit 7 of port 2 & bit 15 of external memory address
29	26	32	#PSEN	L	o	program storage enable
30	27	33	ALE	-	o	address latch enable
31	29	35	#EA	L	i	external access
32	30	36	P0.7/AD7		i/o	bit 7 of port 0 & data/address bit 7 of external memory
33	31	37	P0.6/AD6		i/o	bit 6 of port 0 & data/address bit 6 of external memory
34	32	38	P0.5/AD5		i/o	bit 5 of port 0 & data/address bit 5 of external memory
35	33	39	P0.4/AD4		i/o	bit 4 of port 0 & data/address bit 4 of external memory
36	34	40	P0.3/AD3		i/o	bit 3 of port 0 & data/address bit 3 of external memory
37	35	41	P0.2/AD2		i/o	bit 2 of port 0 & data/address bit 2 of external memory
38	36	42	P0.1/AD1		i/o	bit 1 of port 0 & data/address bit 1 of external memory
39	37	43	P0.0/AD0		i/o	bit 0 of port 0 & data/address bit 0 of external memory
40	38	44	VDD			Drive Voltage, +5 Vcc

Specifications subject to change without notice, contact your sales representatives for the most recent information.



SFR Memory MAP

\$F8								\$FF
\$F0	B							\$F7
\$E8								\$EF
\$E0	ACC							\$E7
\$D8								\$DF
\$D0	PSW							\$D7
\$C8	T2CON		RC2L	RC2H	TL2	TH2		\$CF
\$C0								\$C7
\$B8	IP						SCONF	\$BF
\$B0	P3							\$B7
\$A8	IE							\$AF
\$A0	P2							\$A7
\$98	SCON	SBUF					WDTC	\$9F
\$90	P1							\$97
\$88	TCON	TMOD	TL0	TL1	TH0	TH1		\$8F
\$80	P0	SP	DPL	DPH	(Reserved)		PCON	\$87

Note: The text of SFRs with bold type characters are Extension Special Function Registers for SM8051/8052

Extension Function Description

Watch Dog Timer

The Watch Dog Timer (WDT) is a 16-bit free-running counter that generate reset signal if the counter overflows. The WDT is useful for systems which are susceptible to noise, power glitches, or electronics discharge which causing software dead loop or runaway. The WDT function can help user software recover form abnormal software condition. The WDT is different from Timer0, Timer1 and Timer2 of general 8052. To prevent a WDT reset can be done by software periodically clearing the WDT counter.

The SM8051/8052 WDT has selectable divider input for the time base source clock. To select the divider input, the setting of bit2~bit0 (PS2~PS0) OF Watch Dog Timer Control Register (WDTC) should be set accordingly.

To enable the WDT is done by setting 1 to the bit 7 (WDTE) of WDTC. After WDTE set to 1, the 16-bit counter starts to count with the selected time base source clock which set by PS2~PS0. It will generate a reset signal when overflows. The WDTE bit will be cleared to 0 automatically when SM8051/8052 been reset, either hardware reset or WDT reset.

To reset the WDT is done by setting 1 to the bit 5 (CLEAR) of WDTC. This will clear the content of the 16-bit counter and let the counter re-start to count from the beginning.



Watch Dog Timer Registers - WDT Control Register (WDTC, \$9F)

Reset value	WDTE	Unused	CLEAR	Unused	Unused	PS2	PS1	PS0
	0	*	0	*	*	0	0	0
	MSB				LSB			

WDTE : Watch Dog Timer enable bit

CLEAR : Watch Dog Timer reset bit

PS2 ~ PS0 : clock source divider bit

PS [2:0]	Divider (OSC in)	Time Period (ms) @40MHZ
000	8	13.1
001	16	26.21
010	32	52.42
011	64	104.8
100	128	209.71
101	256	419.43
110	512	838.86
111	1024	1677.72

Watch Dog Timer Register - System Control Register (SCONF, \$BF)

Reset value	WDR	Unused	Unused	Unused	Unused	Unused	Unused	ALEI
	0	*	*	*	*	*	*	0
	MSB				LSB			

WDR : Watch Dog Timer Reset. When system reset by Watch Dog Timer overflow, WDR will be set to 1
ALEI : ALE output inhibit bit, to reduce EMI

The bit 7(WDR) of SCONF is Watch Dog Timer Reset bit. It will be set to 1 when reset signal generated by WDT overflow. User should check WDR bit whenever un-predicted reset happened.

Reduce EMI Function

The SM8051/8052 allows user to reduce the EMI emission by setting 1 to the bit 0 (ALEI) of SCONF register. This function will inhibit the clock signal in Fosc/6Hz output to the ALE pin. This function is available when there is no external program memory or no external data RAM in the system.



Operating Conditions

Symbol	Description	Min.	Typ.	Max.	Unit.	Remarks
TA	Operating temperature	0	25	70	°C	Ambient temperature under bias
TS	Storage temperature	-55	25	155	°C	
VCC5	Supply voltage	4.5	5.0	5.5	V	For C Version
VCC3	Supply voltage	3	3.3	3.6	V	For L Version
Fosc 25	Oscillator Frequency	3.0	25	25	MHz	For 5V, 3.3V application
Fosc 40	Oscillator Frequency	3.0	40	40	MHz	For 5V application

DC Characteristics

(12MHz, typical operating conditions, valid for SM8051/8052 series)

Symbol	Parameter	Valid	Min.	Max.	Unit	Test Conditions
VIL1	Input Low Voltage	port 0,1,2,3,4,#EA	-0.5	0.8	V	
VIL2	Input Low Voltage	RES, XTAL1	0	0.8	V	
VIH1	Input High Voltage	port 0,1,2,3,4,#EA	2.0	V _{cc} +0.5	V	
VIH2	Input High Voltage	RES, XTAL1	70%V _{cc}	V _{cc} +0.5	V	
VOL1	Output Low Voltage	port 0, ALE, #PSEN		0.45	V	IOL=8mA (5V) / IOL=6mA (3.3V)
VOL2	Output Low Voltage	port 1,2,3,4		0.45	V	IOL=6.5mA (5V) / IOL=6mA (3.3V)
VOH1	Output High Voltage	port 0	2.4		V	IOH=-800uA (only for VCC=5V)
			90%V _{cc}		V	IOH=-80uA
VOH2	Output High Voltage	port 1,2,3,4,ALE,#PSEN	2.4		V	IOH=-60uA (only for VCC=5V)
			90%V _{cc}		V	IOH=-10uA
IIL	Logical 0 Input Current	port 1,2,3,4		-75	uA	Vin=0.45V
ITL	Logical Transition Current	port 1,2,3,4		-650	uA	Vin=2.0V
ILI	Input Leakage Current	port 0, #EA		± 10	uA	0.45V<Vin<Vcc
R RES	Reset Pulldown Resistance	RES	50	300	Kohm	
C IO	Pin Capacitance			10	pF	Freq=1MHz, Ta=25°C
I CC	Power Supply Current	Vdd		7	mA	Active mode, 16MHz
				4.5	mA	Idle mode, 16MHz
				10	uA	Power down mode

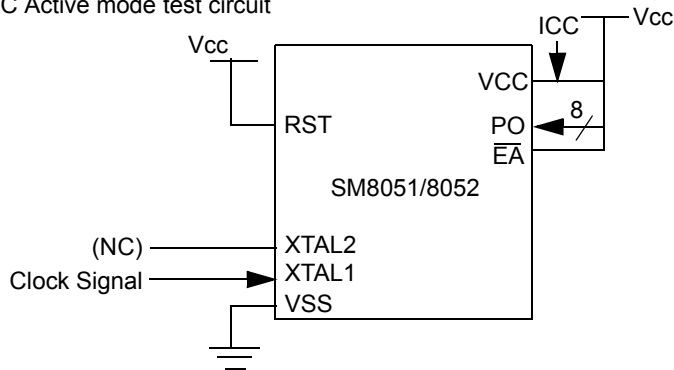


AC Characteristics

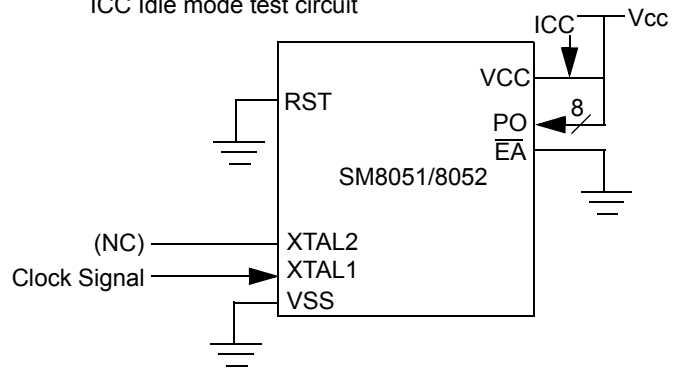
(25/40MHz, operating conditions; CL for Port 0, ALE and PSEN Outputs=100pF; CL for all Other Output=80pF)

Symbol	Parameter	Valid Cycle	fosc=16MHz			Variable fosc			Unit	Remarks
			Min.	Typ.	Max	Min.	Typ.	Max		
T LHLL	ALE pulse width	RD/WRT	115			2xT - 10			nS	
T AVLL	Address Valid to ALE low	RD/WRT	43			T - 20			nS	
T LLAX	Address Hold after ALE low	RD/WRT	53			T - 10			nS	
T LLIV	ALE low to Valid Instruction In	RD			240			4xT - 10	nS	
T LLPL	ALE low to #PSEN low	RD	53			T - 10			nS	
T PLPH	#PSEN pulse width	RD	173			3xT - 15			nS	
T PLIV	#PSEN low to Valid Instruction In	RD			177			3xT - 10	nS	
T PXIX	Instruction Hold after #PSEN	RD	0			0			nS	
T PXIZ	Instruction Float after #PSEN	RD			87			T + 25	nS	
T AVIV	Address to Valid Instruction In	RD			292			5xT - 20	nS	
T PLAZ	#PSEN low to Address Float	RD			10			10	nS	
T RLRH	#RD pulse width	RD	365			6xT - 10			nS	
T WLWH	#WR pulse width	WRT	365			6xT - 10			nS	
T RLDV	#RD low to Valid Data In	RD			302			5xT - 10	nS	
T RHDX	Data Hold after #RD	RD	0			0			nS	
T RHDZ	Data Float after #RD	RD			145			2xT + 20	nS	
T LLDV	ALE low to Valid Data In	RD			590			8xT - 10	nS	
T AVDV	Address to Valid Data In	RD			542			9xT - 20	nS	
T LLYL	ALE low to #WR High or #RD low	RD/WRT	178		197	3xT - 10		3xT + 10	nS	
T AVYL	Address Valid to #WR or #RD low	RD/WRT	230			4xT - 20			nS	
T QVWH	Data Valid to #WR High	WRT	403			7xT - 35			nS	
T QVWX	Data Valid to #WR transition	WRT	38			T - 25			nS	
T WHQX	Data hold after #WR	WRT	73			T + 10			nS	
T RLAZ	#RD low to Address Float	RD						5	nS	
T YALH	#WR or #RD high to ALE high	RD/WRT	53		72	T - 10		T + 10	nS	
T CHCL	clock fall time								nS	
T CLCX	clock low time								nS	
T CLCH	clock rise time								nS	
T CHCX	clock high time								nS	
T, TCLCL	clock period			63			1/fosc		nS	

ICC Active mode test circuit



ICC Idle mode test circuit

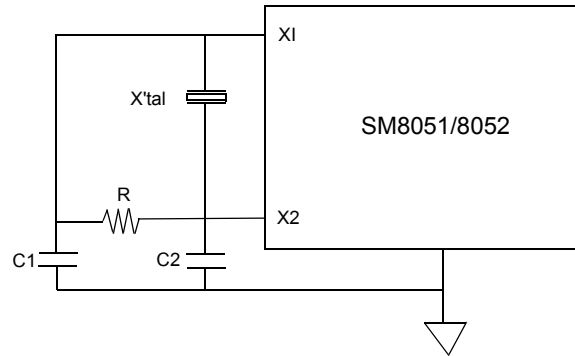


Specifications subject to change without notice, contact your sales representatives for the most recent information.



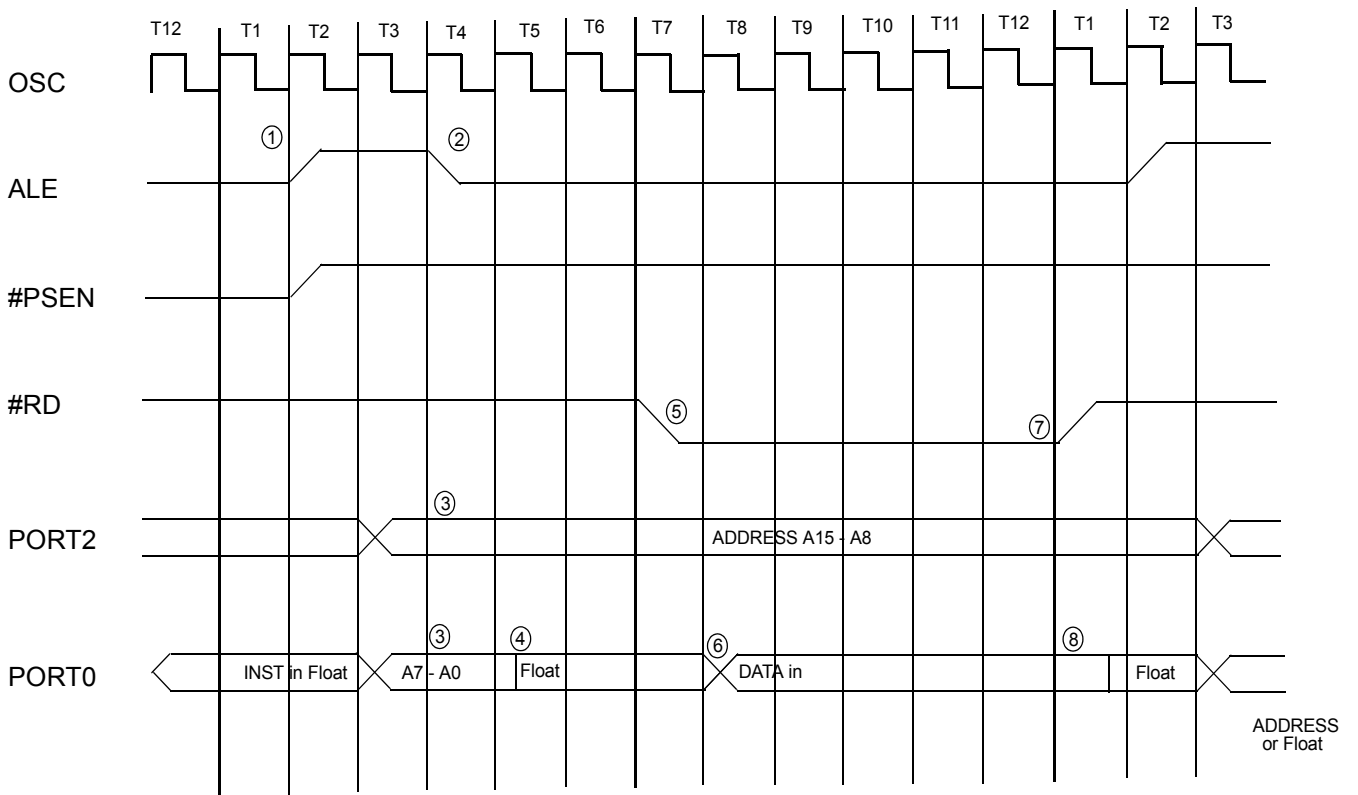
Application Reference

Valid for SM8051/8052				
X'tal	3MHz	6MHz	9MHz	12MHz
C1	30 pF	30 pF	30 pF	30 pF
C2	30 pF	30 pF	30 pF	30 pF
R	open	open	open	open
X'tal	16MHz	25MHz	33MHz	40MHz
C1	30 pF	15 pF	10 pF	5 pF
C2	30 pF	15 pF	10 pF	5 pF
R	open	62KΩ	6.8KΩ	4.7KΩ



NOTE: Oscillation circuit may differs with different crystal or ceramic resonator in higher oscillation frequency which was due to each crystal or ceramic resonator has its own characteristics. User should check with the crystal or ceramic resonator manufacturer for appropriate value of external components.

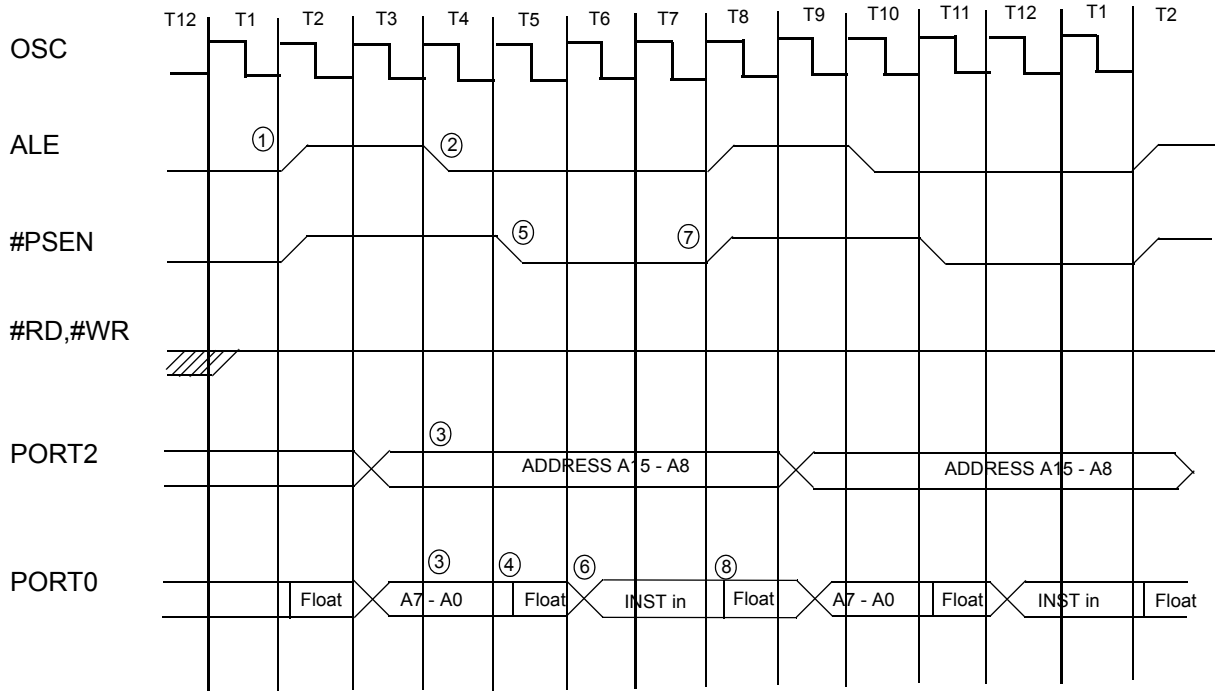
Data Memory Read Cycle Timing



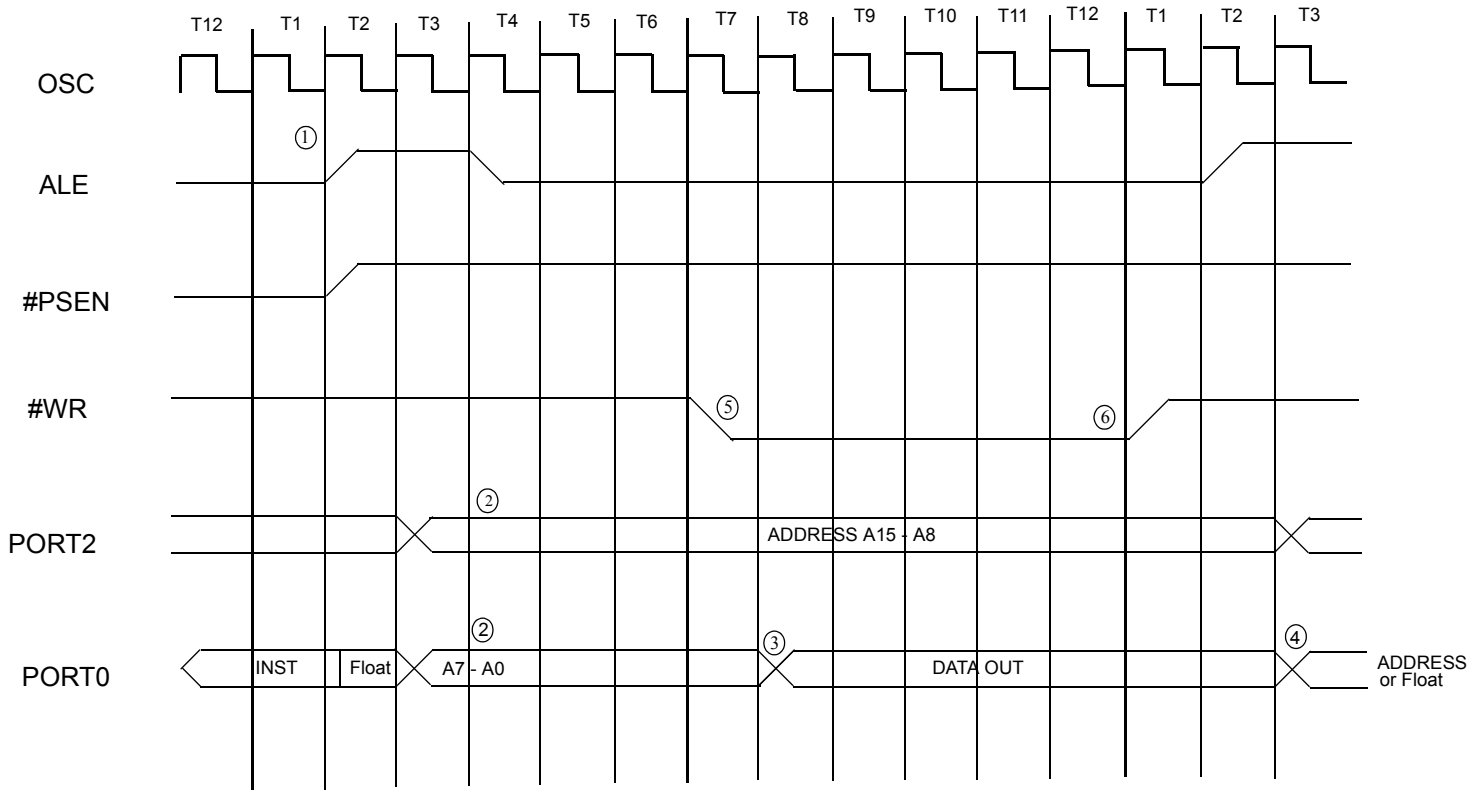
Specifications subject to change without notice, contact your sales representatives for the most recent information.



Program Memory Read Cycle Timing



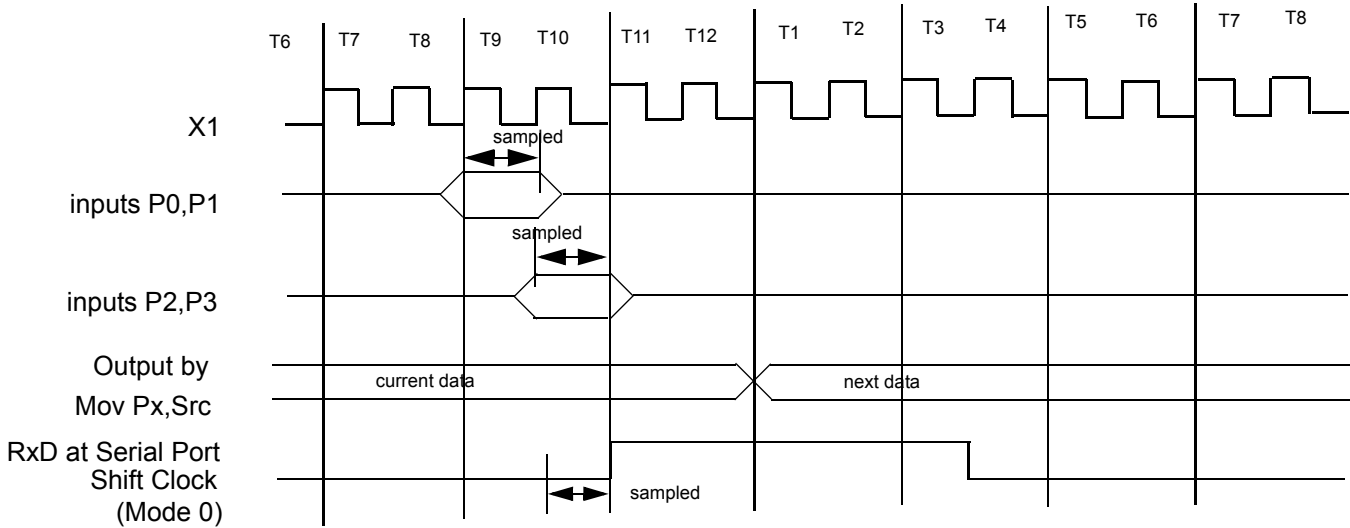
Data Memory Write Cycle Timing



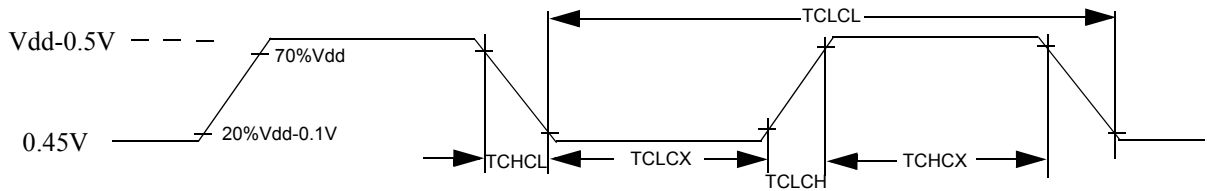
Specifications subject to change without notice, contact your sales representatives for the most recent information.



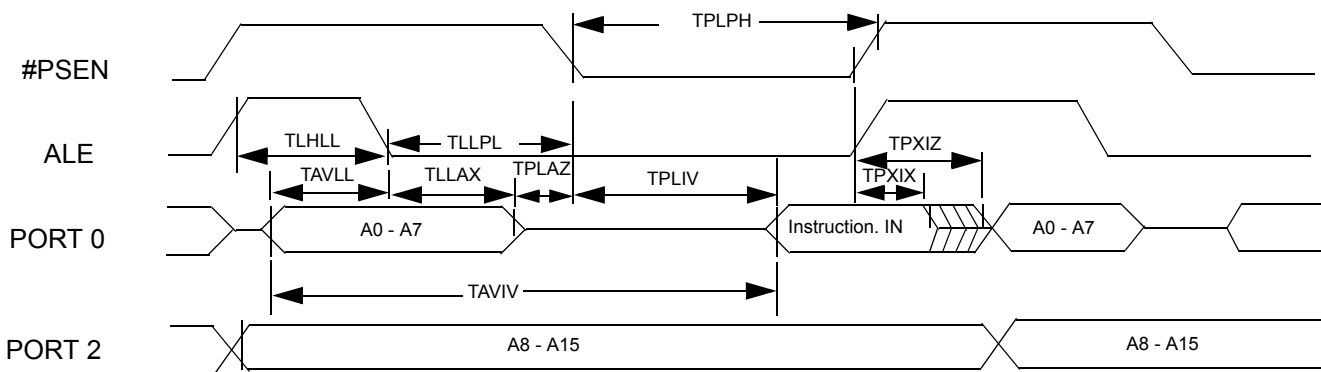
I/O Ports Timing



Timing Critical, Requirement of External Clock (Vss=0.0V is assumed)

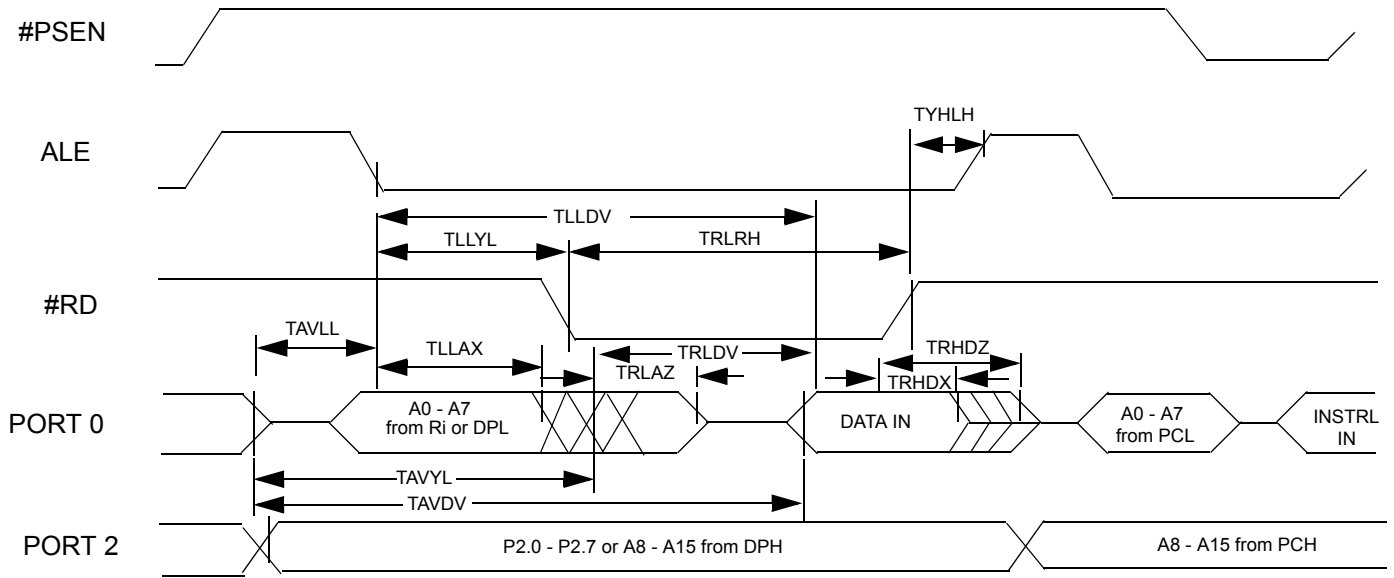


Tm.1 External Program Memory Read Cycle

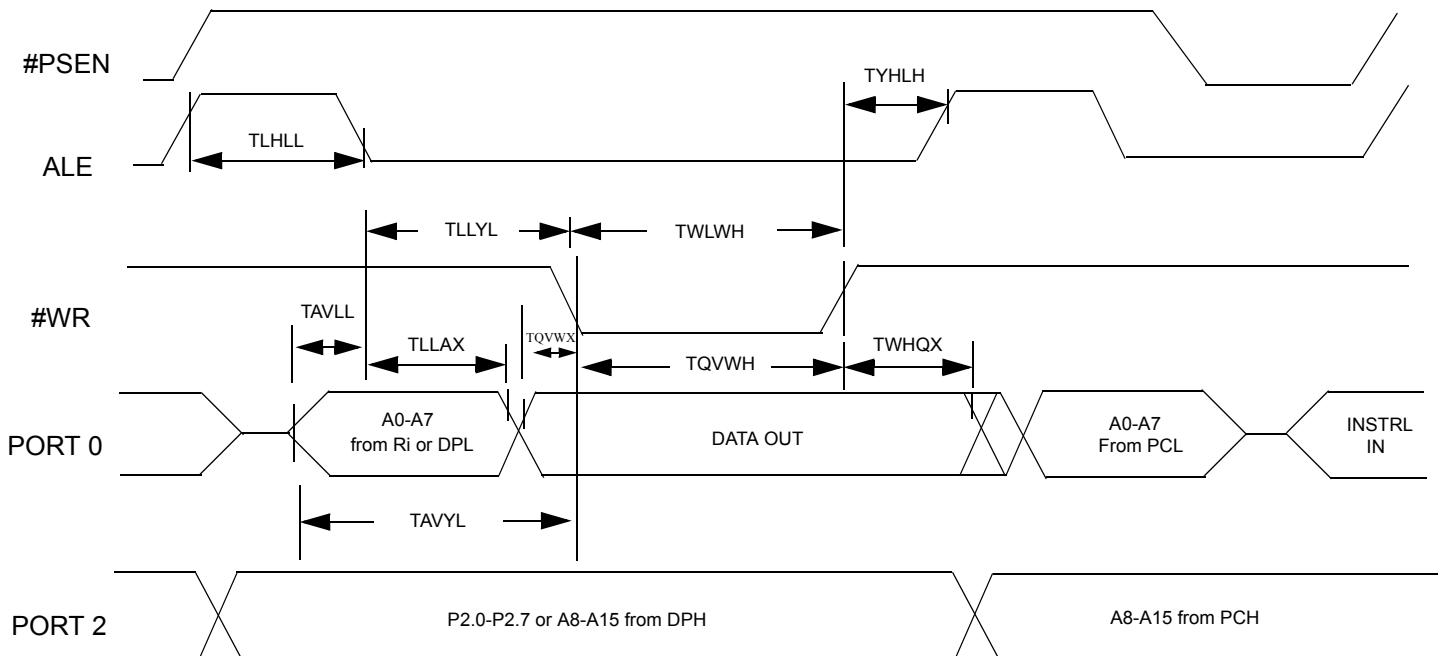




Tm.II External Data Memory Read Cycle



Tm.III External Data Memory Write Cycle

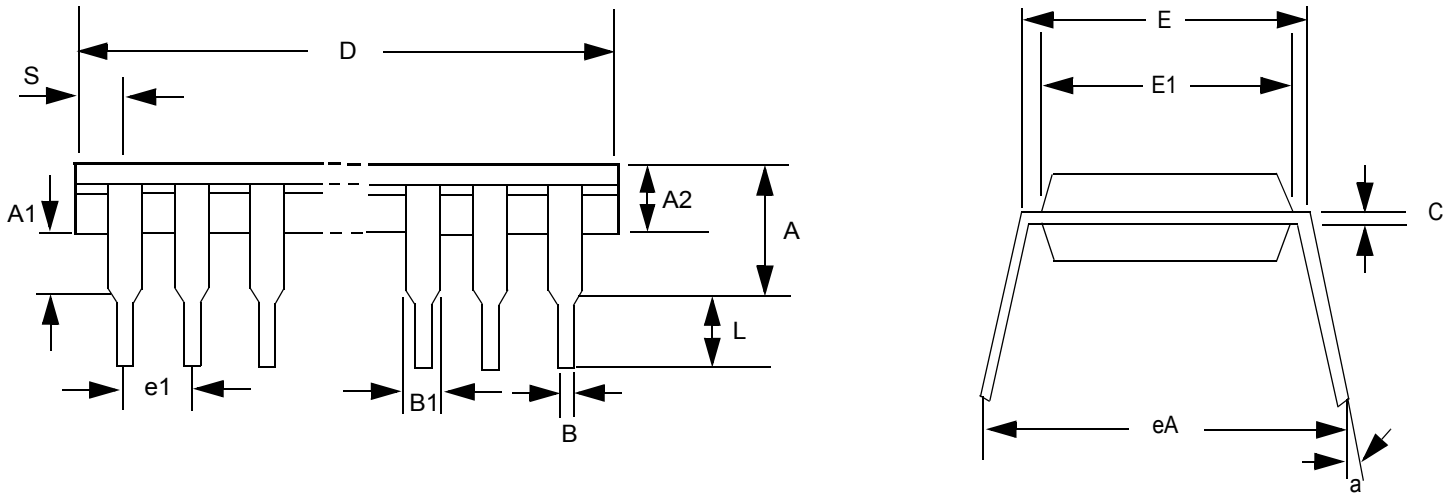


Specifications subject to change without notice, contact your sales representatives for the most recent information.



May 2001

40L 600mil PDIP Information



Note:

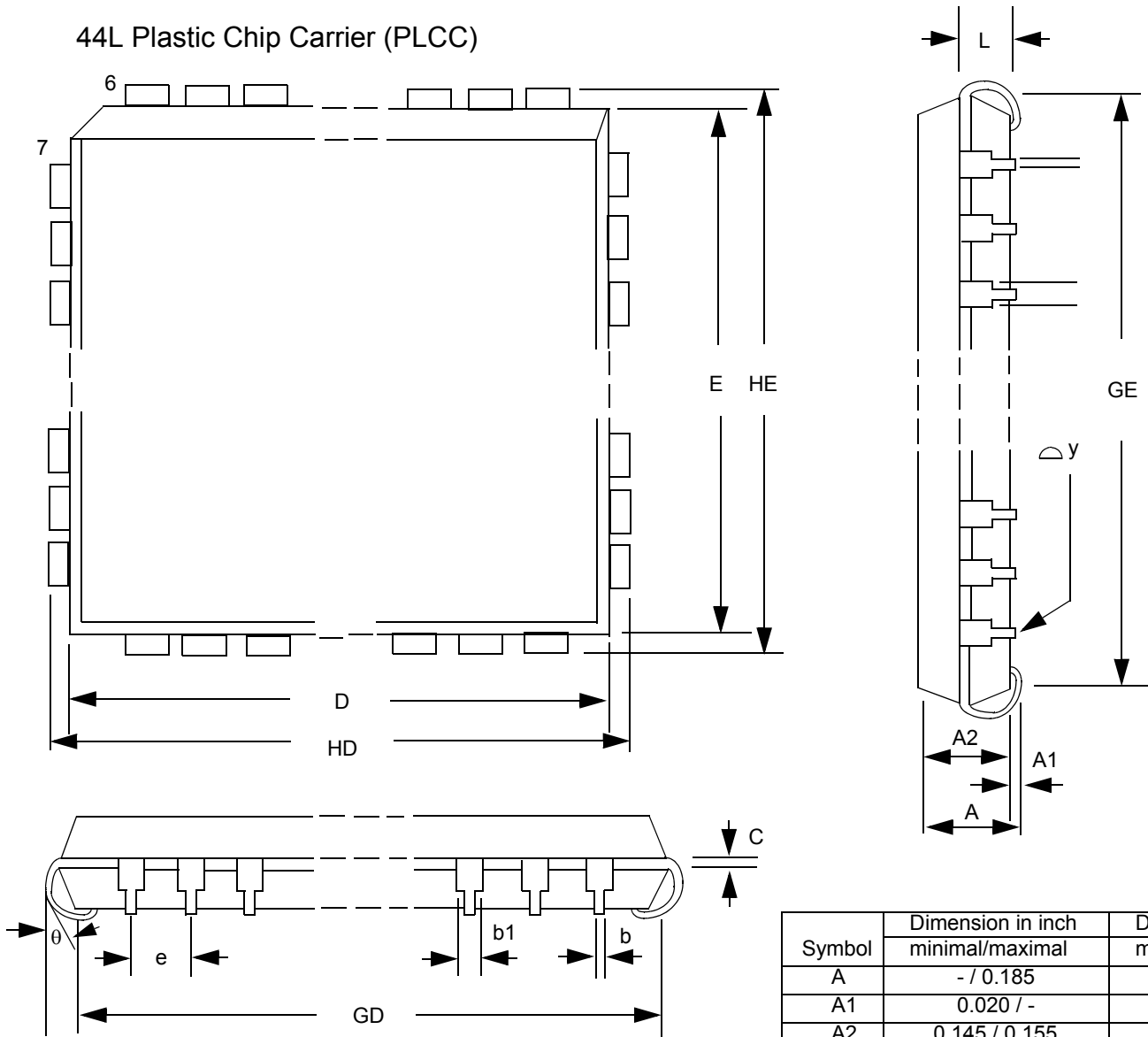
1. Dimension D Max & include mold flash or tie bar burrs.
2. Dimension E1 does not include inter lead flash.
3. Dimension D & E1 include mold mismatch and are determined at the mold parting line.
4. Dimension B1 does not include dam bar protrusion/infusion.
5. Controlling dimension is inch.
6. General appearance spec. should base on final visual inspection spec.

Symbol	Dimension in inch	Dimension in mm
	minimal/maximal	minimal/maximal
A	- / 0.210	- / 5.33
A1	0.010 / -	0.25 / -
A2	0.150 / 0.160	3.81 / 4.06
B	0.016 / 0.022	0.41 / 0.56
B1	0.048 / 0.054	1.22 / 1.37
C	0.008 / 0.014	0.20 / 0.36
D	- / 2.070	- / 52.58
E	0.590 / 0.610	14.99 / 15.49
E1	0.540 / 0.552	13.72 / 14.02
e1	0.090 / 0.110	2.29 / 2.79
L	0.120 / 0.140	3.05 / 3.56
a	0° / 15°	0° / 15°
eA	0.630 / 0.670	16.00 / 17.02
S	- / 0.090	- / 2.29



May 2001

44L Plastic Chip Carrier (PLCC)



Note:

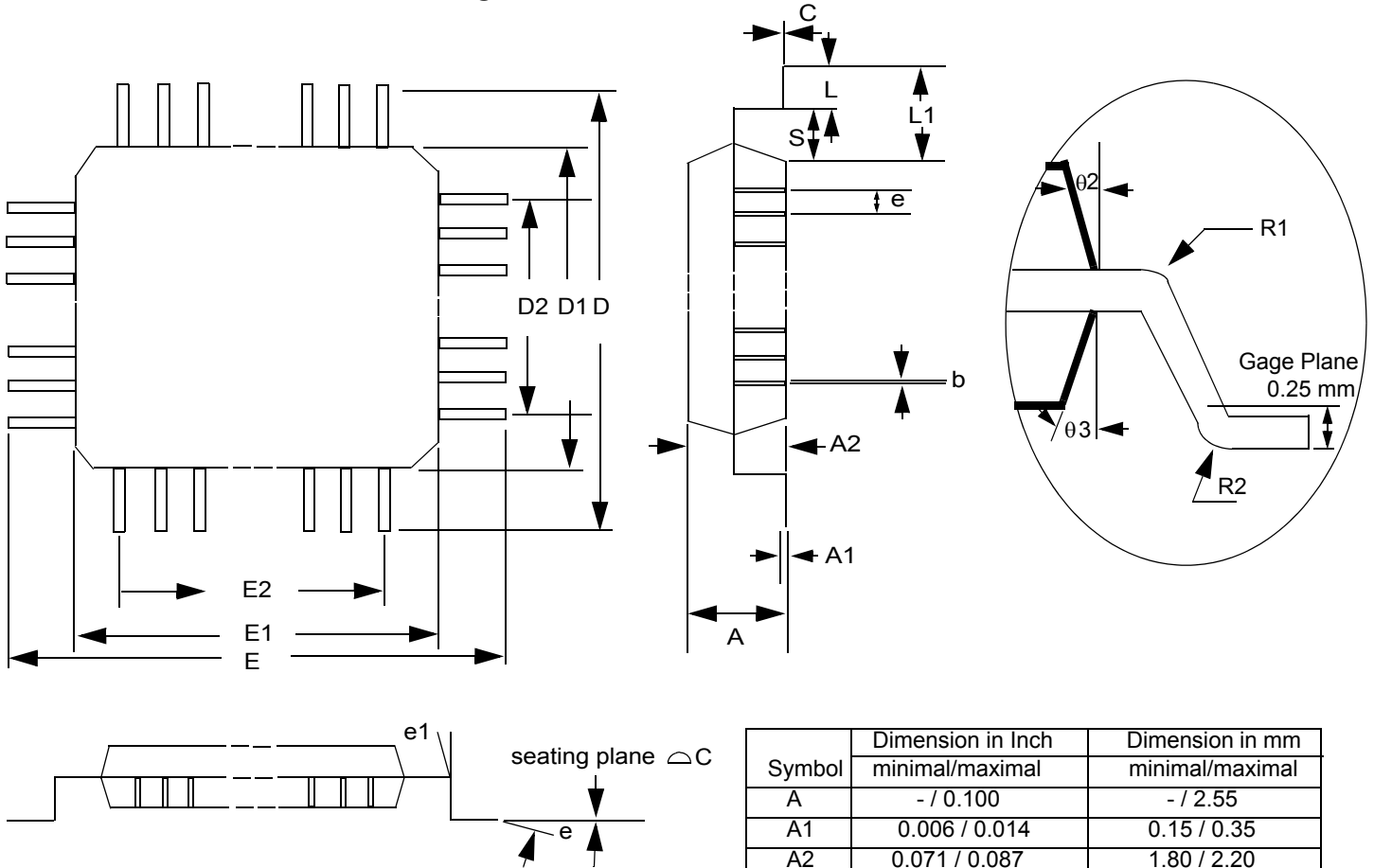
1. Dimension D & E does not include inter lead flash.
2. Dimension b1 does not include dam bar protrusion/ intrusion.
3. Controlling dimension: Inch
4. General appearance spec. should base on final visual inspection spec.

Symbol	Dimension in inch minimal/maximal	Dimension in mm minimal/maximal
A	- / 0.185	- / 4.70
A1	0.020 / -	0.51 / -
A2	0.145 / 0.155	3.68 / 3.94
b1	0.026 / 0.032	0.66 / 0.81
b	0.016 / 0.022	0.41 / 0.56
C	0.008 / 0.014	0.20 / 0.36
D	0.648 / 0.658	16.46 / 16.71
E	0.648 / 0.658	16.46 / 16.71
e	0.050 BSC	1.27 BSC
GD	0.590 / 0.630	14.99 / 16.00
GE	0.590 / 0.630	14.99 / 16.00
HD	0.680 / 0.700	17.27 / 17.78
HE	0.680 / 0.700	17.27 / 17.78
L	0.090 / 0.110	2.29 / 2.79
θ	- / 0.004	- / 0.10
Δy	/	/



May 2001

44L Plastic Quad Flat Package



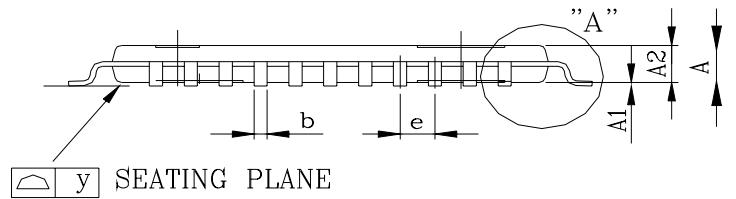
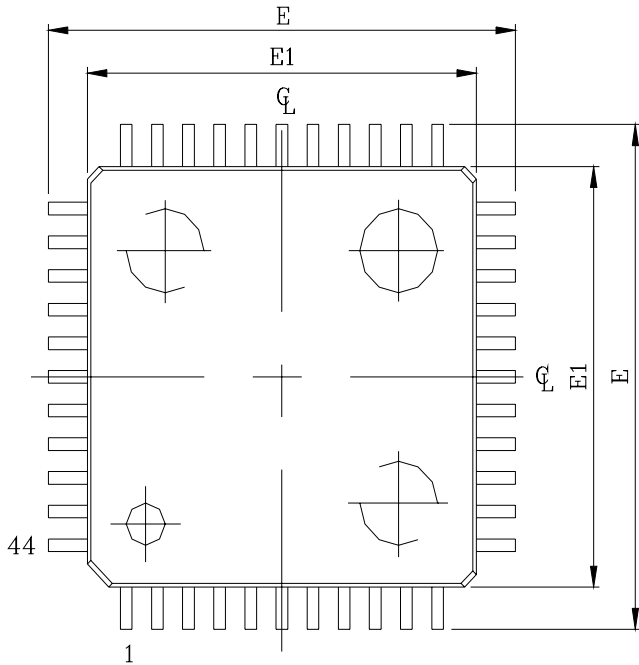
Note:
 Dimension D1 and E1 do not include mold protrusion.
 Allowance protrusion is 0.25mm per side.
 Dimension D1 and E1 do include mold mismatch
 and are determined datum plane.
 Dimension b does not include dam bar protrusion.
 Allowance dam bar protrusion shall be 0.08 mm total
 in excess of the b dimension at maximum material
 condition. Dam bar cannot be located on the lower
 radius or the lead foot.

Symbol	Dimension in Inch	Dimension in mm
	minimal/maximal	minimal/maximal
A	- / 0.100	- / 2.55
A1	0.006 / 0.014	0.15 / 0.35
A2	0.071 / 0.087	1.80 / 2.20
b	0.012 / 0.018	0.30 / 0.45
c	0.004 / 0.009	0.09 / 0.20
D	0.520 BSC	13.20 BSC
D1	0.394 BSC	10.00 BSC
D2	0.315	8.00
E	0.520 BSC	13.20 BSC
E1	0.394 BSC	10.00 BSC
E2	0.315	8.00
e	0.031 BSC	0.80 BSC
L	0.029 / 0.041	0.73 / 1.03
L1	0.063	1.60
R1	0.005 / -	0.13 / -
R2	0.005 / 0.012	0.13 / 0.30
S	0.008 / -	0.20 / -
θ	0° / 7°	as left
θ1	0° / -	as left
θ2	10° REF	as left
θ3	7° REF	as left
△ C	0.004	0.10

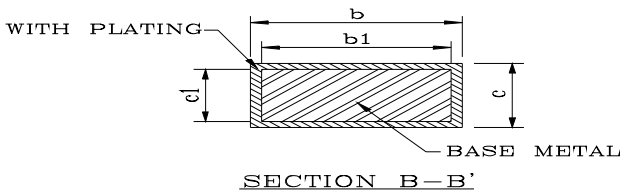
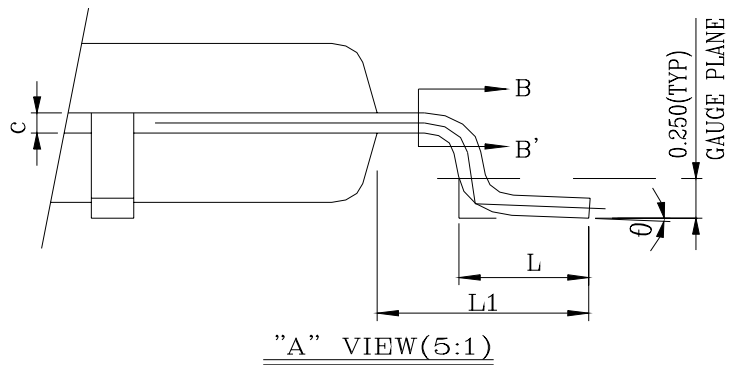
Specifications subject to change without notice, contact your sales representatives for the most recent information.



44L Thin Plastic Quad Flat Package



y SEATING PLANE



Symbol	Dimension in inch (REF)	Dimension in mm (BASE)
	minimal/maximal	minimal/maximal
A	0.047 (MAX)	1.200 (MAX)
A1	0.004 +/- 0.002	0.100 +/- 0.050
A2	0.039 +/- 0.002	1.000 +/- 0.050
b	0.012 (TYP)	0.30 (TYP)
E1	0.472 +/- 0.004	12.000 +/- 0.100
E	0.394 +/- 0.004	10.000 +/- 0.100
e	0.031 (TYP)	0.800 (TYP)
t	0.005 (TYP)	0.127 (TYP)
y	0.003 (TYP)	0.076 (TYP)
theta	0° ~ 7°	0° ~ 7°
L	0.024 +/- 0.006	0.600 +/- 0.150
L1	0.039 (REF)	1.000 (REF)

Specifications subject to change without notice, contact your sales representatives for the most recent information.