

ZXMN2F34MA

20V DFN2X2 N-channel enhancement mode MOSFET

Summary

$V_{(BR)DSS}$	$R_{DS(on)}$ (Ω)	I_D (A)
20	0.060 @ $V_{GS} = 4.5V$	5.1
	0.120 @ $V_{GS} = 2.5V$	3.6

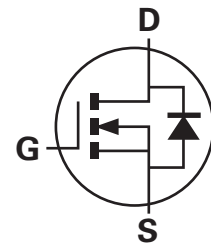


Description

This new generation Trench MOSFET from Zetex features low on-resistance achievable with low (2.5V) gate drive. The 2mm x 2mm DFN package provides superior thermal performance versus alternative leaded devices

Features

- Low on-resistance
- Superior thermal performance (versus to SOT23)
- 2.5V gate drive capability
- DFN 2x2 package

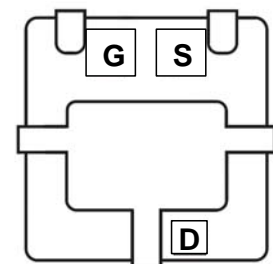


Applications

- Buck/Boost DC-DC Converters
- Motor Control
- LED Lighting

Ordering information

DEVICE	Reel size (inches)	Tape width (mm)	Quantity per reel
ZXMN2F34MATA	7	8	3000



Device marking

1M4

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Absolute maximum ratings

Parameter	Symbol	Limit	Unit
Drain source voltage	V_{DSS}	20	V
Gate source voltage	V_{GS}	± 12	V
Continuous Drain Current @ $V_{GS}=4.5$; $T_A=25^\circ\text{C}^{(b)}$ @ $V_{GS}=4.5$; $T_A=70^\circ\text{C}^{(b)}$ @ $V_{GS}=4.5$; $T_A=25^\circ\text{C}^{(a)}$	I_D	5.1	A
		4.1	A
		4.0	A
Pulsed drain current ^(c)	I_{DM}	19	A
Continuous source current (body diode) ^(b)	I_S	2.2	A
Pulsed source current (body diode) ^(c)	I_{SM}	19	A
Power dissipation at $T_A=25^\circ\text{C}^{(a)}$	P_D	1.35	W
Linear derating factor		10.8	mW/°C
Power dissipation at $T_A=25^\circ\text{C}^{(b)}$	P_D	2.2	W
Linear derating factor		17.8	mW/°C
Operating and storage temperature range	T_j, T_{stg}	-55 to 150	°C

Thermal resistance

Parameter	Symbol	Limit	Unit
Junction to ambient ^(a)	$R_{\theta JA}$	92.5	°C/W
Junction to ambient ^(b)	$R_{\theta JA}$	56	°C/W
Junction to lead ^(d)	$R_{\theta JL}$	19	°C/W

NOTES:

(a) For a device surface mounted on 25mm x 25mm FR4 PCB with high coverage of single sided 1oz copper, in still air conditions.

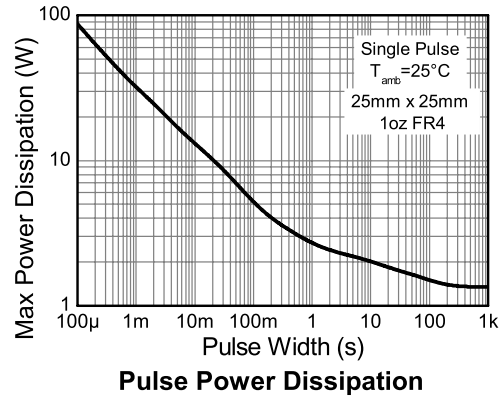
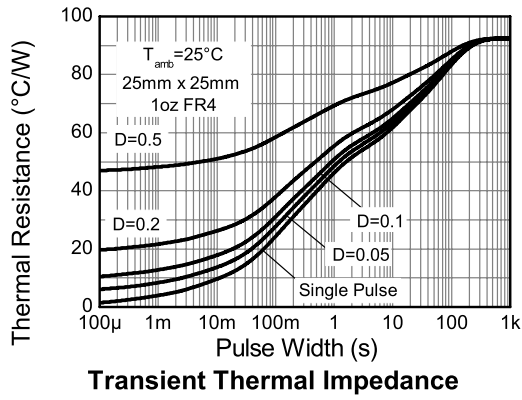
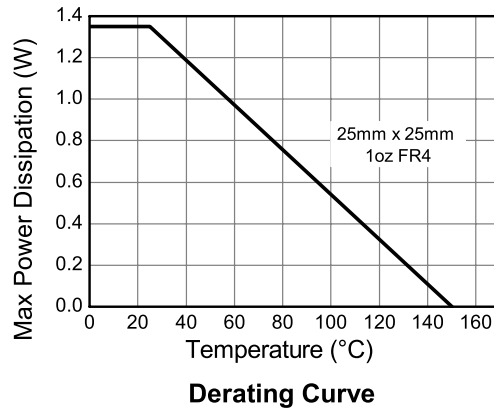
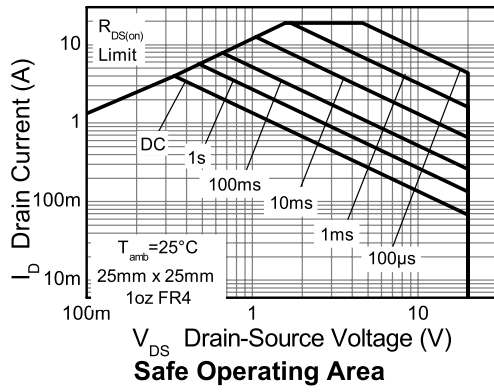
(b) For a device surface mounted on FR4 PCB measured at $t \leq 5$ sec.

(c) Repetitive rating - 25mm x 25mm FR4 PCB, $D=0.02$, pulse width 300 μs - pulse width limited by maximum junction temperature.

(d) Thermal resistance from junction to solder-point (at end of drain lead).

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Thermal characteristics



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Electrical characteristics (at $T_{amb} = 25^{\circ}\text{C}$ unless otherwise stated)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	20			V	$I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$
Zero Gate Voltage Drain Current	I_{DSS}			1	μA	$V_{DS} = 20\text{V}$, $V_{GS} = 0\text{V}$
Gate-Body Leakage	I_{GSS}			100	nA	$V_{GS} = \pm 12\text{V}$, $V_{DS} = 0\text{V}$
Gate-Source Threshold Voltage	$V_{GS(th)}$	0.5	0.8	1.5	V	$I_D = 250\mu\text{A}$, $V_{DS} = V_{GS}$
Static Drain-Source On-State Resistance (*)	$R_{DS(on)}$			0.060 0.120	Ω Ω	$V_{GS} = 4.5\text{V}$, $I_D = 2.5\text{A}$ $V_{GS} = 2.5\text{V}$, $I_D = 1.0\text{A}$
Forward Transconductance ^{(*)(†)}	g_{fs}		7.5		S	$V_{DS} = 10\text{V}$, $I_D = 2.5\text{A}$
Dynamic (†)						
Input Capacitance	C_{iss}		277		pF	$V_{DS} = 10\text{V}$, $V_{GS} = 0\text{V}$ $f = 1\text{MHz}$
Output Capacitance	C_{oss}		65		pF	
Reverse Transfer Capacitance	C_{rss}		35		pF	
Switching (‡)(†)						
Turn-On-Delay Time	$t_{d(on)}$		2.65		ns	$V_{DD} = 10\text{V}$, $V_{GS} = 4.5\text{V}$ $I_D = 1\text{A}$ $R_G \approx 6.0\Omega$
Rise Time	t_r		4.2		ns	
Turn-Off Delay Time	$t_{d(off)}$		9.9		ns	
Fall Time	t_f		5.1		ns	
Total Gate Charge	Q_g		2.8		nC	$V_{DS} = 10\text{V}$, $V_{GS} = 4.5\text{V}$ $I_D = 2.5\text{A}$
Gate-Source Charge	Q_{gs}		0.61		nC	
Gate Drain Charge	Q_{gd}		0.63		nC	
Source-drain diode						
Diode Forward Voltage ^(*)	V_{SD}		0.73	1.2	V	$I_S = 1.25\text{A}$, $V_{GS} = 0\text{V}$

NOTES:

(*) Measured under pulsed conditions. Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.

(†) For design aid only, not subject to production testing.

(‡) Switching characteristics are independent of operating junction temperature.

Typical characteristics

Fig1. $I_D - V_{DS}$

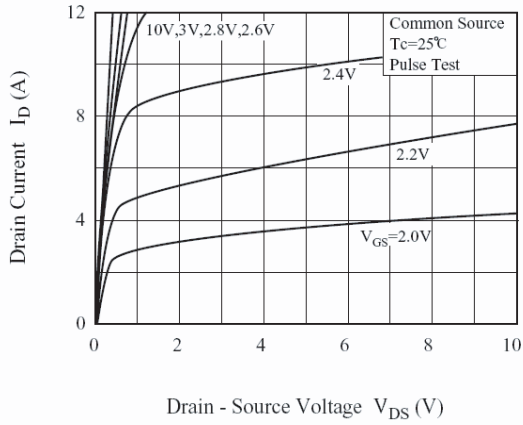


Fig2. $R_{DS(on)} - I_D$

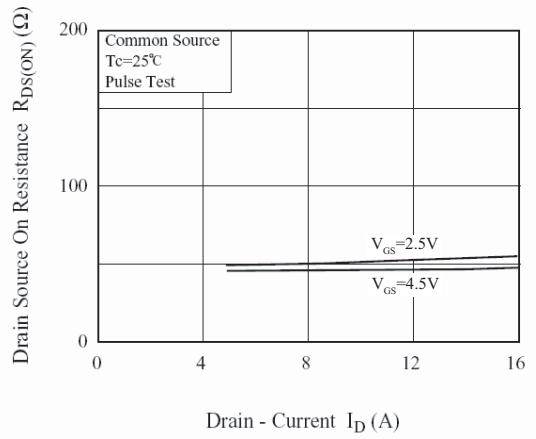


Fig3. $I_D - V_{GS}$

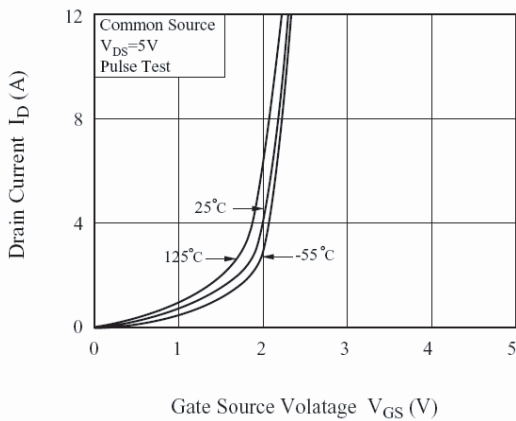


Fig4. $R_{DS(on)} - T_j$

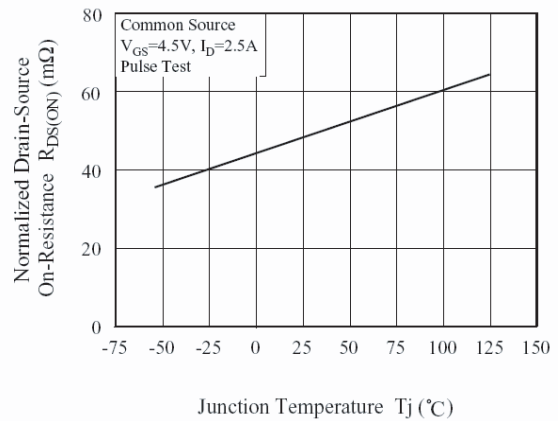


Fig5. $V_{th} - T_j$

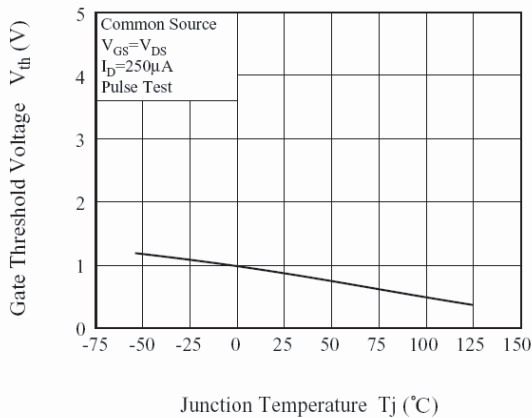
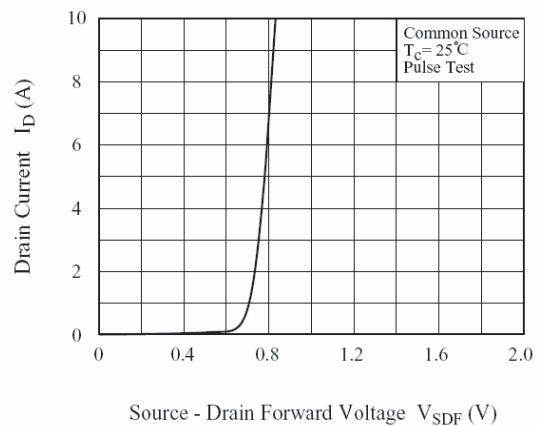
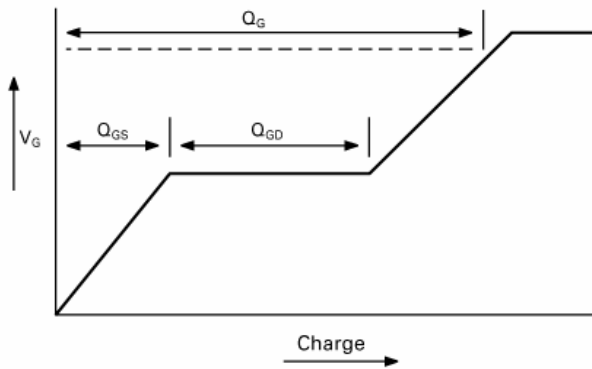


Fig6. $I_S - V_{SDF}$

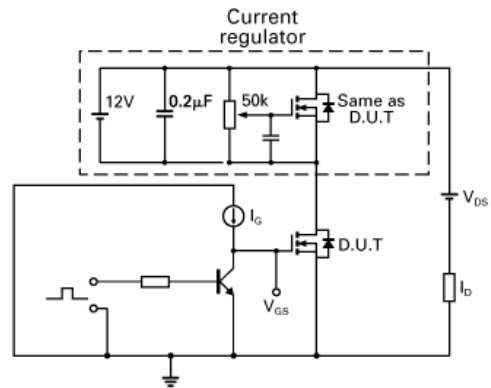


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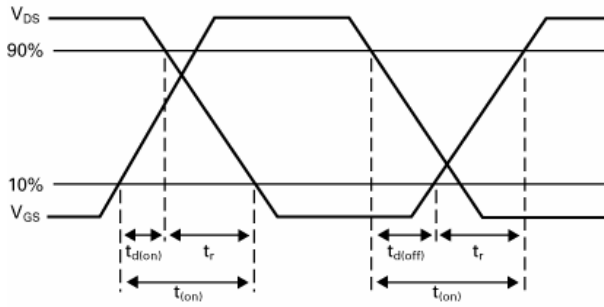
Test circuits



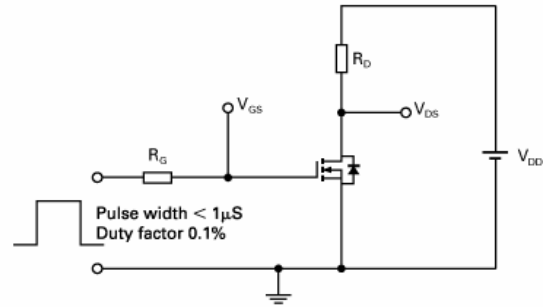
Basic gate charge waveform



Gate charge test circuit



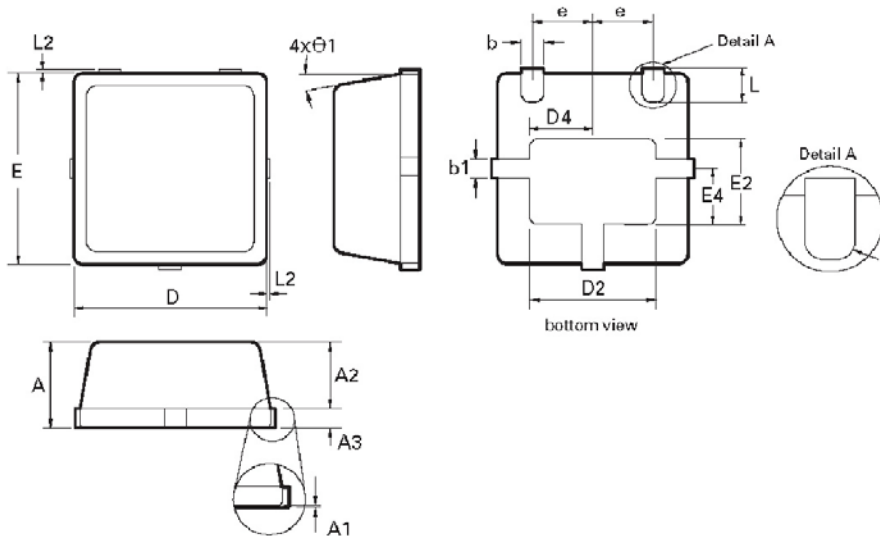
Switching time waveforms



Switching time test circuit

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Package outline - 2mm x 2mm DFN



DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min	Max	Min	Max		Min	Max	Min	Max
A	0.0315	0.0393	0.80	1.00	e	0.0255 REF.		0.65 REF.	
A1	0.00	0.002	0.00	0.05	E	0.0787 BSC		2.00 BSC	
A2	0.0255	0.0295	0.65	0.75	E2	0.031	0.039	0.79	0.99
A3	0.0059	0.0098	0.15	0.25	E4	0.0188	0.0267	0.48	0.68
b	0.0070	0.0110	0.18	0.28	L	0.0078	0.0177	0.20	0.45
b1	0.0066	0.0118	0.17	0.30	L2	0.005 REF.		0.125 MAX.	
D	0.0787 BSC		2.00 BSC		r	0.0029 BSC		0.075 BSC	
D2	0.0480	0.0559	1.22	1.42	θ	0°	12°	0°	12°
D4	0.0220	0.0299	0.56	0.76	-	-	-	-	-

Note: Controlling dimensions are in millimeters. Approximate dimensions are provided in inches

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