19-0613; Rev 1; 11/07

High-/Full-Speed USB 2.0 Switches with High ESD

General Description

The MAX4906EF are electrostatic discharge (ESD)-protected analog switches that combine low on-capacitance (C_{ON}) and low on-resistance (R_{ON}) necessary for high-performance switching applications. The COM_ inputs are protected against ±15kV ESD without latchup or damage. The device is designed for USB 2.0 high-speed applications at 480Mbps. The switches also handle all the requirements for USB low- and full-speed signaling.

The MAX4906EF features two single-pole/double-throw (SPDT) switches. The device is fully specified to operate from a single +2.7V to +3.6V power supply and is protected against a +5.5V short to all analog inputs (COM_, NC_, NO_). This feature makes the MAX4906EF fully compliant with the USB 2.0 specification of +5.5V fault protection. The device features a low threshold voltage and a +1.4V V_{IH}, permitting them to be used with low-voltage logic. The device features a $\overline{QP}$ input that when driven high, turns the charge pump off and sets the device in standby mode. When the device is in standby mode, the quiescent supply current is reduced to 3µA (max) and the switches remain operable.

The MAX4906EF is available in a space-saving, 2mm x 2mm µDFN package and operates over a -40°C to +85°C temperature range.

Applications

- USB Switching
- Cell Phones
- PDAs
- Digital Still Cameras
- GPS
- Notebook Computers
- Relay Replacements
- Ethernet Switching
- Video Switching
- Bus Switches
- T3/E3 Switches for Redundancy Protection

Features

- **±15kV (Human Body Model) ESD Protection, on COM_**
- **Fully Specified for a Single +2.7V to +3.6V Power-Supply Voltage**
- **Low 4Ω (typ), 7Ω (max) On-Resistance (R_{ON})**
- **-3dB Bandwidth: 500MHz (typ)**
- **Low Bit-to-Bit Skew ≤ 20ps**
- **Charge-Pump Noise = 90µV (typ)**
- **Charge-Pump Enable**
- **No Need for Logic-Level Shifters for 1.4V or Above**
- **COM_ Analog Inputs Fault-Protected Against Shorts to USB Supply Rail Up to +5.5V**
- **Low Supply Current 3µA (max) in Standby**
- **Space-Saving 10-Pin, 2mm x 2mm µDFN Package**

Ordering Information

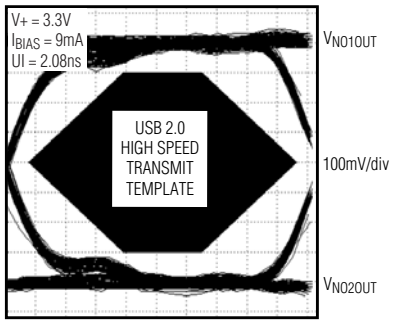
PART	PIN-PACKAGE	TOP MARK	PKG CODE
MAX4906EFELB+T	10 µDFN-10	AAJ	L1022-1

Note: *The device operates over the -40°C to +85°C operating temperature range.*

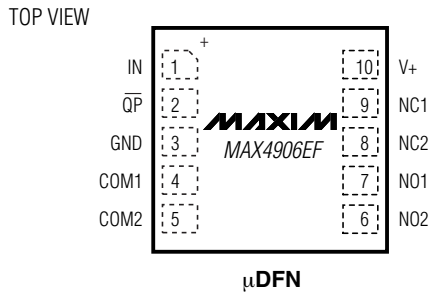
+Denotes a lead-free package.

Typical Operating Characteristics

EYE DIAGRAM



Pin Configuration



µDFN

High-/Full-Speed USB 2.0 Switches with High ESD

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)
V+ .....-0.3V to +4V
IN, $\overline{QP}$ (Note 1) .....-0.3V to +4V
COM_, NO_, NC_ .....-0.3V to +5.5V
Continuous Current (COM_ to NO_/NC_) .....±120mA
Peak Current, (COM_ to NO_/NC_)
(pulsed at 1ms 10% duty cycle).....±240mA

Continuous Power Dissipation (T_A = +70°C)
10-Pin µDFN (derate 5.0mW/°C above +70°C) 403mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: Signals on IN, $\overline{QP}$ exceeding GND are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = +2.7V to +3.6V, T_A = T_{MIN} to T_{MAX}, charge-pump enabled, unless otherwise noted. Typical values are at V+= 3.3V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	$V_{COM\_}$, $V_{NO\_}$, $V_{NC\_}$	$\overline{QP}$ = 0 or V+ (Note 3)		0		3.6	V
Fault-Protection Trip Threshold (Note 9)	V_{FP}			3.62	3.9	4.20	V
On-Resistance, Charge-Pump Enabled	R_{ON}	V+ = 2.7V, $I_{COM\_}$ = -10mA, $V_{COM\_}$ = 0V, 1.5V, $\overline{QP}$ = 0V	T_A = +25°C		3.8	5	Ω
			T_A = T_{MIN} to T_{MAX}			6	
		V+ = 2.7V, $I_{COM\_}$ = -10mA, $V_{COM\_}$ = 2.7V, $\overline{QP}$ = 0V	T_A = +25°C		4	7	Ω
			T_A = T_{MIN} to T_{MAX}			8	
On-Resistance, Charge-Pump Disabled	R_{ON}	V+ = 3.0V, $I_{COM\_}$ = -10mA, $V_{COM\_}$ = 0V, 1.5V, $\overline{QP}$ = V+	T_A = +25°C		5	12	Ω
			T_A = T_{MIN} to T_{MAX}			13	
		V+=2.7V, $I_{COM\_}$ = -10mA, $V_{COM\_}$ = 0V, 1.5V, $\overline{QP}$ = V+	T_A = +25°C		8	15	
			T_A = T_{MIN} to T_{MAX}			17	
On-Resistance Match Between Channels	ΔR_{ON}	V+ = 2.7V, $I_{COM\_}$ = -10mA, $V_{COM\_}$ = 0V, 1.5V, 2.7V (Note 4)	T_A = +25°C		0.5	0.8	Ω
			T_A = T_{MIN} to T_{MAX}			1.0	
On-Resistance Flatness	$R_{FLAT(ON)}$	V+ = 2.7V, $I_{COM\_}$ = -10mA, $V_{COM\_}$ = 0V, 1.5V (Note 5)			0.5		Ω

ELECTRICAL CHARACTERISTICS (continued)

(V+ = +2.7V to +3.6V, T_A = T_{MIN} to T_{MAX}, charge-pump enabled, unless otherwise noted. Typical values are at V+= 3.3V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Off-Leakage Current	$I_{NC\_}$, $I_{NO\_}$ (OFF)	V+ = 3.6V, $V_{COM\_}$ = 0.3V, 3.3V; $V_{NO\_}$ or $V_{NC\_}$ = 3.3V, 0.3V	-1		+1	µA
On-Leakage Current	$I_{NC\_}$, $I_{NO\_}$ (ON)	V+ = 3.6V, V_{COM} = 0.3V, 3.3V; $V_{NO\_}$ or $V_{NC\_}$ = 0.3V, 3.3V, or floating	-1		+1	µA
SWITCH AC PERFORMANCE						
On-Channel -3dB Bandwidth	BW	R_L = R_S = 50Ω, signal = 0dBm, Figure 1		500		MHz
Off-Isolation	V_{ISO}	f = 10MHz; $V_{NO\_}$, $V_{NC\_}$ = $1V_{P-P}$; R_L = R_S = 50Ω, Figure 1		-60		dB
		f = 250MHz; $V_{NO\_}$, $V_{NC\_}$ = $1V_{P-P}$; R_L = R_S = 50Ω, Figure 1		-32		
Crosstalk (Note 6)	V_{CT}	f = 10MHz; $V_{NO\_}$, $V_{NC\_}$ = $1V_{P-P}$; R_L = R_S = 50Ω, Figure 1		-59		dB
		f = 250MHz; $V_{NO\_}$, $V_{NC\_}$ = $1V_{P-P}$; R_L = R_S = 50Ω, Figure 1		-31		
Charge-Pump Noise (Note 7)	V_{QP}	Any input or output switch terminal = 50Ω		90		µV
SWITCH DYNAMICS						
NO_, NC_, COM_ Off-Capacitance (Note 8)	$C_{(OFF)}$	f = 1MHz, Figure 2		9	10	pF
NO_, NC_, COM_ On-Capacitance (Note 8)	$C_{(ON)}$	f = 1MHz, Figure 2		10	12	pF
Switch On-Capacitance Matching (Note 8)	C_{ONM}	f = 1MHz		0.4		pF
Turn-On Time	t_{ON}	$V_{NO\_}$, $V_{NC\_}$ = 1.5V; R_L = 300Ω, C_L = 35pF, V_{IH} = V+, V_{IL} = 0V, $\overline{QP}$ = 0V, Figure 3		1.4		ns
Turn-Off Time	t_{OFF}	$V_{NO\_}$, $V_{NC\_}$ = 1.5V; R_L = 300Ω, C_L = 35pF, V_{IH} = V+, V_{IL} = 0V, $\overline{QP}$ = 0V, Figure 3		35		ns
Propagation Delay	$t_{PLH\_}$,t_{PHL}	R_L = R_S = 50Ω, Figure 4		0.2		ns
Fault-Protection Response Time	t_{FP}	$V_{COM\_}$ = 0 to 5V step, R_L = R_S = 50Ω, C_L = 10pF, Figure 5		1		µs
Fault-Protection Recovery Time	t_{FPR}	$V_{COM\_}$ = 5V to 3V step, R_L = R_S = 50Ω, C_L = 10pF, Figure 5		1		µs
Output Skew Between Switches (Note 8)	$t_{SK(o)}$	Skew between switch 1 and switch 2, R_L = R_S = 50Ω, Figure 4		20	100	ps
Output Skew Same Switch (Note 8)	$t_{SK(p)}$	Skew between opposite transitions in same switch, R_L = R_S = 50Ω, Figure 4		5	100	ps

High-/Full-Speed USB 2.0 Switches with High ESD

ELECTRICAL CHARACTERISTICS (continued)

(V+ = +2.7V to +3.6V, T_A = T_{MIN} to T_{MAX}, charge-pump enabled, unless otherwise noted. Typical values are at V+= 3.3V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Total Harmonic Distortion Plus Noise	THD+N	$V_{COM\_}$ = $2V_{P-P}$, R_L = 600Ω, f = 20Hz to 20kHz		0.01		%
Charge Injection	Q	V_{GEN} = 1.5V, R_{GEN} = 0Ω, C_L = 100pF, Figure 6		20		pC
SWITCH LOGIC						
Logic-Input Voltage Low	V_{IL}				0.4	V
Logic-Input Voltage High	V_{IH}		1.4			V
Input-Logic Hysteresis	V_{HYST}			100		mV
Input Leakage Current	I_{IN}	V+ = 3.6V, V_{IN} = 0 or V+	-1		+1	µA
Operating Supply-Voltage Range	V+		2.7		3.6	V
Quiescent Supply Current	I+	V+ = 3.6V, V_{IN} = 0 or V+, $\overline{QP}$ = 0V		160	1000	µA
Quiescent Supply Current With Charge-Pump Disabled	I+	V+ = 3.6V, V_{IN} = 0 or V+, $\overline{QP}$ = V+			3	µA
ESD PROTECTION						
COM_		Human Body Model		±15		kV

Note 2: All units are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and not production tested.

Note 3: The switch will turn off for voltages above (V_{FP}); therefore, protecting downstream circuits in case of a fault condition.

Note 4: $\Delta R_{ON(MAX)} = | R_{ON(CH1)} - R_{ON(CH2)} |$

Note 5: Flatness is defined as the difference between the maximum and minimum value of on-resistance, as measured over specified analog signal ranges.

Note 6: Between any two switches.

Note 7: Noise specification is measured peak to peak.

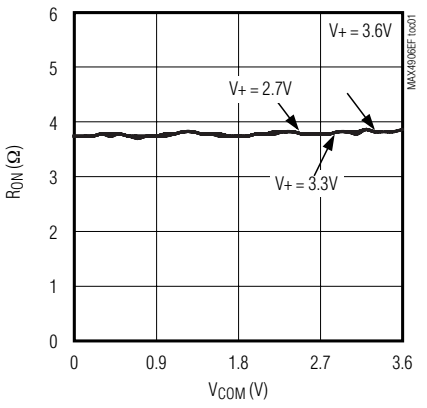
Note 8: Switch off-capacitance, switch on-capacitance, output skew between switches, and output skew same-switch limits are not production tested; design guaranteed by correlation.

Note 9: Fault-protection trip threshold, limits are not production tested; guaranteed by design.

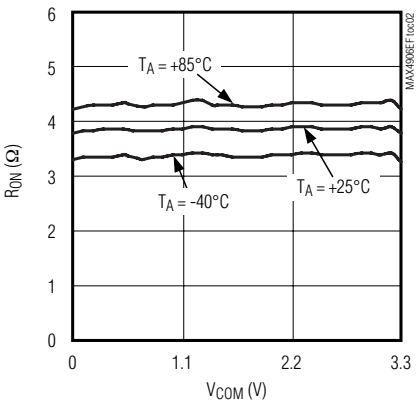
Typical Operating Characteristics

(V+ = 3.3V, T_A = +25°C, unless otherwise noted.)

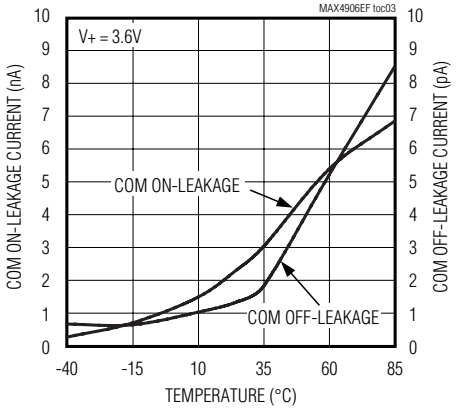
ON-RESISTANCE vs. V_{COM}



ON-RESISTANCE vs. V_{COM}



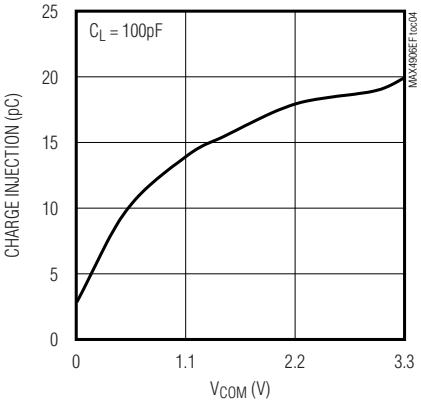
LEAKAGE CURRENT vs. TEMPERATURE



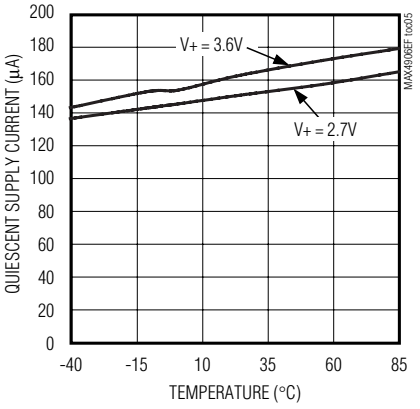
Typical Operating Characteristics (continued)

(V+ = 3.3V, T_A = +25°C, unless otherwise noted.)

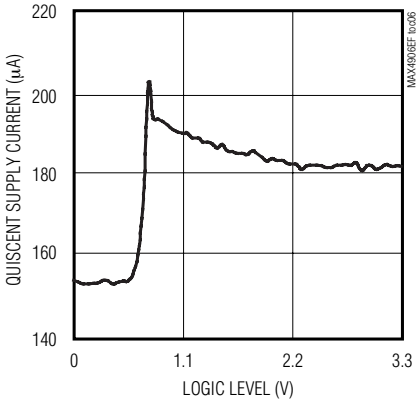
CHARGE INJECTION vs. V_{COM}



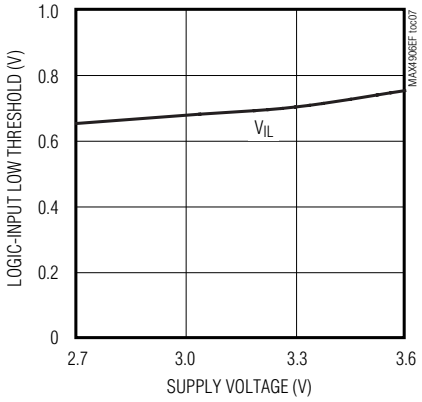
QUIESCENT SUPPLY CURRENT vs. TEMPERATURE



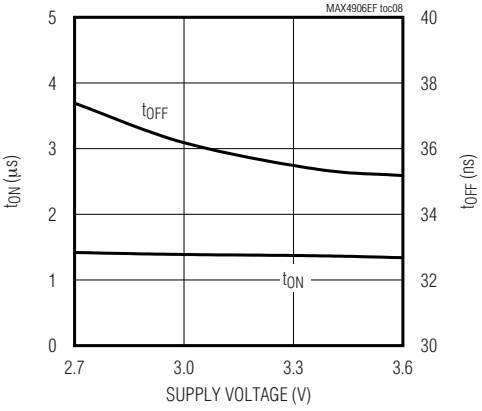
QUIESCENT SUPPLY CURRENT vs. LOGIC LEVEL



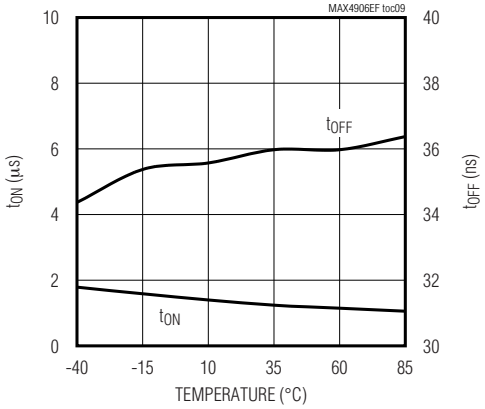
LOGIC-INPUT LOW THRESHOLD vs. SUPPLY VOLTAGE



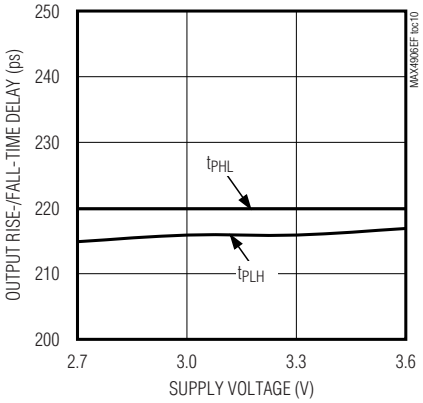
TURN-ON/-OFF TIME vs. SUPPLY VOLTAGE



TURN-ON/-OFF TIME vs. TEMPERATURE



RISE-/FALL-TIME PROPAGATION DELAY vs. SUPPLY VOLTAGE

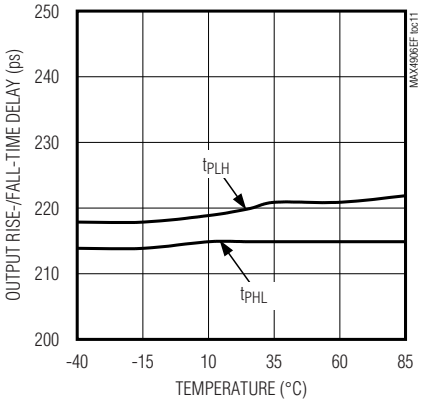


High-/Full-Speed USB 2.0 Switches with High ESD

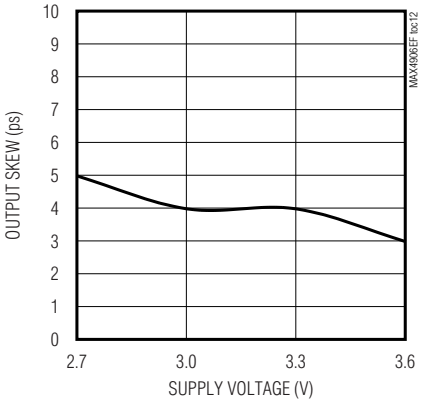
Typical Operating Characteristics (continued)

(V+ = 3.3V, T_A = +25°C, unless otherwise noted.)

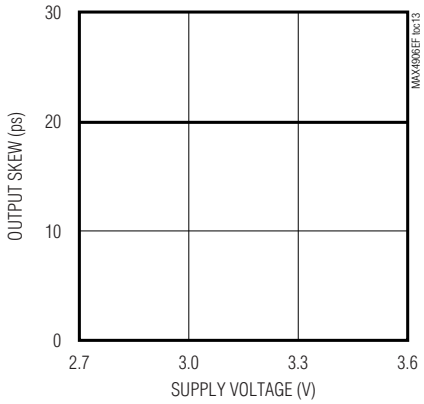
RISE-/FALL-TIME PROPAGATION DELAY vs. TEMPERATURE



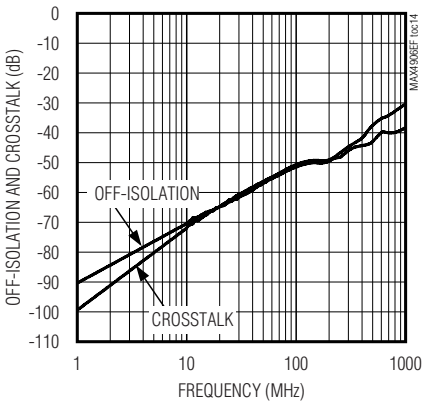
SAME SWITCH OUTPUT SKEW vs. SUPPLY VOLTAGE



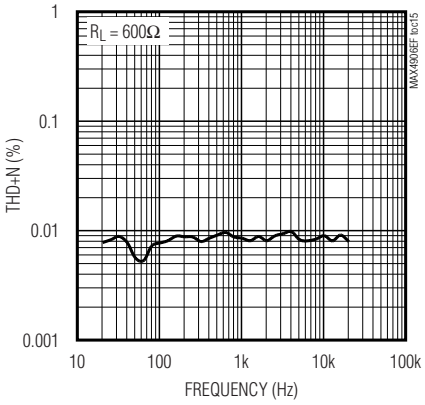
OUTPUT SKEW BETWEEN SWITCHES vs. SUPPLY VOLTAGE



FREQUENCY RESPONSE



TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



Pin Description

PIN	NAME	FUNCTION
1	IN	Digital Control Input. IN controls switch 1 and switch 2.
2	$\overline{QP}$	Charge-Pump Enable Input. Drive $\overline{QP}$ high to turn charge pump off. For normal operation, drive $\overline{QP}$ low.
3	GND	Ground
4	COM1	Analog Switch 1—Common Terminal
5	COM2	Analog Switch 2—Common Terminal
6	NO2	Analog Switch 2—Normally Open Terminal
7	NO1	Analog Switch 1—Normally Open Terminal
8	NC2	Analog Switch 2—Normally Closed Terminal
9	NC1	Analog Switch 1—Normally Closed Terminal
10	V+	Positive-Supply Voltage Input. Connect V+ to a +2.7V to +3.6V supply voltage. Bypass V+ to GND with a 0.1µF capacitor.

Test Circuits/Timing Diagrams

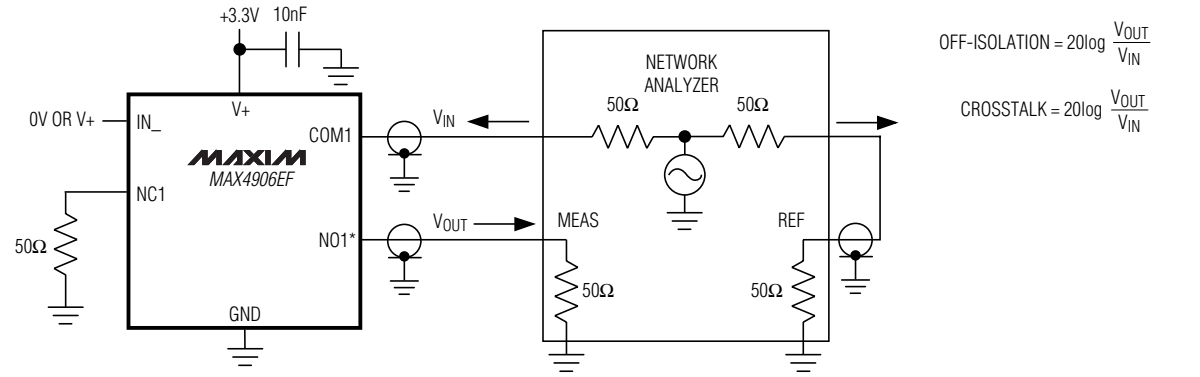


Figure 1. Off-Isolation and Crosstalk

High-/Full-Speed USB 2.0 Switches with High ESD

Test Circuits/Timing Diagrams (continued)

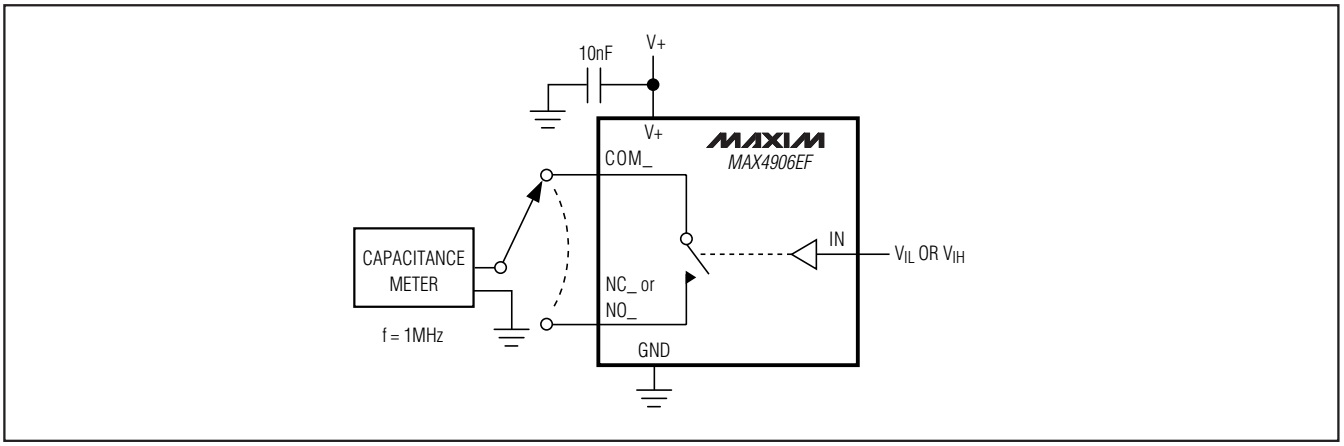


Figure 2. Channel Off-/On-Capacitance

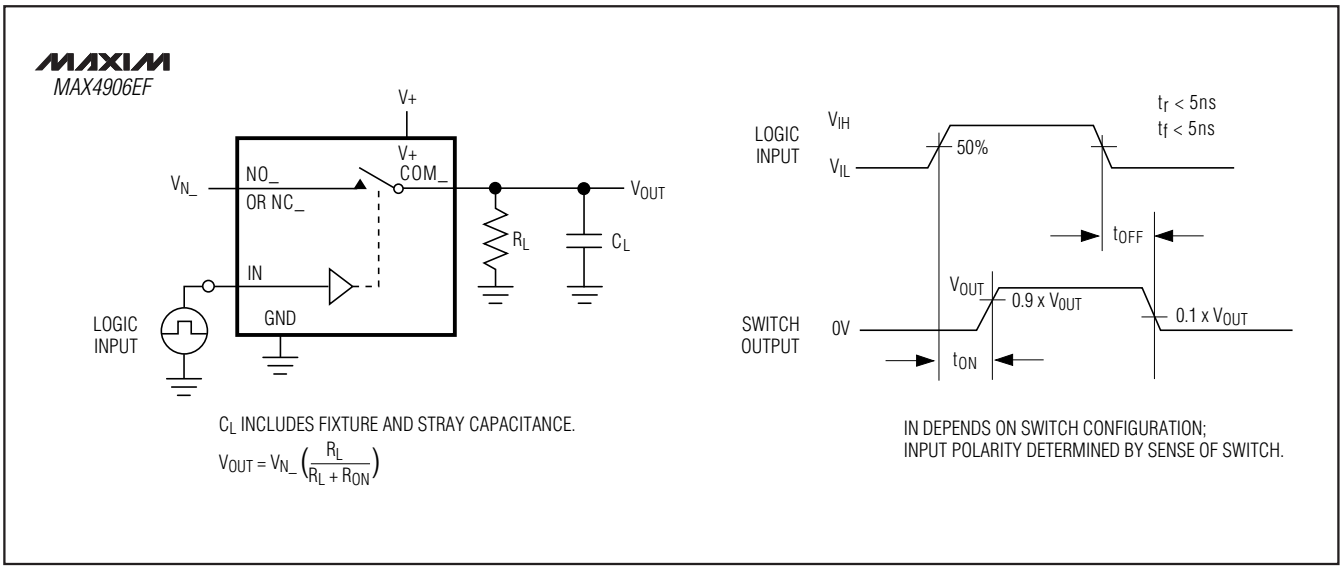


Figure 3. Switching Time

Test Circuits/Timing Diagrams (continued)

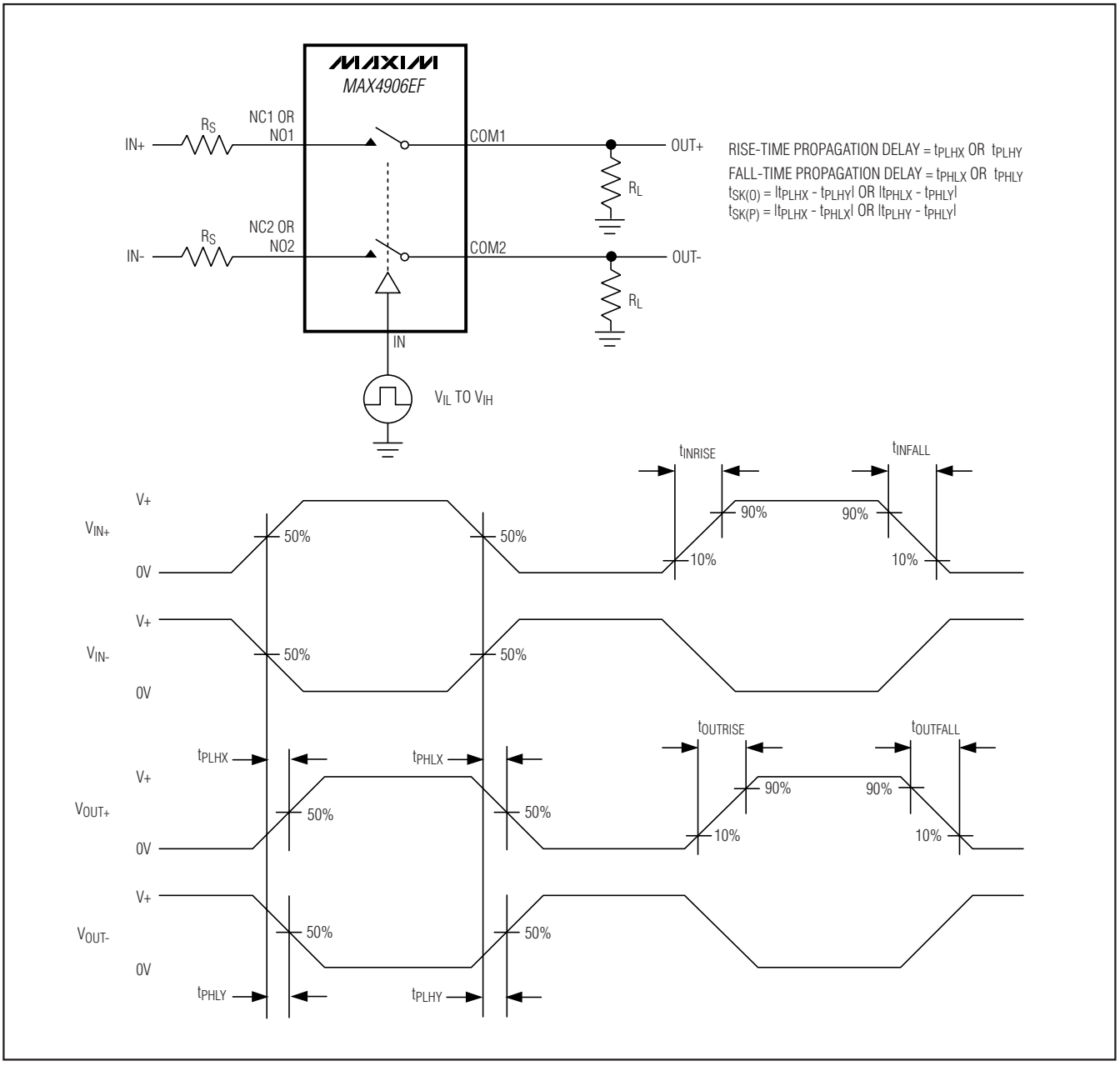


Figure 4. Output Signal Skew, Rise/Fall Time, Propagation Delay

High-/Full-Speed USB 2.0 Switches with High ESD

Test Circuits/Timing Diagrams (continued)

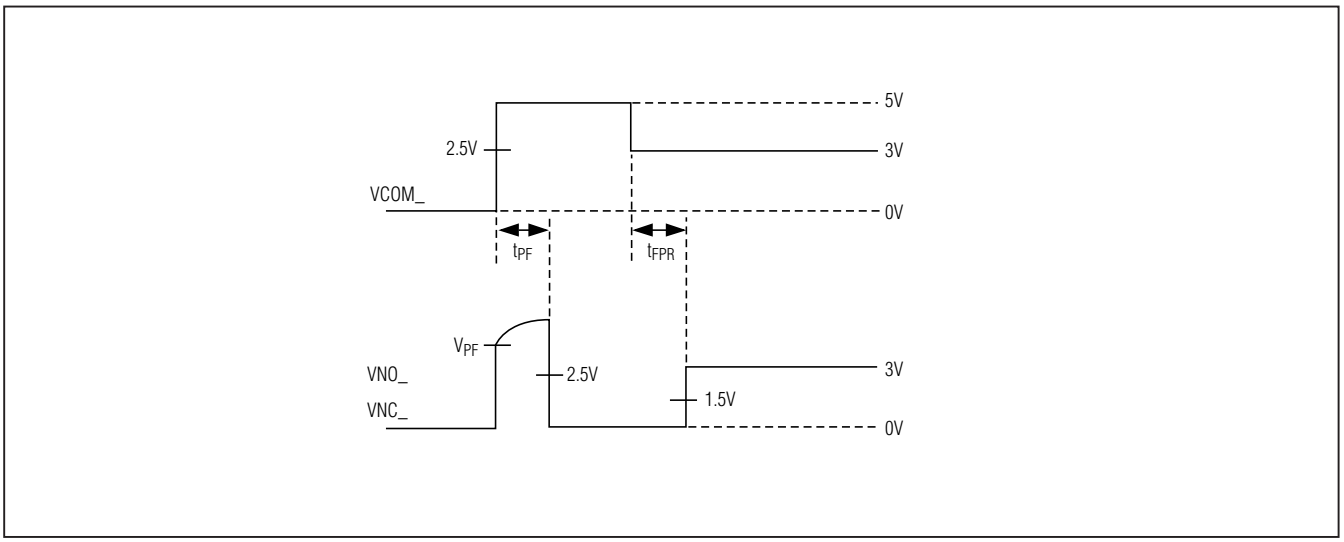


Figure 5. MAX4906EF Fault-Protection Response/Recovery Time

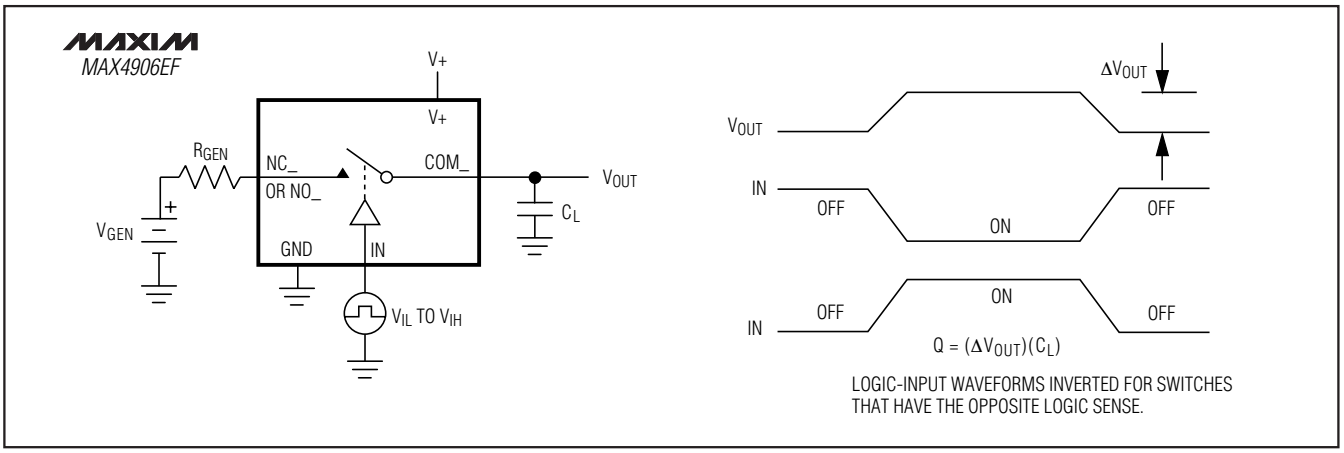


Figure 6. Charge Injection

Detailed Description

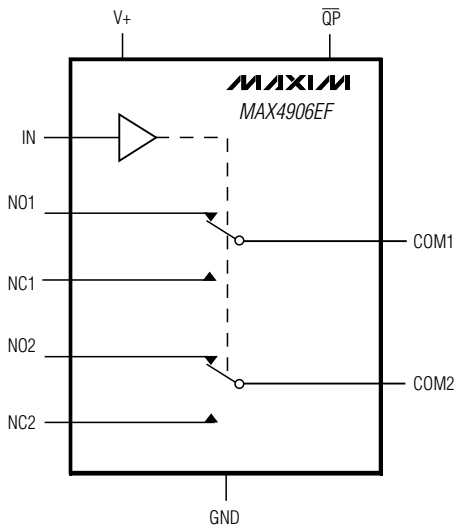
The MAX4906EF are ESD-protected analog switches where the COM_ inputs are further protected up to ±15kV ESD without latchup or damage. The device is targeted for USB 2.0 high-speed (480Mbps) switching applications. The device still meets USB low- and full-speed requirements and is suitable for 10/100 Ethernet switching. The MAX4906EF features two SPDT switches.

The MAX4906EF is fully specified to operate from a single +2.7V to +3.6V supply and is +5.5V fault protected. When operating from a +2.7V to +3.6V supply, the low threshold of the device permits them to be used with logic levels as low as 1.4V. The MAX4906EF is based on a charge-pump-assisted n-channel architecture and thus operate at 170µA (max) quiescent current. The device features a standby mode to reduce the quiescent current to less than 3µA (max).

Digital Control Input

The MAX4906EF provides a single-digit control logic input, IN. IN controls the position of the switches as shown in the *Functional Diagram/Truth Table*. Driving IN

Functional Diagram/Truth Table



MAX4906EF				
$\overline{QP}$	IN	NO1 NO2	NC1 NC2	
0	0	OFF	ON	HIGH PERFORMANCE
0	1	ON	OFF	HIGH PERFORMANCE
1	0	OFF	ON	LOW PERFORMANCE
1	1	ON	OFF	LOW PERFORMANCE

rail-to-rail minimizes power consumption. With a +2.7V to +3.6V supply voltage range, the device is +1.4V logic compatible.

Analog Signal Levels

The on-resistance of the MAX4906EF is very low and stable as the analog input signals are swept from ground to V+ (see the *Typical Operating Characteristics*). These switches are bidirectional, allowing NO_, NC_, and COM_ to be configured as either inputs or outputs.

Overvoltage Fault Protection

The MAX4906EF features +5.5V fault protection to all analog inputs. Fault protection prevents these switches from being damaged due to shorts to the USB bus voltage rail.

Charge-Pump Enable

The MAX4906EF features a charge-pump enable mode that improves the performance and the dynamic range of the device. The device features a $\overline{QP}$ input that when driven high, turns the charge pump off and sets the device in standby mode. When the device is in standby mode, the quiescent supply current is reduced to 3µA (max) and the switches remain operable. When $\overline{QP}$ is driven low, the charge pump is enabled and the switches enter an improved high-performance mode.

Applications Information

USB Switching

The MAX4906EF analog switch is fully compliant with the USB 2.0 specification. The low on-resistance and low on-capacitance of these switches make the device ideal for high-performance switching applications. The MAX4906EF is ideal for routing USB data lines (see Figure 7) and for applications that require switching between multiple USB hosts (see Figure 8). The MAX4906EF also features +5.5V fault protection to guard systems against shorts to the USB bus voltage that is recommended for all USB applications.

Ethernet Switching

The wide bandwidth of the MAX4906EF meets the needs of 10/100 Ethernet switching. The device switch the signals from two interface transformers and connect the signals to a single 10/100 Base-T Ethernet PHY, simplifying docking station design and reducing manufacturing costs.

±15kV ESD Protection

As with all Maxim devices, ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. COM_ are further protected against static electricity. Maxim's engineers have developed state-of-the-art structures to protect these pins against ESD up to ±15kV without damage. The ESD structures withstand high ESD in normal operation, and when the device is powered down. After an ESD event, the MAX4906EF continues to function without latchup, whereas competing products can latch and must be powered down to restore functionality.

ESD protection can be tested in various ways. The ESD protection of COM_ are characterized for ±15kV (Human Body Model) using the MIL-STD-883.

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Human Body Model

Figure 9a shows the Human Body Model and Figure 9b shows the current waveform it generates when discharged into a low impedance. This model consists of

High-/Full-Speed USB 2.0 Switches with High ESD

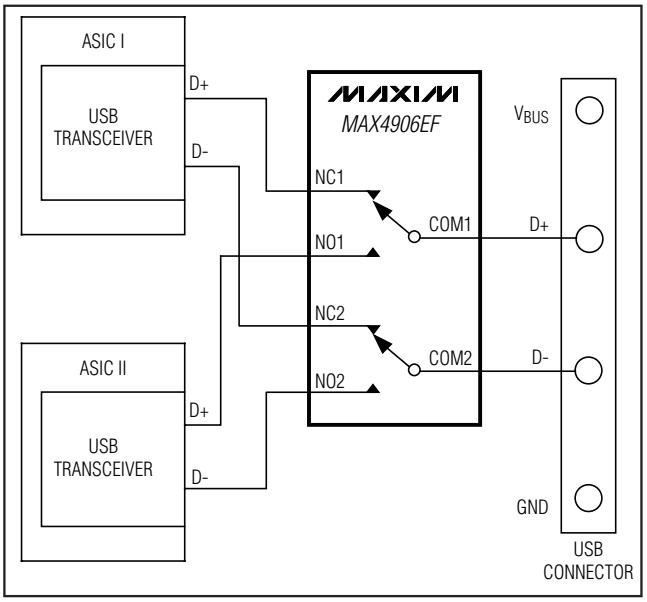


Figure 7. USB Data Routing

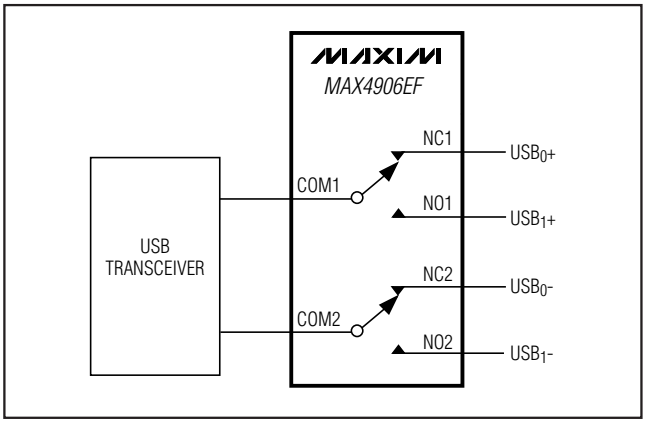


Figure 8. Switching Between Multiple USB Hosts

a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

Layout

High-speed switches require proper layout and design procedures for optimum performance. Keep design-controlled-impedance PC board traces as short as possible. Ensure that bypass capacitors are as close to the device as possible. Use large ground planes where possible.

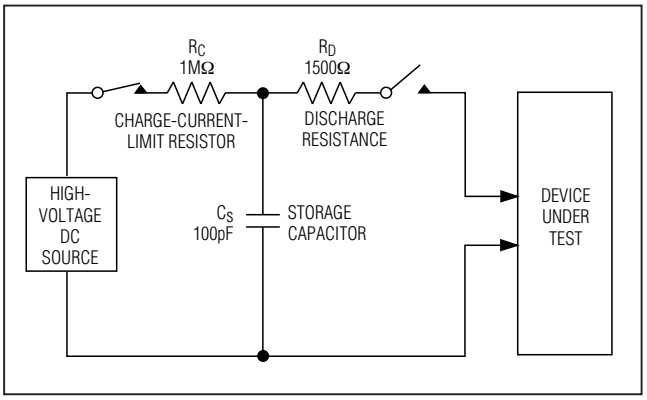


Figure 9a. Human Body ESD Test Model

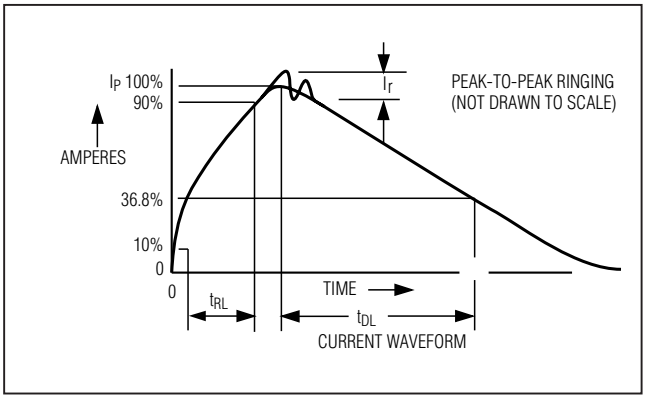


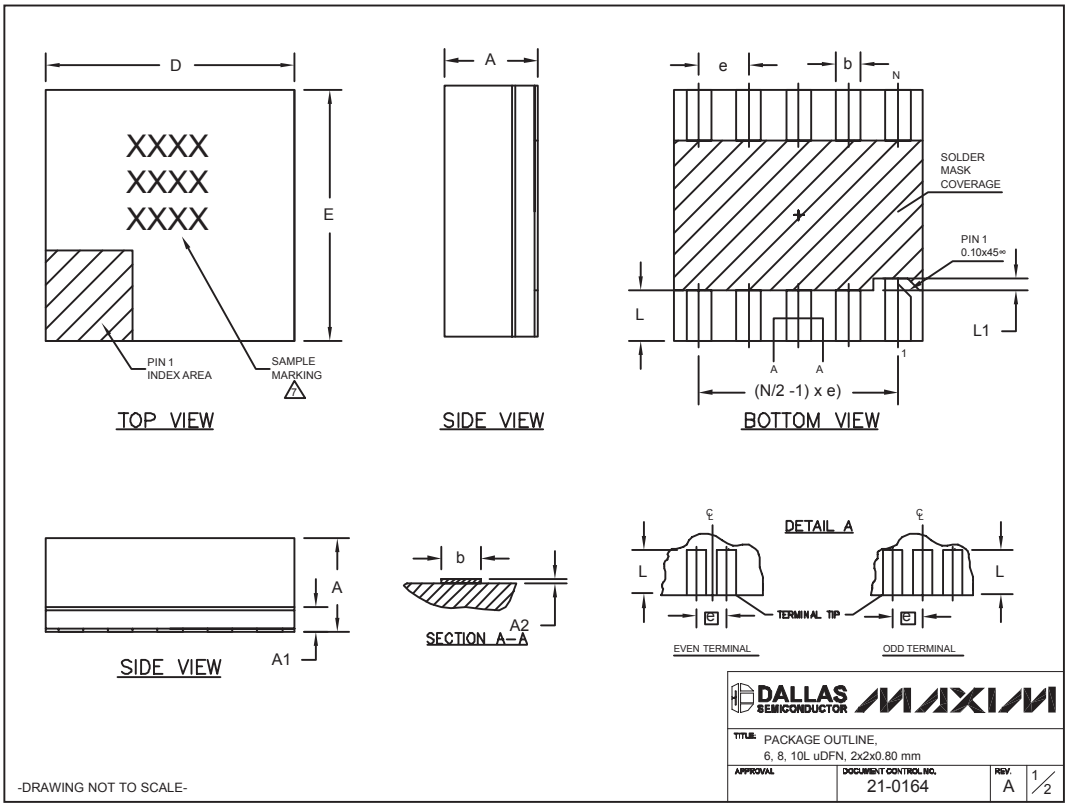
Figure 9b. Human Body Current Waveform

Chip Information

PROCESS: BiCMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



High-/Full-Speed USB 2.0 Switches with High ESD

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS			
SYMBOL	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.15	0.20	0.25
A2	0.020	0.025	0.035
D	1.95	2.00	2.05
E	1.95	2.00	2.05
L	0.30	0.40	0.50
L1	0.10 REF.		

PACKAGE VARIATIONS				
PKG. CODE	N	e	b	(N/2 -1) x e
L622-1	6	0.65 BSC	0.30±0.05	1.30 REF.
L822-1	8	0.50 BSC	0.25±0.05	1.50 REF.
L1022-1	10	0.40 BSC	0.20±0.03	1.60 REF.

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08mm.
3. WARPAGE SHALL NOT EXCEED 0.10mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. "N" IS THE TOTAL NUMBER OF LEADS.
6. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
7. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 6, 8, 10L uDFN, 2x2x0.80 mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0164	A	2/2

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/06	Initial release	—
1	11/07	Changes to EC Table	2, 4