SM5168 series
PLL Synthesizer IC

OVERVIEW

The SM5168 series are PLL synthesizer ICs fabricated using NPC's Molybdenum-gate CMOS process. They provide several combinations of reference and comparator frequency divider ratios, set in master-slice, making them ideal for frequency synthesizers in IF stages of mobile communications devices. They also feature a lock detect signal output (LD).

FEATURES

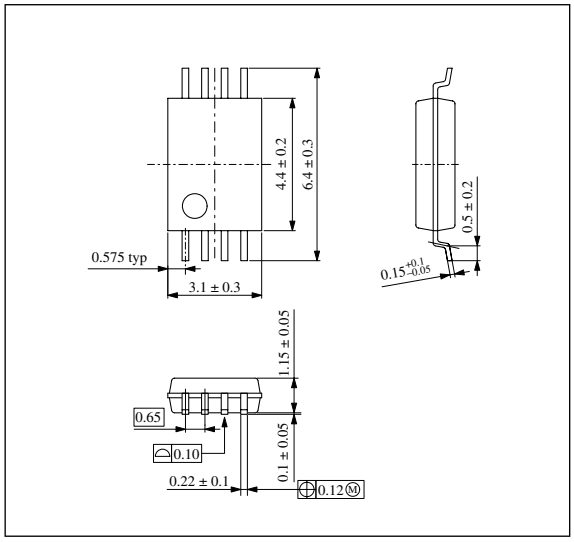
- 2.7 to 3.6V operating supply voltage range
- Maximum operating frequency
  - SM5168A× series: 200MHz, V_{DD} = 2.7V
  - SM5168C× series: 340MHz, V_{DD} = 2.7V
- Operating current consumption
  - SM5168A× series: 3.3mA (typ, 200MHz at 0.3Vp-p, V_{DD} = 3.0 V)
  - SM5168C× series: 4mA (typ, 340MHz at 0.3Vp-p, V_{DD} = 3.0 V)
- SM5168A× (built-in standby function) and SM168C× (dual frequency divider ratios) series available, as set by master-slice
- Charge pump output with output polarity for connection to passive filter
- Lock detect function output
- −30 to 85°C operating temperature range
- 8-pin plastic VSOP

APPLICATIONS

- Mobile communications
- Portable telephones
- Related applications

PACKAGE DIMENSIONS

(Unit: mm)



SERIES CONFIGURATION

Version	Maximum operating frequency	Reference/comparator frequency dividers	Frequency divider ratio range[1]		Standby function
			N counter	R counter	
SM5168A× series	200MHz	1	272 to 65535	5 to 65535	Yes
SM5168C× series	340MHz	2	272 to 65535	5 to 65535	No

1. SM5168C× series: Dual frequency divider ratios are set within the ratio ranges.

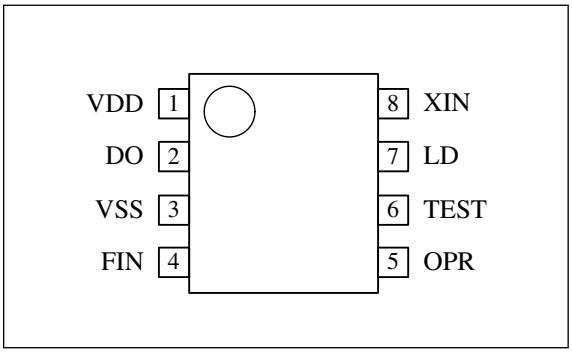
ORDERING INFORMATION

Device	Package
SM5168××V	8-pin VSOP

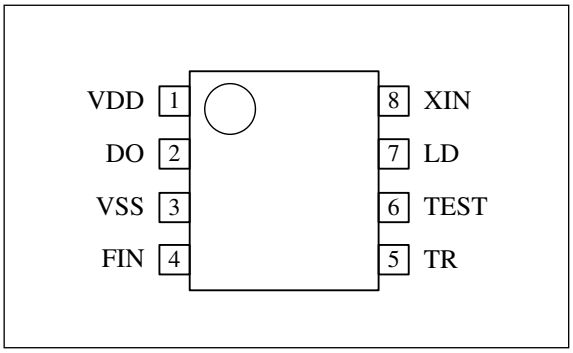
PINOUT

(Top view)

SM5168A× series



SM5168C× series

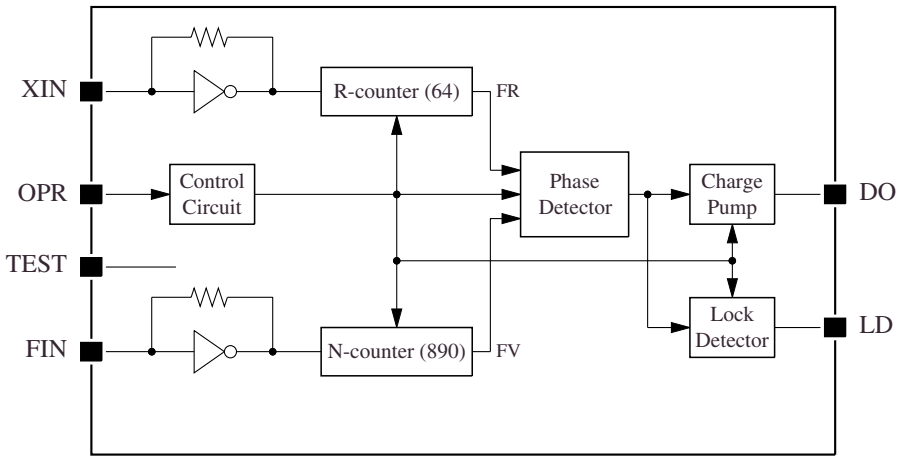


PIN DESCRIPTION

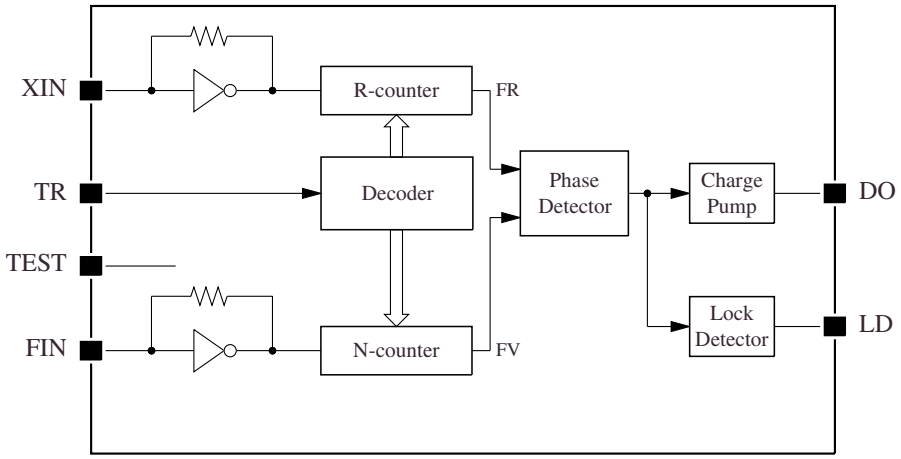
Number	Name	I/O	Description
1	VDD	–	2.7 to 3.6V supply
2	DO	O	Phase comparator error signal three-state output pin. Built-in charge pump means that this output can be connected to a low-pass filter. The output polarity is preset for connection to a passive filter.
3	VSS	–	Ground pin
4	FIN	I	Phase comparator frequency divider (N-counter) signal input pin. Feedback resistor built-in, so input can be AC-coupled.
5	OPR (SM5168A× series)	I	Power-save control pin. Start when HIGH, standby mode when LOW.
	TR (SM5168C× series)		Frequency divider switching control. Switches between 2 sets of reference and comparator frequency dividers.
6	TEST	I	Test pin. Leave open or connect to VSS for normal operation.
7	LD	O	Unlock signal output pin. (Unlocked when LOW)
8	XIN	I	Reference frequency divider (R-counter) external clock input pin. Feedback resistor built-in, so input can be AC-coupled.

BLOCK DIAGRAMS

SM5168A× series



SM5168C× series



SPECIFICATIONS

Absolute Maximum Ratings

V_{SS} = 0V

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD}	–0.3 to 6.0	V
Input voltage range	V_{IN}	V_{SS} – 0.3 to V_{DD} + 0.3	V
Storage temperature range	T_{STG}	–55 to 125	°C
Power dissipation	P_D	100	mW

Recommended Operating Conditions

V_{SS} = 0V

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD}	2.7 to 3.6	V
Operating temperature range	T_{OPR}	–30 to 85	°C

Electrical Characteristics

V_{SS} = 0V, V_{DD} = 2.7 to 3.6V, Ta = –30 to 85°C unless otherwise noted.

Parameter	Symbol	Condition		Rating			Unit
				min	typ	max	
Supply voltage	V_{DD}			2.7	–	3.6	V
VDD operating current consumption 1 (SM5168A× series)	I_{DD1}	Note 1.	V_{DD} = 3.0V	–	3.3	–	mA
			V_{DD} = 3.3V	–	–	5.2	
VDD operating current consumption 2 (SM5168C× series)	I_{DD2}	Note 2.	V_{DD} = 3.0V	–	4	–	mA
			V_{DD} = 3.6V	–	–	8	
FIN maximum operating frequency 1 (SM5168A× series)	f_{max1}	300mVp-p sine wave. Note 3.	V_{DD} = 2.7V	200	–	–	MHz
XIN maximum operating frequency 1 (SM5168A× series)	f_{max2}	300mVp-p sine wave Note 3.	V_{DD} = 2.7V	20	–	–	MHz
FIN maximum operating frequency 2 (SM5168C× series)	f_{max1}	300mVp-p sine wave Note 3.	V_{DD} = 2.7V	340	–	–	MHz
XIN maximum operating frequency 2 (SM5168C× series)	f_{max2}	300mVp-p sine wave Note 3.	V_{DD} = 2.7V	20	–	–	MHz
FIN minimum operating input frequency	f_{min}	300mVp-p sine wave Note 3.	V_{DD} = 3.6V	–	–	10	MHz
FIN AC-coupled input voltage range	V_{AC1}	340MHz	V_{DD} = 2.7V	0.3	–	–	Vp-p
XIN AC-coupled input voltage range	V_{AC2}	20MHz	V_{DD} = 2.7V	0.3	–	–	Vp-p
OPR, TR LOW-level input voltage	V_{IL}		V_{DD} = 2.7V	–	–	0.3	V
OPR, TR HIGH-level input voltage	V_{IH}		V_{DD} = 2.7V	V_{DD} – 0.3	–	–	V
XIN LOW-level input current	I_{IL1}	V_{IN} = 0V	V_{DD} = 3.6V	–	–	50	µA
FIN LOW-level input current	I_{IL2}	V_{IN} = 0V	V_{DD} = 3.6V	–	–	50	µA
XIN HIGH-level input current	I_{IH1}	V_{IN} = V_{DD}	V_{DD} = 3.6V	–	–	50	µA
FIN HIGH-level input current	I_{IH2}	V_{IN} = V_{DD}	V_{DD} = 3.6V	–	–	50	µA
OPR, TR LOW-level input leakage current	I_{LL}	V_{IN} = 0V	V_{DD} = 3.6V	–	–	100	nA
OPR, TR HIGH-level input leakage current	I_{LH}	V_{IN} = V_{DD}	V_{DD} = 3.6V	–	–	100	nA
DO, LD LOW-level output voltage	V_{OL}	I_{OL} = 0.25mA	V_{DD} = 2.7V	–	–	0.4	V
DO, LD HIGH-level output voltage	V_{OH}	I_{OH} = 0.25mA	V_{DD} = 2.7V	V_{DD} – 0.4	–	–	V
DO, LD LOW-level output current	I_{OL}	V_{OL} = 0.4V	V_{DD} = 2.7V	0.25	–	–	mA
DO, LD HIGH-level output current	I_{OH}	V_{OH} = V_{DD} – 0.4V	V_{DD} = 2.7V	0.25	–	–	mA
DO three-state output high-impedance leakage current	I_{OZL}	V_{OL} = 0V	V_{DD} = 3.6V	–	–	100	nA
	I_{OZH}	V_{OH} = V_{DD}	V_{DD} = 3.6V	–	–	100	nA

Note 1. f_{FIN} = 200MHz (300mVp-p sine wave), f_{XIN} = 20MHz (300mVp-p sine wave), TR = HIGH
Note 2. f_{FIN} = 340MHz (300mVp-p sine wave), f_{XIN} = 20MHz (300mVp-p sine wave), TR = HIGH
Note 3. Signal generator AC-coupled input with 50Ω termination.

FUNCTIONAL DESCRIPTION

SM5168A× series

Frequency dividers

The comparator frequency divider (N-counter) and reference frequency divider (R-counter), one of each, are set in master-slice to the following values.

- Comparator frequency divider (N-counter) = 272 to 65535
- Reference frequency divider (R-counter) = 5 to 65535

Standby mode

When OPR goes from HIGH to LOW, the PLL is in standby mode with the following input/output conditions.

Block	State
Input FIN	LOW level
Comparator frequency divider (N-counter)	Stopped
Input XIN	LOW level
Reference frequency divider (R-counter)	Stopped
Phase comparator	Reset
Output DO	Floating
Output LD	LOW-level

When OPR goes from LOW to HIGH, standby mode is released and the PLL is in operating mode, and the following start-up sequence is executed.

Internal feedback resistance is connected to XIN to activate the reference frequency divider (R-counter).
Internal feedback resistance is connected to FIN.
The comparator frequency divider (N-counter) and the phase comparator are reset.
DO is floating and LD is LOW.

↓

Reference frequency divider (R-counter) starts to perform frequency division.
An internal signal (FR signal) is output on the 2nd clock cycle.

↓

Phase comparator starts and comparator frequency divider (N-counter) starts to perform frequency division.
DO floating condition is released and LD goes HIGH.

SM5168C× series

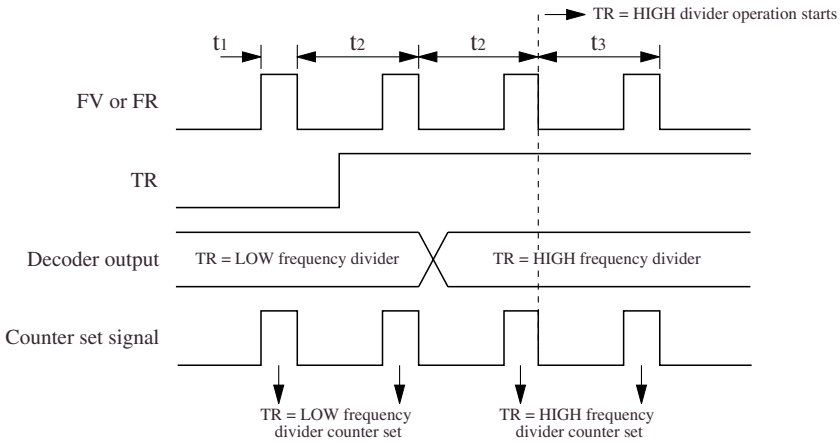
Frequency Dividers

The comparator frequency divider (N-counter) and reference frequency divider (R-counter), with 2 sets of comparator frequency divider and reference frequency divider ratios, are set in master-slice. The frequency divider set selected is determined by the state of TR (pin 5). The ratio ranges are the same when TR is HIGH or LOW, and are:

- Comparator frequency divider (N-counter) = 272 to 65535
- Reference frequency divider (R-counter) = 5 to 65535

Frequency Divider Switching

When switching the frequency dividers using TR, the dividers switch in sync with the R-counter divider signal (FR) and the N-counter divider signal (FV) to minimize any disturbance in the PLL loop.



If t_F represents the FIN cycle time:
$t_1 = 48t_F$
t_2 = (divider ratio when TR = LOW) × t_F
t_3 = (divider ratio when TR = HIGH) × t_F

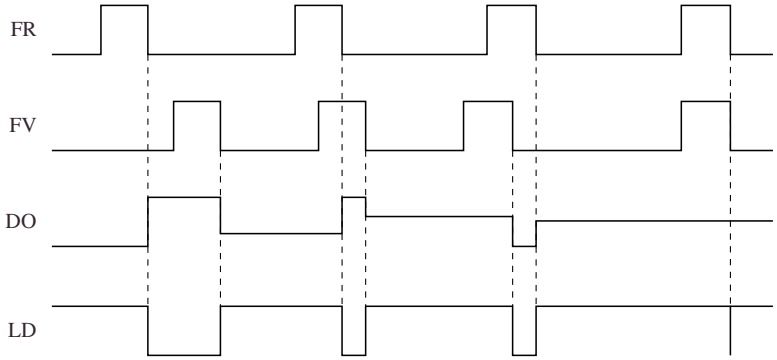
If t_X represents the XIN cycle time:
$t_1 = 3t_X$
t_2 = (divider ratio when TR = LOW) × t_X
t_3 = (divider ratio when TR = HIGH) × t_X

Both the R-counter and N-counter are configured with presettable counters. The divider outputs (FR and FV) are then input to the phase comparator which performs phase comparison on the falling edge of each signal. The FR/FV signals also function as the R/N-counter preset strobe signals, respectively. Consequently, when the TR signal level switches, the decoder output changes on the first FR/FV (R/N-counter preset strobe) signal and the counters are set in the new frequency dividers on the second FR/FV (R/N-counter preset strobe) signal. Frequency division with the new frequency dividers starts on the falling edge of the second FR/FV (R/N-counter preset strobe) signal.

The timing in the diagram shows an example when TR goes from LOW to HIGH only, but the timing operation is identical under the reverse transition. The R/N-counters operate with the same timing, although the N-counter has a dual modulus prescaler in the initial-stage which means the HIGH-level pulsewidth of the FV and FR signals is different.

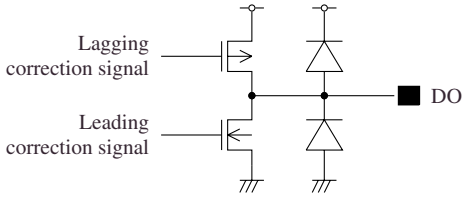
DO Output Timing

The phase comparator error signal charge pump signal is output on DO with polarity for connection to an external passive filter. The signals compared are FV and FR, which are the internal comparator frequency divider output signal and reference frequency divider output signal, respectively. The timing is shown in the following figure.

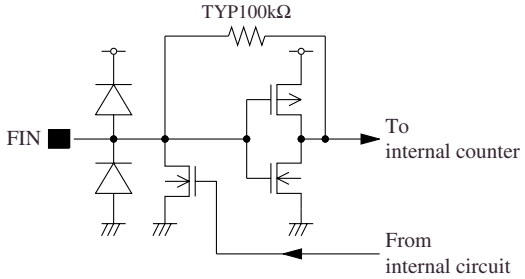


INPUT/OUTPUT EQUIVALENT CIRCUITS

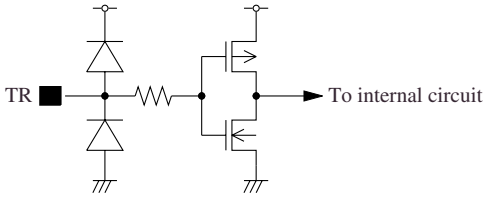
DO



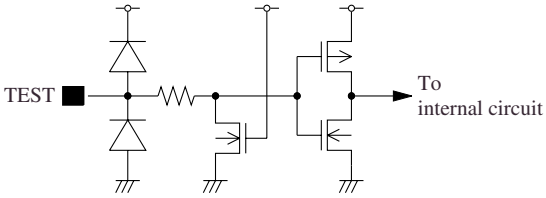
FIN



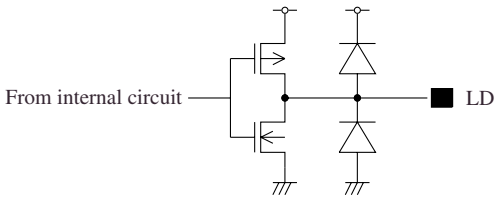
TR



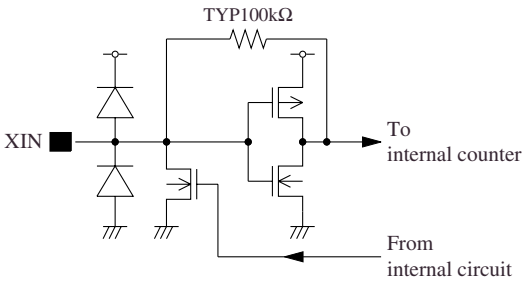
TEST



LD



XIN



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