250 mW Power Amplifier with T/R and Diversity Switches 2.4 - 2.5 GHz

AM55-0003

Features

- Highly Integrated Power Amplifier With T/R and Diversity Switches
- Operates Over 2.7 V to 6 V Supply Voltage
- High Linear Output Power (P_{1dB}: +24 dBm)
- Individual Gate Control for Each Amplifier Stage
- Low Cost SSOP-28 Plastic Package

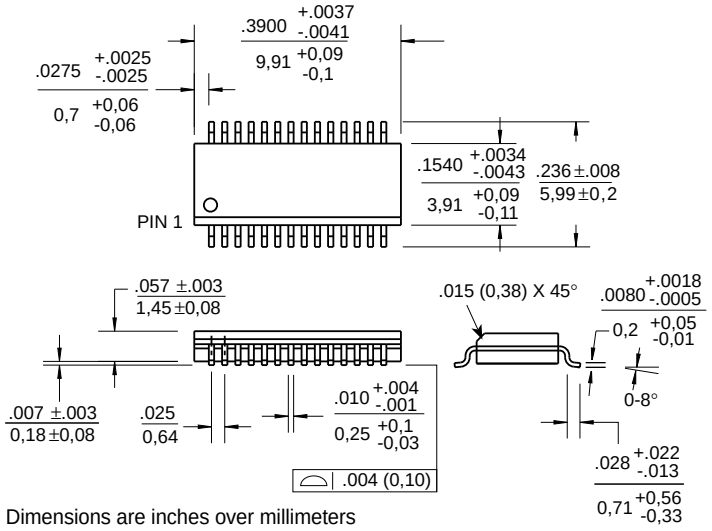
Description

M/A-COM's AM55-0003 is a GaAs power amplifier with integrated transmit/receive and an antenna diversity switch in a low cost SSOP 28 plastic package. The power amplifier delivers +24 dBm of linear power with high efficiency and can be operated with voltages as low as 2.7 volts. The power amplifier switch is fully monolithic. The T/R and diversity switches achieve good insertion loss and isolation without degrading the overall linearity. The switches can be controlled with CMOS logic levels.

The AM55-0003 is ideally suited for QPSK, BPSK or other linearly modulated systems in the 2.4 GHz ISM frequency band. It can also be used in GFSK systems where levels of +25 dBm are required. Typical applications include WLAN and wireless portable data collection. This power amplifier can be combined with a transceiver IC (MD58-0001 or MD58-0002) to form a complete RF front end.

M/A-COM's AM55-0003 is fabricated using a mature 0.5-micron gate length GaAs process. The process features full passivation for increased performance and reliability.

SSOP-28



Dimensions are inches over millimeters

Ordering Information

Part Number	Description
AM55-0003	SSOP 28-Lead Plastic Package
AM55-0003TR	Forward Tape & Reel*
AM55-0003RTR	Reverse Tape & Reel*
AM55-0003SMB	Designer's Kit

* If specific reel size is required, consult factory for part number assignment.

Typical Electrical Specifications

Test Conditions: Frequency: 2.45 GHz, $V_{DD1,2,3}$ = 5 V±5%, V_{G1} adjusted for 20 mA quiescent bias on V_{DD1}, V_{G2} adjusted for 70 mA quiescent bias on V_{DD2}, V_{G3} adjusted for 90 mA quiescent bias on V_{DD3}, T_A = +25°C

Parameter	Units	Min.	Typ.	Max.
Power Amplifier				
Linear Gain	dB	24	28	32
VSWR In/Out			1.75:1	
Output Power @ P_{1dB}	dBm	22.5	24.5	
Second Harmonic @ P_{1dB}	dBc		-20	0
Third Harmonic @ P_{1dB}	dBc		-30	-10
I_{DD} @ P_{1dB} (V_{DD1} + V_{DD2} + V_{DD3})	mA		270	375
T/R and Diversity Switches				
Insertion Loss	dB		1.2	
Isolation	dB	10	12	
VSWR In/Out			1.5:1	

Pin Configuration

Pin No.	Pin Name	Description
1	ANT CTRL	Antenna selection: Select ANT 1 (0V) or ANT 2 (+5 V)
2	ANT COMMON	Common Port of Diversity Switch
3	GND	DC and RF Ground
4	ANT 1	Output #1 of Diversity Switch
5	GND	DC and RF Ground
6	ANT 2	Output #2 of Diversity Switch
7	GND	DC and RF Ground
8	RX OUT	Output of T/R Switch for receive mode
9	V_{G2}	Negative bias control for the second PA stage, adjusted to set V_{DD2} quiescent bias current, which is typically 70 mA. Typical voltage at pin = -0.55 V Input impedance: > 1 MΩ
10	GND	DC and RF Ground
11	V_{DD1}	Positive bias for the first stage of the PA, 2.7 to 6 volts
12	GND	DC and RF Ground
13	GND	DC and RF Ground
14	V_{G1}	Negative bias control for the first PA stage, adjusted to set V_{DD1} quiescent bias current, which is typically 20 mA. Typical voltage at pin = -0.75 V Input impedance: > 1 MΩ
15	RF IN	RF Input of the Power Amplifier
16	GND	DC and RF Ground
17	V_{G3}	Negative bias control for the third PA stage, adjusted to set V_{DD3} quiescent bias current, which is typically 90 mA. Typical voltage at pin = -0.95 V Input impedance: > 1 MΩ
18	V_{DD2}	Positive bias for the second stage of the PA, 2.7 to 6 volts
19	GND	DC and RF Ground
20	GND	DC and RF Ground
21	GND	DC and RF Ground
22	GND	DC and RF Ground
23	V_{DD3}	Positive bias for the third stage of the PA, 2.7 to 6 volts
24	GND	DC and RF Ground
25	RF OUT	RF output of T/R switch and power amplifier for transmit mode
26	T/R CTRL	0 V for transmit mode, +5 V for receive mode
27	V_{DD} TR	V_{DD} for T/R switch
28	V_{DD} ANT	V_{DD} for Diversity Switch

Absolute Maximum Ratings[1]

Parameter	Absolute Maximum
Max. Input Power[2]	+23 dBm
Operating Voltages[2,3]	V_{DD} = 8 V V_{GG} = -8 V
Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +150°C

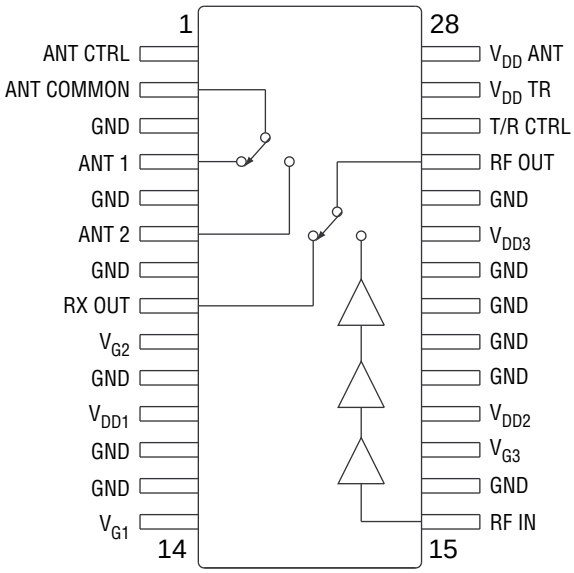
1. Exceeding these limits may cause permanent damage.
2. Ambient temperature (T_A) = +25°C
3. $|V_{DD}| + |V_{GG}|$ not to exceed 12 volts.

Truth Table

Control Line		Operating Mode
ANT CTRL	T/R CTRL	
X	1	Receive
X	0	Transmit
0	X	ANT 1
1	X	ANT 2

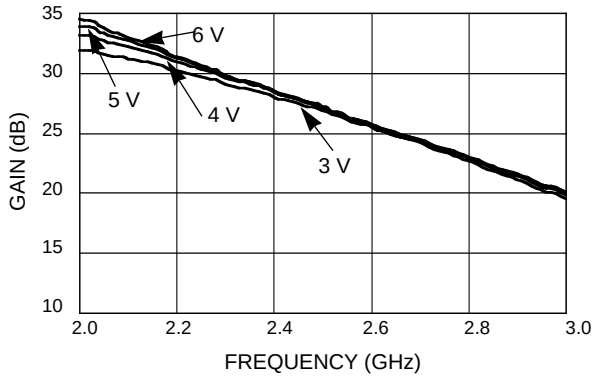
X - Don't Care
"0" = 0 V to 0.2 V @ 100 µA
"1" = V_{DD} to V_{DD} - 0.2 V @ 200 µA

Functional Diagram and Pin Configuration

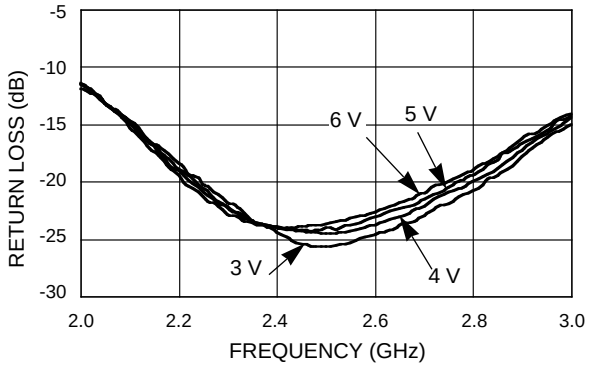


Power Amplifier Small Signal Performance[1]

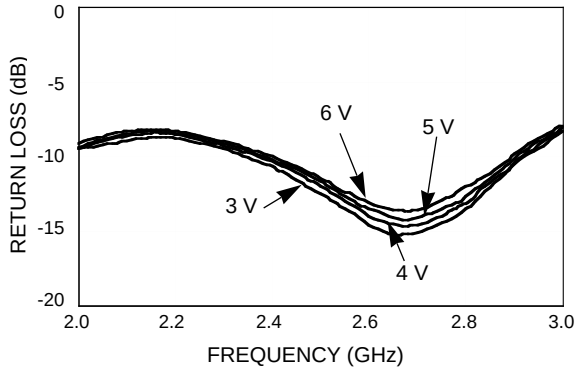
LINEAR GAIN, $V_{DD1} = V_{DD2} = V_{DD3}$



INPUT MATCH

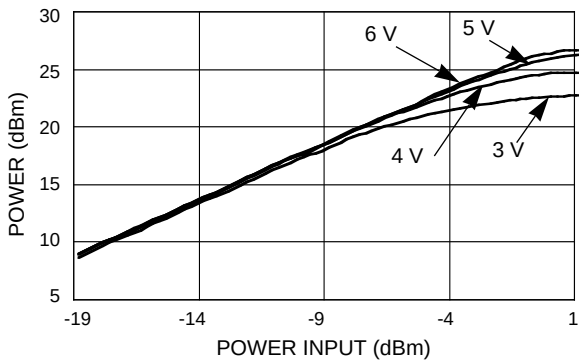


OUTPUT MATCH

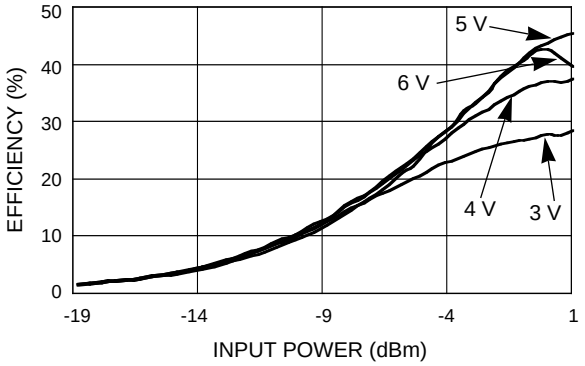


Power Amplifier CW Performance at Various Supply Voltages[1]

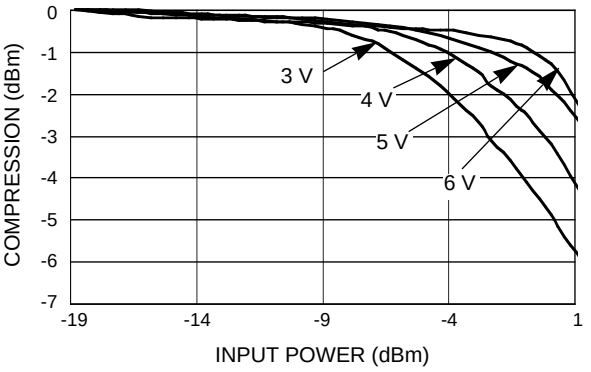
POWER OUTPUT @ 2.45 GHz, $V_{DD1} = V_{DD2} = V_{DD3}$



POWER ADDED EFFICIENCY (%)
@ 2.45 GHz, $V_{DD1} = V_{DD2} = V_{DD3}$



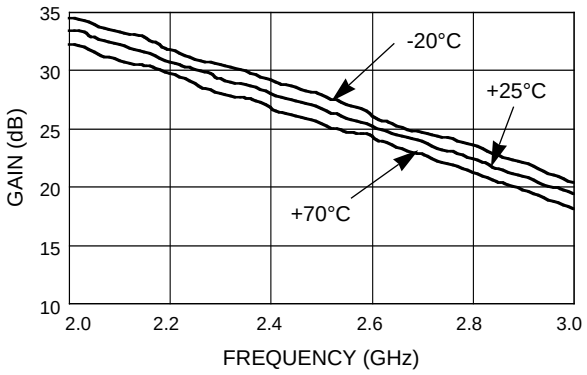
GAIN COMPRESSION @ 2.45 GHz, $V_{DD1} = V_{DD2} = V_{DD3}$



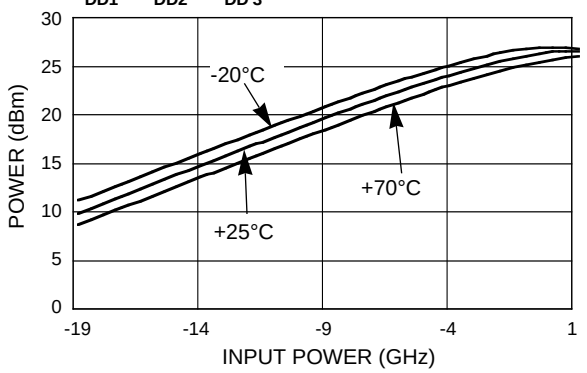
1. All data measured at T_A = +25°C and V_{G1}, V_{G2} and V_{G3} adjusted for first stage quiescent current of 20 mA, second stage current of 70 mA and third stage current of 90 mA, respectively.

Power Amplifier Temperature Performance[1]

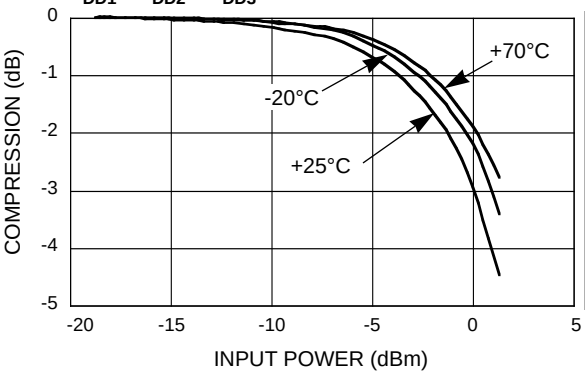
LINEAR GAIN, $V_{DD1} = V_{DD2} = V_{DD\,3} = +5$ V



POWER OUTPUT @ 2.45 GHz,
$V_{DD1} = V_{DD2} = V_{DD\,3} = +5$ V

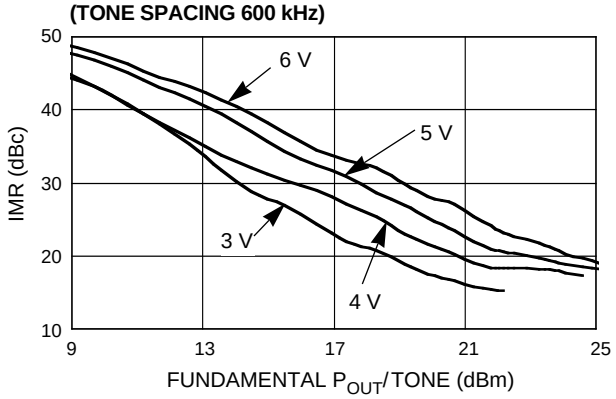


GAIN COMPRESSION @ 2.45 GHz,
$V_{DD1} = V_{DD2} = V_{DD3} = +5$ V

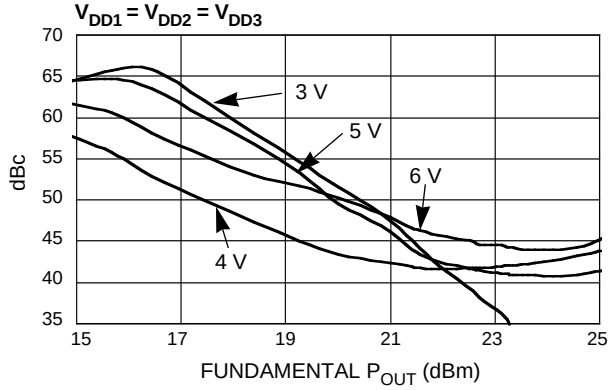


Power Amplifier Spurious Response at Various Supply Voltages[1]

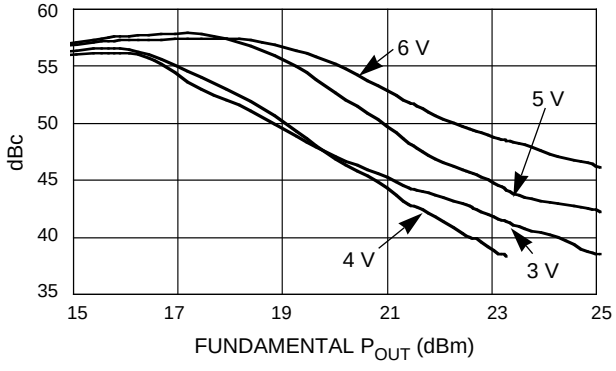
THIRD ORDER INTERMODULATION RATIO@ 2.45 GHz, (TONE SPACING 600 kHz)



SECOND HARMONIC RATIO @ 2.45 GHz,
$V_{DD1} = V_{DD2} = V_{DD3}$



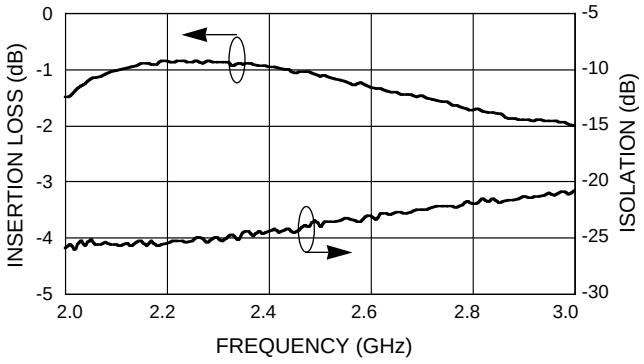
THIRD HARMONIC RATIO @ 2.45 GHz,
$V_{DD1} = V_{DD2} = V_{DD\,3}$



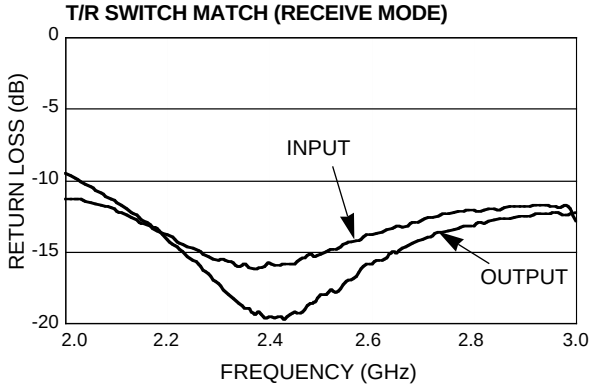
1. All data measured at T_A = +25°C and V_{G1}, V_{G2} and V_{G3} adjusted for first stage quiescent current of 20 mA, second stage current of 70 mA and third stage current of 90 mA, respectively.

Transmit/Receive Switch Performance[1]

T/R INSERTION LOSS/ISOLATION (RECEIVE MODE)

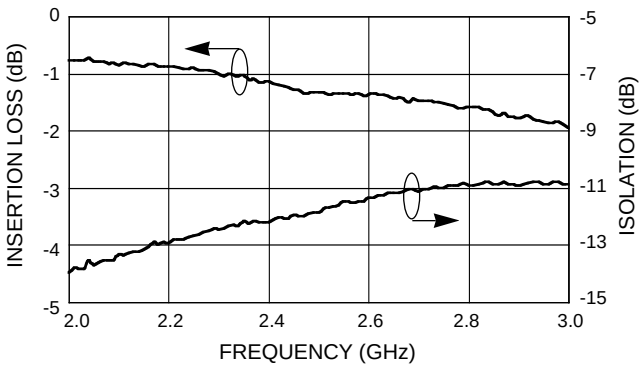


T/R SWITCH MATCH (RECEIVE MODE)

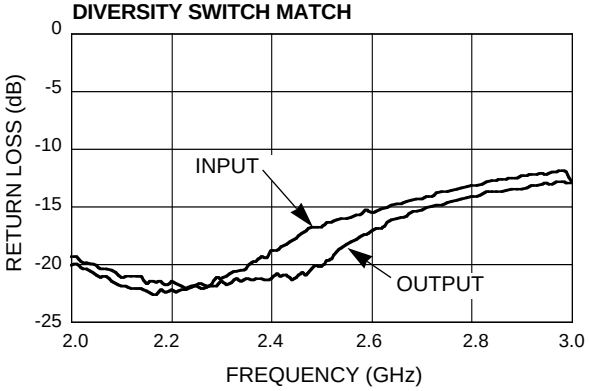


Diversity Switch Performance[1]

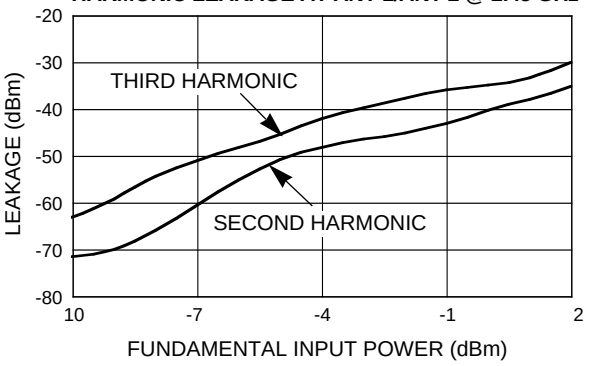
DIVERSITY SWITCH INSERTION LOSS/ISOLATION



DIVERSITY SWITCH MATCH



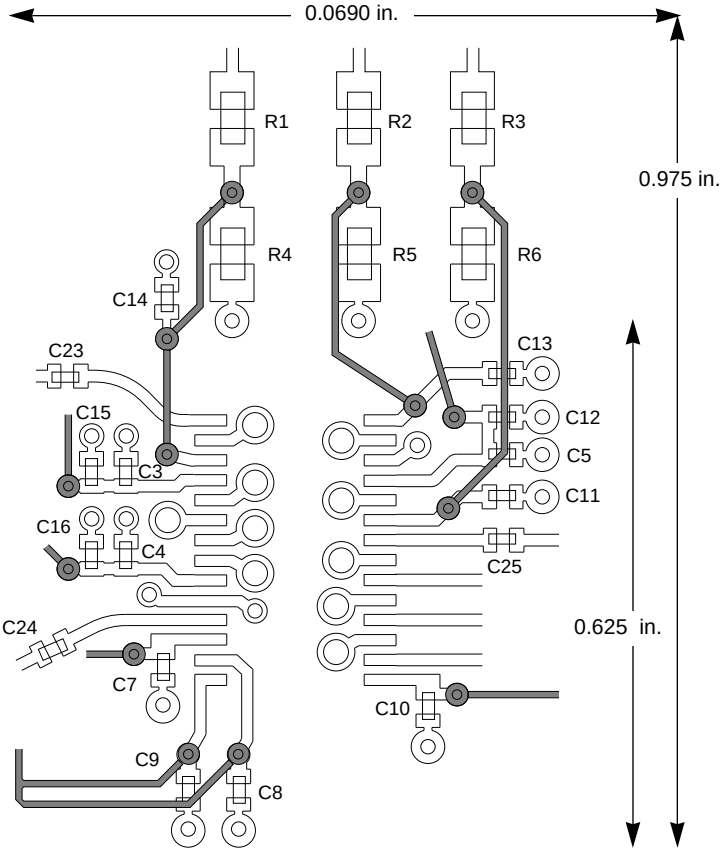
HARMONIC LEAKAGE AT ANT 1/ANT 2 @ 2.45 GHz[2]



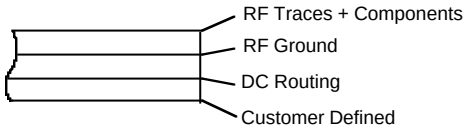
1. All data measured with V_{DD} TR = V_{DD} ANT = +5 V, T_A = +25°C.
2. Measured at 2.45 GHz at RF IN. Output measured at ANT 1 or ANT 2, with RF OUT and ANT COMMON terminated in 50 Ω.

Recommended PCB Configuration

Layout View



Cross-Section View



The PCB dielectric between RF traces and RF ground layers should be chosen to reduce RF discontinuities between 50-Ω lines and package pins. M/A-COM recommends an FR-4 dielectric thickness of 0.008 in. (0.2 mm), yielding a 50-Ω line width of 0.015 in. (0.38 mm). The recommended metalization thickness is 1 oz. copper.

Shaded traces are vias to DC routing layer and traces on DC routing layer.

Biasing Procedure

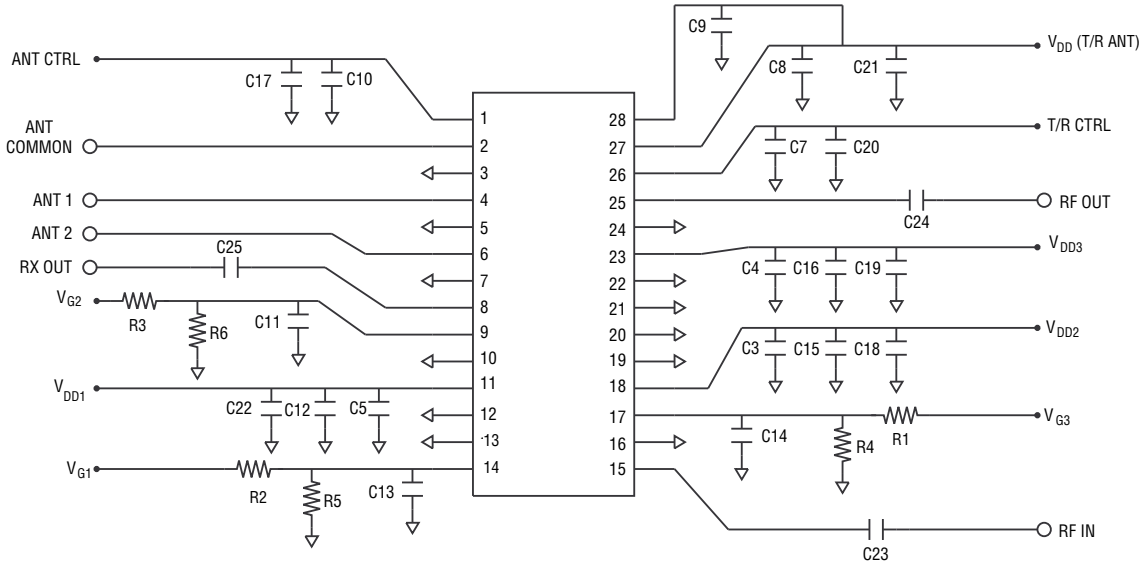
The AM55-0003 requires that V_{GG} bias be applied prior to ***any*** V_{DD} bias. Permanent damage may occur if this procedure is not followed. All FETs in the PA will draw excessive current and damage internal circuitry.

External Circuitry Parts List

Label	Value	Purpose
C1 - C6	22 pF	Bypass (GHz)
C23 - C24	22 pF	DC Block
C7 - C16	1000 pF	Bypass (MHz)
C17 - C22	0.01 µF	Bypass (kHz)
R1, R6	1.5 kΩ	FET Gate Divider Network
R3, R5	5 kΩ	
R2	12 kΩ	
R4	1 kΩ	

All off-chip components are low-cost surface mount components obtainable from multiple sources. (0.020 in. x 0.040 in. or 0.030 in. x 0.050 in.)

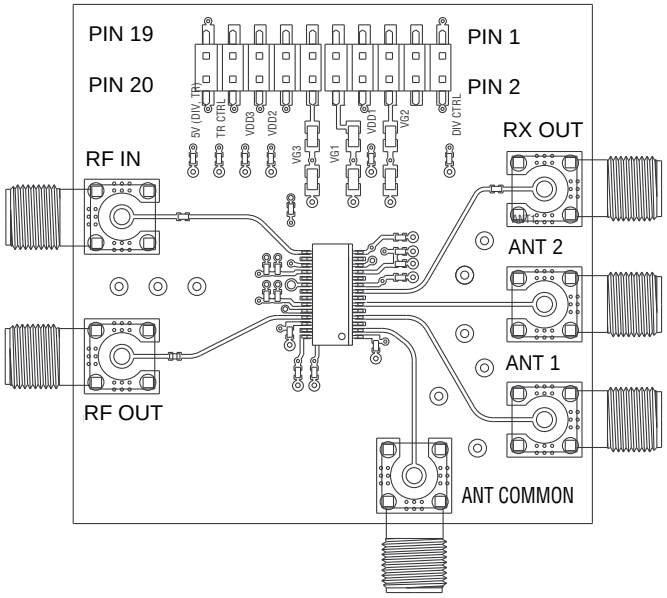
External Circuitry



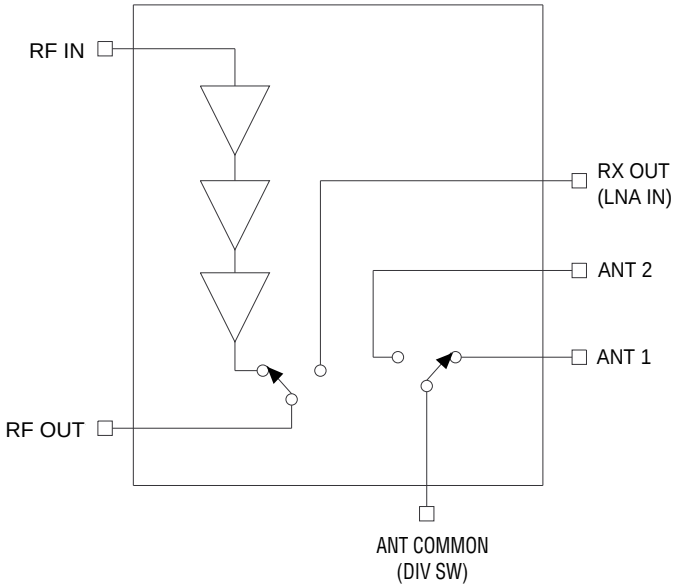
Designer's Kit (AM55-0003SMB)

The AM55-0003SMB Designer's Kit allows for immediate evaluation of M/A-COM's AM55-0003 integrated power amplifier with T/R and diversity switches. The evaluation board consists of an AM55-0003, recommended external surface mount circuitry, RF connectors and a DC multi-pin connector, all mounted to a multi-layer FR-4 PCB. Other items included in the Designer's Kit: a floppy disk (with typical performance data and a .DXF file of the recommended PCB layout) and any additional Application Notes. The AM55-0003SMB evaluation PCB and block diagram are illustrated below with all functional ports labeled.

P/A Switch Sample Board



Functional Block Diagram



DC Connector Pinout

PCB DC Connector	Function	Device Pin Number
1	GND	N/C
2	ANT CTRL (0 V/ +5 V)	1
3	N/C	N/C
4	N/C	N/C
5	N/C	N/C
6	V_{G2}	9
7	VSW	N/C
8	V_{DD1} (+5 V)	11
9	N/C	N/C
10	V_{G1}	14

PCB DC Connector	Function	Device Pin Number
11	N/C	N/C
12	V_{G3}	17
13	N/C	N/C
14	V_{DD2} (+5 V)	18
15	N/C	N/C
16	V_{DD3} (+5 V)	23
17	N/C	N/C
18	T/R CTRL (0 V/ +5 V)	8
19	GND	N/C
20	V_{DD} TR, V_{DD} ANT(+5 V)	27, 28

AM55-0003SMB Biasing Procedure

In order to prevent transients which may damage the MMIC, please adhere to the following procedure.

- Turn on all power supplies and set all voltages to 0 volts BEFORE connecting the power supplies to the DC connector.
- Apply a -5.0 volt supply to DC connector pin 10 (V_{G1}).
- Apply a -5.0 volt supply to DC connector pin 6 (V_{G2}).
- Apply a -5.0 volt supply to DC connector pin 12 (V_{G3}).
- Apply a +5.0 volt supply to the DC connector pin 20 (V_{DD} TR, V_{DD} ANT).
- Apply a +5.0 volt supply to the DC connector pin 8 (V_{DD1}).
- Apply a +5.0 volt supply to the DC connector pin 14 (V_{DD2}).
- Apply a +5.0 volt supply to the DC connector pin 16 (V_{DD3}).
- Apply a GND or +5.0 volt supply to the DC connector pin 18 (T/R CTRL, see truth table for desired mode).
- Apply a GND or +5.0 volt supply to the DC connector pin 2 (ANT CTRL, see truth table for desired mode).
- Adjust V_{G1}, V_{G2}, V_{G3} supplies to -5 volts.
- Adjust all V_{DD} supplies to +5 volts.
- Adjust V_{G1} supply for desired V_{DD1} quiescent current (typically 20 mA, V_{G1} nominally -2.5 volts).
- Adjust V_{G2} supply for desired V_{DD2} quiescent current (typically 70 mA, V_{G2} nominally -2.5 volts).
- Adjust V_{G3} supply for desired V_{DD3} quiescent current (typically 90 mA, V_{G3} nominally -2.5 volts).
- To power off, reverse above procedure.
  1) Set all V_{DD} lines to 0 volts.
  2) Set V_{G1}, V_{G2} and V_{G3} to 0 volts.
  3) Disconnect bias lines from DC connector.
  4) Turn off power supplies.

Evaluation PCB and RF Connector Losses

Port Reference	Loss (dB)
RF IN	0.25
RF OUT	0.25
RX OUT (LNA IN)	0.25
ANT COMMON (DIV SW)	0.25
ANT 1	0.25
ANT 2	0.25

The DC connector on the Designer's Kit PCB allows selection of all the device's operating modes. It is accomplished by one or more of the following methods.

1. A mating female multi-pin connector (Newark Electronics Stock #46F-4658, not included)
2. Wires soldered to the necessary pins (not included)
3. Clip leads (not included)
4. A combination of clip leads or wires and jumpers (jumpers included as required)