$\div$1/$\div$2 DIFFERENTIAL-TO-LVDS CLOCK GENERATOR

ICS87421I

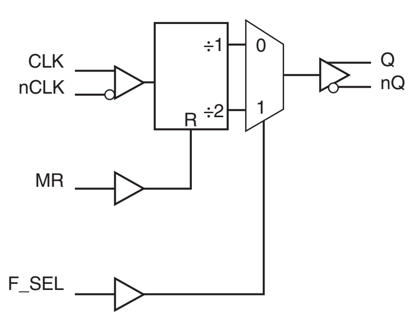
GENERAL DESCRIPTION

The ICS87421I is a high performance ÷1/÷2 Differential-to-LVDS Clock Generator and a member of the HiPerClockS™ family of High Performance Clock Solutions from IDT. The CLK, nCLK pair can accept most standard differential input levels. The ICS87421I is characterized to operate from a 3.3V power supply. Guaranteed part-to-part skew characteristics make the ICS87421I ideal for those clock distribution applications demanding well defined performance and repeatability.

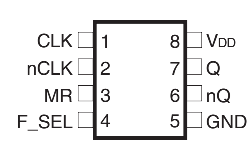
FEATURES

- One differential LVDS output
- One differential CLK, nCLK input pair
- CLK, nCLK pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- Maximum clock input frequency: 1GHz
- Translates any single ended input signal (LVCMOS, LVTTL, GTL) to LVDS levels with resistor bias on nCLK input
- Part-to-part skew: 500ps (maximum)
- Propagation delay: 1.7ns (maximum)
- Additive phase jitter, RMS @ 155.52MHz: 0.17ps (typical)
- Full 3.3V operating supply
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS87421I

8-Lead SOIC

3.90mm x 4.90mm x 1.37mm package body

M Package

Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	CLK	Input	Pulldown	Non-inverting differential clock input.
2	nCLK	Input	Pullup	Inverting differential clock input.
3	MR	Input	Pulldown	Active High Master Reset. When logic HIGH, the internal dividers are reset causing the true output (Q) to go low and the inverted output (nQ) to go high. When logic LOW, the internal dividers and the output are enabled. LVCMOS / LVTTL interface levels. See Table 3.
4	F_SEL	Input	Pulldown	Selects divider value for Q, nQ outputs as described in Table 3. LVCMOS / LVTTL interface levels.
5	GND	Power		Power supply ground.
6, 7	Q, nQ	Output		Differential output pair. LVDS interface levels.
8	V_{DD}	Power		Positive supply pin.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

TABLE 3. FUNCTION TABLE

MR	F_SEL	Divide Value
1	X	Reset: Q output low, nQ output high
0	0	÷1
0	1	÷2

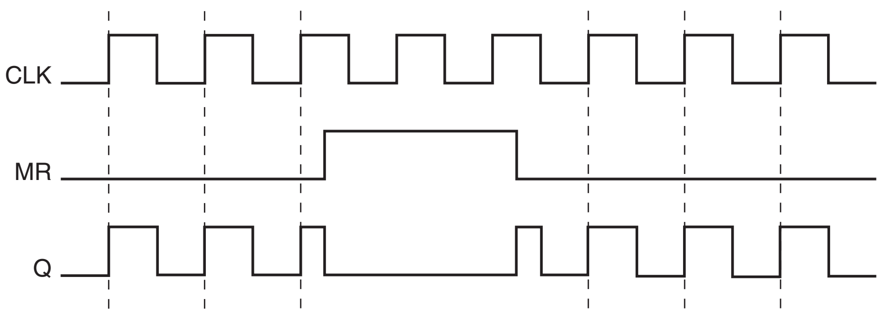


FIGURE 1A. ÷1 CONFIGURATION TIMING DIAGRAM

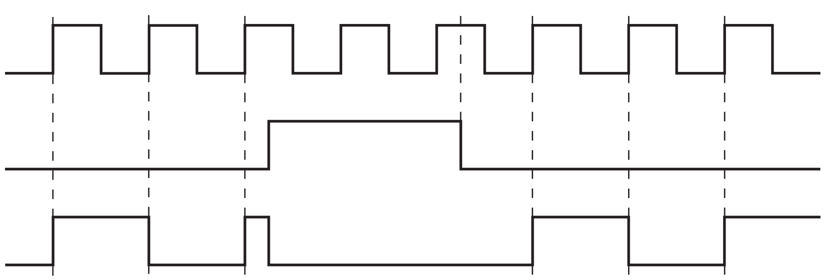


FIGURE 1B. ÷2 CONFIGURATION TIMING DIAGRAM

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, I_O	
Continuous Current	10mA
Surge Current	15mA
Package Thermal Impedance, θ_{JA}	96°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, V_{DD} = 3.3V±5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current			55		mA

TABLE 4B. LVCMOS/LVTTL DC CHARACTERISTICS, V_{DD} = 3.3V±5%, TA = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			1.37		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.7	V
I_{IH}	Input High Current	MR, F_SEL	$V_{DD} = V_{IN}$ = 3.465V			150	µA
I_{IL}	Input Low Current	MR, F_SEL	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA

TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS, V_{DD} = 3.3V±5%, TA = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK	$V_{DD} = V_{IN}$ = 3.465V			150	µA
		nCLK	$V_{DD} = V_{IN}$ = 3.465V			5	µA
I_{IL}	Input Low Current	CLK	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		nCLK	V_{DD}= 3.465V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1			GND + 0.5		V_{DD} - 0.85	V

NOTE 1: Common mode voltage is defined as V_{IH}.

TABLE 4D. LVDS DC CHARACTERISTICS, V_{DD} = 3.3V±5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		350	470	540	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.1	1.25	1.4	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

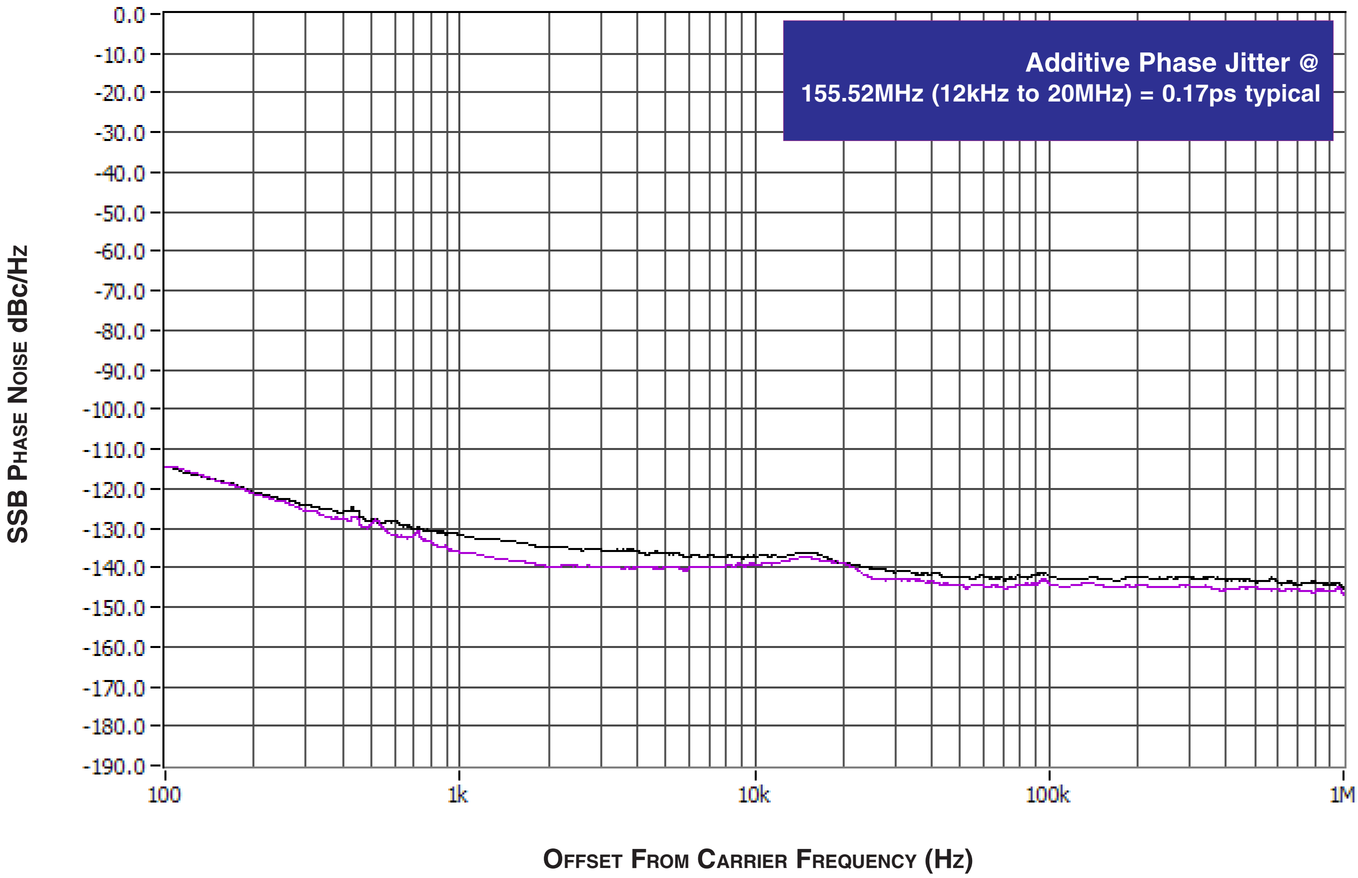
TABLE 5. AC CHARACTERISTICS, V_{DD} = 3.3V±5%, TA = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{CLK}	Clock Input Frequency					1	GHz
t_{PD}	Propagation Delay; NOTE 1	CLK to Q (Dif)		1.0		1.7	ns
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 3					500	ps
t_{JIT}	Additive Phase Noise, RMS; refer to Additive Phase Jitter Section		155.52MHz, Integration Range: 12kHz – 20MHz		0.17		ps
t_R / t_F	Output Rise/Fall Time		20% to 80%	150		500	ps
odc	Output Duty Cycle		f_{IN} < 500MHz	43		57	%

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

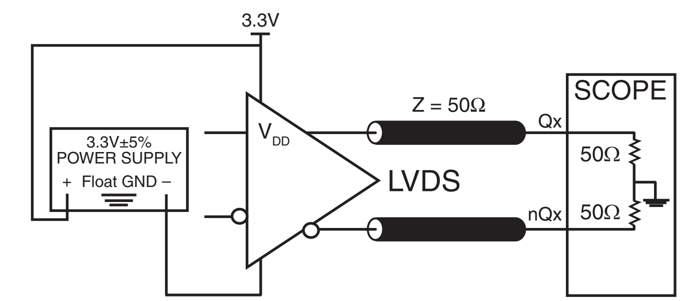
Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

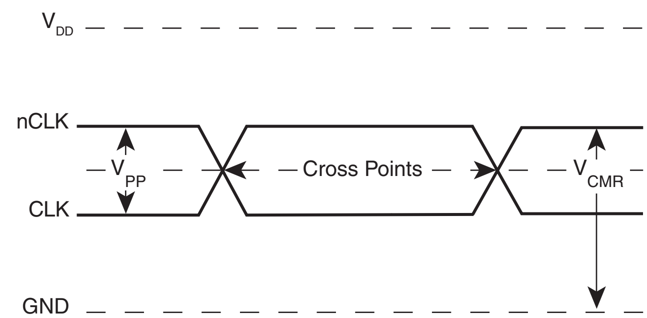


As with most timing specifications, phase noise measurements have issues. The primary issue relates to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependant on the input source and measurement equipment.

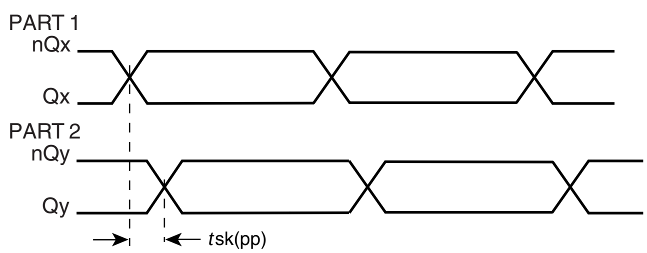
Parameter Measurement Information



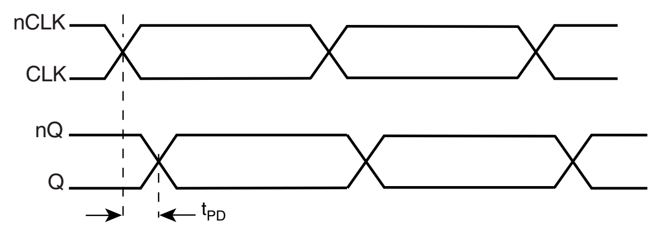
3.3V Output Load AC Test Circuit



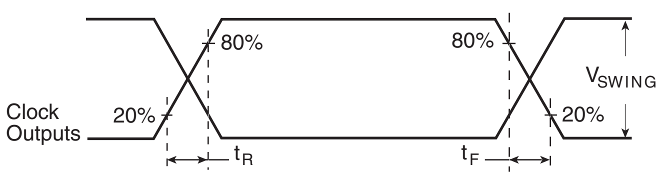
Differential Input Level



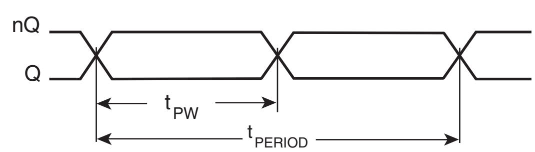
Part-to-Part Skew



Propagation Delay

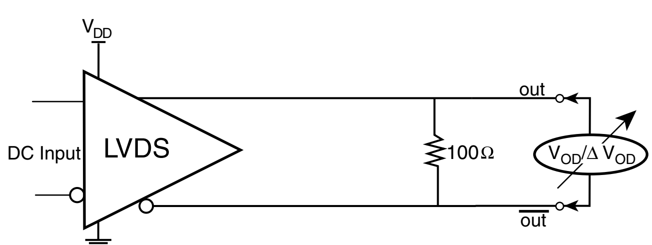


Output Rise/Fall Time

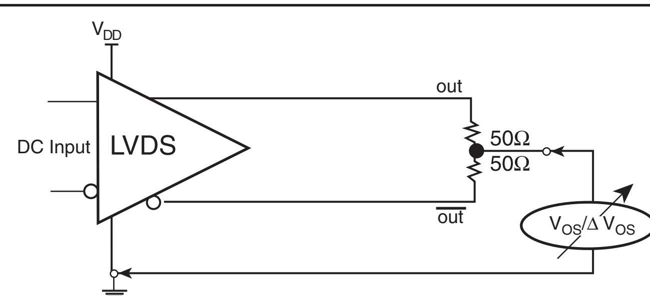


$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

Output Duty Cycle/Pulse Width/Period



Differential Output Voltage Setup



Offset Voltage Setup

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 2 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = $V_{DD}/2$ is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

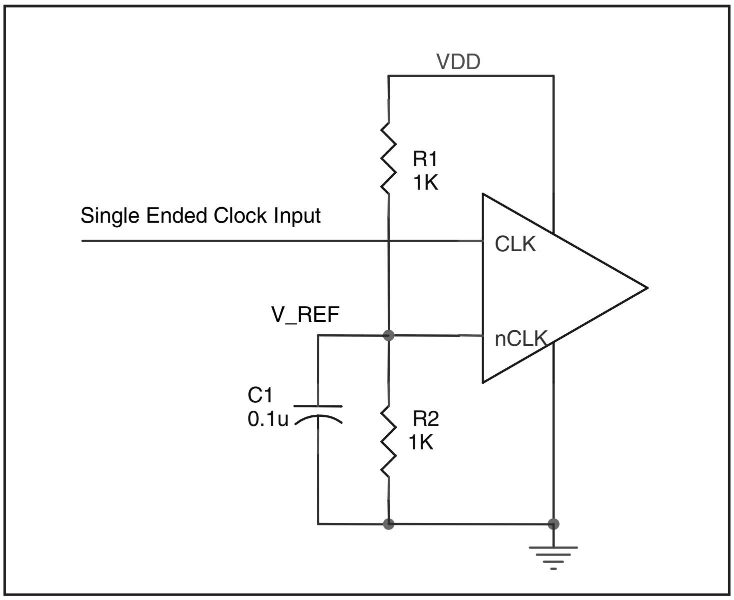


FIGURE 2. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

RECOMMENDATIONS FOR UNUSED INPUT PINS

INPUTS:

LVCMOS CONTROL PINS

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 3A to 3F* show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in Figure 3A, the input termination applies for IDT HiPerClockS open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

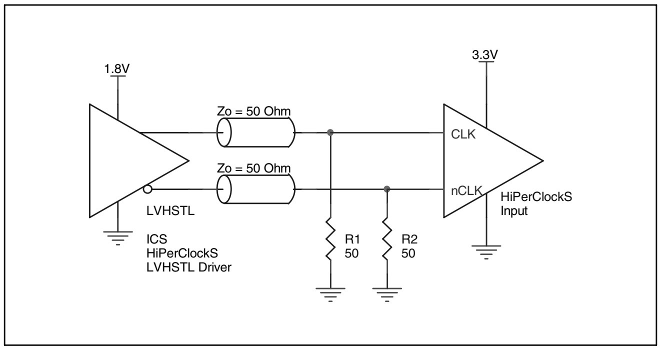


Figure 3A. HiPerClockS CLK/nCLK Input Driven by an IDT Open Emitter HiPerClockS LVHSTL Driver

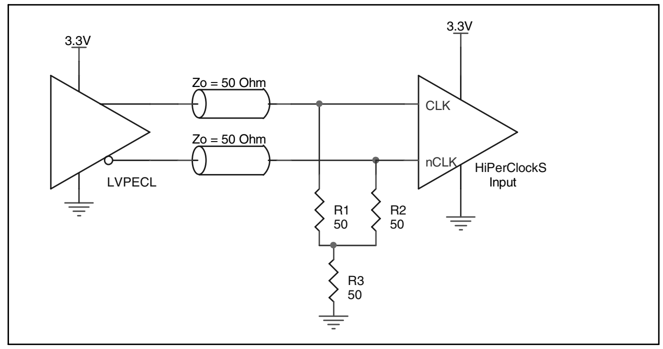


Figure 3B. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver

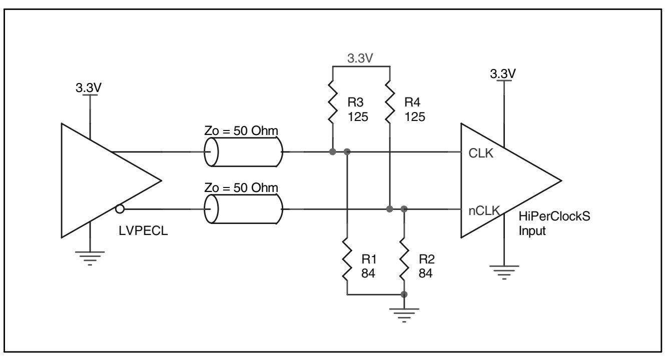


Figure 3C. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver

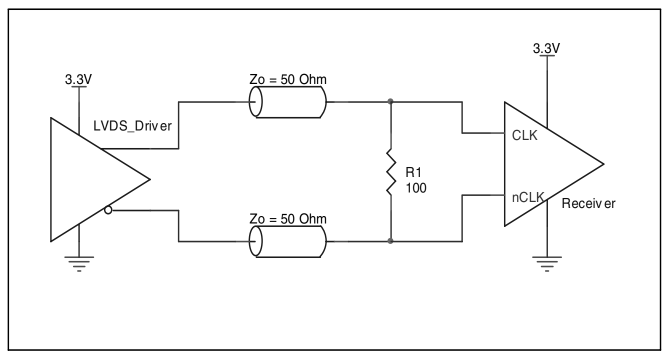


Figure 3D. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVDS Driver

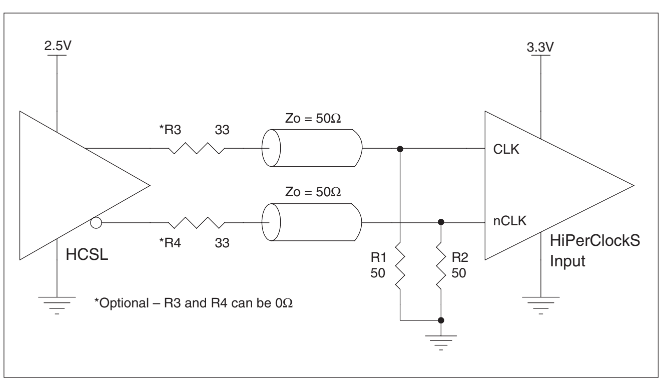


Figure 3E. HiPerClockS CLK/nCLK Input Driven by a 3.3V HCSL Driver

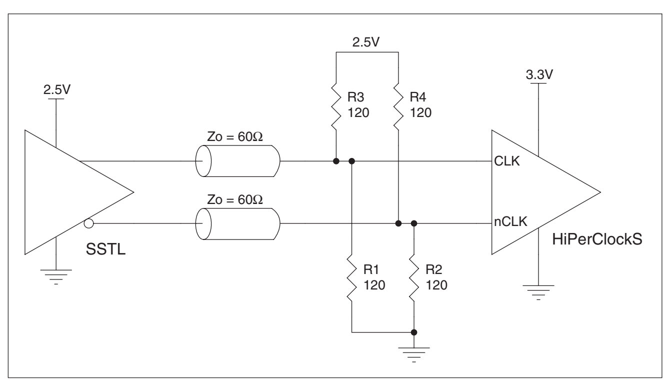


Figure 3F. HiPerClockS CLK/nCLK Input Driven by a 2.5V SSTL Driver

LVDS Driver Termination

A general LVDS interface is shown in *Figure 4.* In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

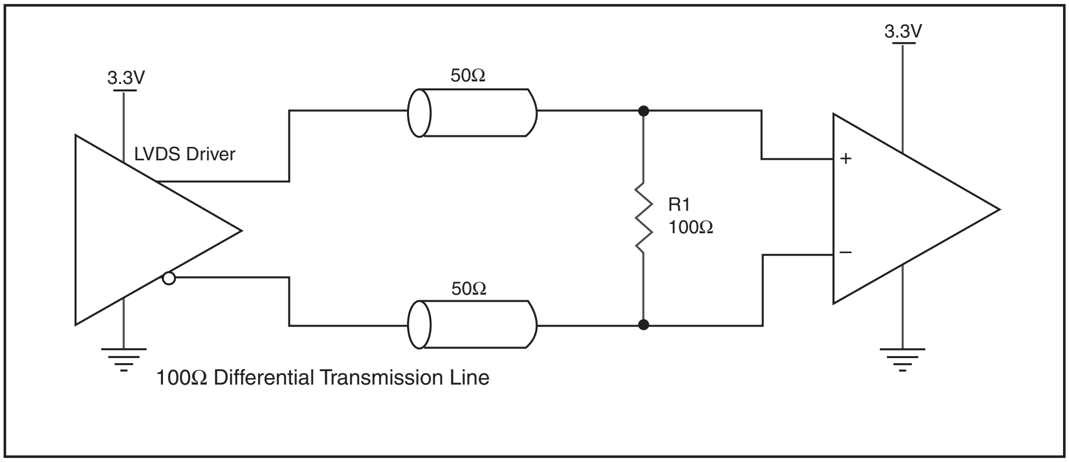


Figure 4. Typical LVDS Driver Termination

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS87421I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS87421I is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

- $Power\_{}_{MAX} = V_{DD\_MAX} * I_{DD\_MAX}$ = 3.465V * 55mA = **198.58mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 96°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
85°C + 0.199W * 96°C/W = 104.1°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 8-PIN SOIC, FORCED CONVECTION

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	96°C/W	87°C/W	82°C/W

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for 8 Lead SOIC

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	96°C/W	87°C/W	82°C/W

Transistor Count

The transistor count for ICS87421I is: 417

Package Outline - M Suffix for 8 Lead SOIC

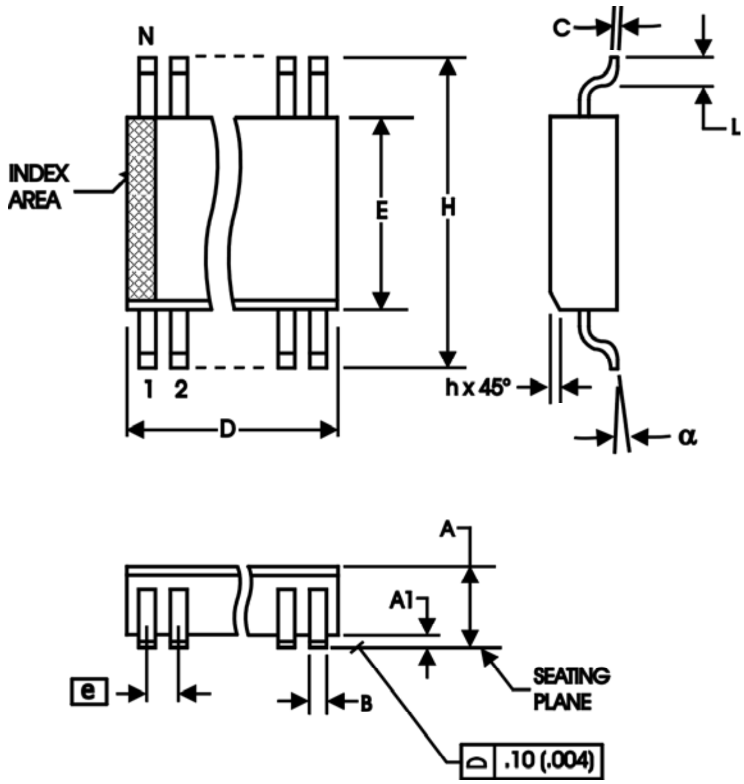


Table 8. Package Dimensions

SYMBOL	Millimeters	
	MINIMUN	MAXIMUM
N	8	
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BASIC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
α	0°	8°

Reference Document: JEDEC Publication 95, MS-012

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS87421AMI	87421AMI	8 lead SOIC	tube	-40°C to 85°C
ICS87421AMI	87421AMI	8 lead SOIC	2500 tape & reel	-40°C to 85°C
ICS87421AMILF	87421AIL	8 lead "Lead-Free" SOIC	tube	-40°C to 85°C
ICS87421AMIFT	87421AIL	8 lead "Lead-Free" SOIC	2500 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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