19-0530; Rev 1; 12/07

175V/2A, High-Speed, Half-Bridge MOSFET Drivers

General Description

The MAX15012/MAX15013 high-frequency, 175V half-bridge, n-channel MOSFET drivers drive high- and low-side MOSFETs in high-voltage applications. These drivers are independently controlled and their 35ns typical propagation delay, from input to output, are matched to within 2ns (typ). The high-voltage operation with very low and matched propagation delay between drivers, and high source/sink current capabilities make these devices suitable for the high-power, high-frequency telecom power converters. A reliable on-chip bootstrap diode connected between V_{DD} and BST eliminates the need for an external discrete diode.

The MAX15012A/C and MAX15013A/C offer both noninverting drivers (see the *Selector Guide*). The MAX15012B/D and MAX15013B/D offer a noninverting high-side driver and an inverting low-side driver. The MAX15012A/B/C/D feature CMOS (V_{DD}/2) logic inputs. The MAX15013A/B/C/D feature TTL logic inputs. The drivers are available in the industry-standard 8-pin SO footprint and pin configuration and a thermally enhanced 8-pin SO package. All devices operate over the -40°C to +125°C automotive temperature range.

Applications

Telecom Half-Bridge Power Supplies

Two-Switch Forward Converters

Full-Bridge Converters

Active-Clamp Forward Converters

Power-Supply Modules

Motor Control

Pin Configurations and Typical Operating Circuit appear at the end of data sheet.

Features

- **HIP2100/HIP2101 Pin Compatible (MAX15012A/C and MAX15013A/C)**
- **Up to 175V Input Operation**
- **8V to 12.6V V_{DD} Input Voltage Range**
- **2A Peak Source and Sink Current Drive Capability**
- **35ns Typical Propagation Delay**
- **Guaranteed 8ns Propagation Delay Matching Between Drivers**
- **Up to 500kHz Switching Frequency**
- **Available in CMOS (V_{DD}/2) or TTL Logic-Level Inputs with Hysteresis**
- **Up to 14V Logic Inputs Independent of Input Voltage**
- **Low 2.5pF Input Capacitance**
- **Low 70µA Supply Current**
- **Versions Available with Combination of Noninverting and Inverting Drivers (MAX15012B/D and MAX15013B/D)**
- **Available in Industry-Standard 8-Pin SO and Thermally Enhanced SO Packages**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX15012AASA+	-40°C to +125°C	8 SO	S8-5
MAX15012BASA+	-40°C to +125°C	8 SO	S8-5
MAX15012CASA+*	-40°C to +125°C	8 SO-EP**	S8E+14
MAX15012DASA+*	-40°C to +125°C	8 SO-EP**	S8E+14

Ordering Information continued at end of data sheet.

+Denotes lead-free package.

**Future product—contact factory for availability.*

***EP = Exposed pad.*

Selector Guide

PART	HIGH-SIDE DRIVER	LOW-SIDE DRIVER	LOGIC LEVELS	PIN COMPATIBLE
MAX15012AASA+	Noninverting	Noninverting	CMOS (V_{DD}/2)	HIP 2100IB
MAX15012BASA+	Noninverting	Inverting	CMOS (V_{DD}/2)	—
MAX15012CASA+	Noninverting	Noninverting	CMOS (V_{DD}/2)	HIP 2100IB
MAX15012DASA+	Noninverting	Inverting	CMOS (V_{DD}/2)	—
MAX15013AASA+	Noninverting	Noninverting	TTL	HIP 2101IB
MAX15013BASA+	Noninverting	Inverting	TTL	—
MAX15013CASA+	Noninverting	Noninverting	TTL	HIP 2101IB
MAX15013DASA+	Noninverting	Inverting	TTL	—

175V/2A, High-Speed, Half-Bridge MOSFET Drivers

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND, unless otherwise noted.)
V_{DD}, IN_H, IN_L.....-0.3V to +14V
DL.....-0.3V to (V_{DD} + 0.3V)
HS.....-5V to +180V
DH to HS.....-0.3V to (V_{DD} + 0.3V)
BST to HS.....-0.3V to +14V
dV/dt at HS.....50V/ns
Continuous Power Dissipation (T_A = +70°C)
8-Pin SO (derate 5.9mW/°C above +70°C).....470.6mW
8-Pin SO-EP (derate 19.2mW/°C above +70°C).....1538.5mW
Junction-to-Case Thermal Resistance (θ_{JC})(Note 1)
8-Pin SO.....40°C/W
8-Pin SO-EP.....6°C/W
Junction-to-Ambient Thermal Resistance (θ_{JA})(Note 1)
8-Pin SO.....170°C/W
8-Pin SO-EP.....52°C/W
Maximum Junction Temperature.....+150°C
Operating Temperature Range.....-40°C to +125°C
Storage Temperature Range.....-65°C to +150°C
Lead Temperature (soldering, 10s).....+300°C

**Per JEDEC 51 Standard Multilayer board.*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JE5D51-7, using a four-layer board. For detailed information on package thermal considerations, see www.maxim-ic.com/thermal-tutorial.

ELECTRICAL CHARACTERISTICS

(V_{DD} = V_{BST} = +8V to +12.6V, V_{HS} = GND = 0V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DD} = V_{BST} = +12V and T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
Operating Supply Voltage	V_{DD}	(Notes 3 and 4)	8.0		12.6	V
V_{DD} Quiescent Supply Current (No Switching)	I_{DD}	IN_H = IN_L = GND (for A/C versions), IN_H = GND, IN_L = V_{DD} (for B/D versions)		70	140	µA
V_{DD} Operating Supply Current	I_{DDO}	f_{SW} = 500kHz, V_{DD} = +12V			3	mA
BST Quiescent Supply Current	I_{BST}	IN_H = IN_L = GND (for A/C versions), IN_H = GND, IN_L = V_{DD} (for B/D versions)		15	40	µA
BST Operating Supply Current	I_{BSTO}	f_{SW} = 500kHz, V_{DD} = V_{BST} = +12V			3	mA
UVLO (V_{DD} to GND)	$UVLO_{VDD}$	V_{DD} rising	6.5	7.3	8.0	V
UVLO (BST to HS)	$UVLO_{BST}$	BST rising	6.0	6.9	7.8	V
UVLO Hysteresis				0.5		V
LOGIC INPUT						
Input-Logic High	$V_{IH\_}$	MAX15012_, CMOS (V_{DD}/2) version	0.67 x V_{DD}	0.55 x V_{DD}		V
		MAX15013_, TTL version	2	1.65		
Input-Logic Low	$V_{IL\_}$	MAX15012_, CMOS (V_{DD}/2) version		0.4 x V_{DD}	0.33 x V_{DD}	V
		MAX15013_, TTL version		1.4	0.8	
Logic-Input Hysteresis	V_{HYS}	MAX15012_, CMOS (V_{DD}/2) version		1.6		V
		MAX15013_, TTL version		0.25		

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = V_{BST} = +8V to +12.6V, V_{HS} = GND = 0V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DD} = V_{BST} = +12V and T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Logic-Input Current	$I_{\_IN}$	V_{IN_L} = V_{DD} for MAX15012B/MAX15012D/ MAX15013B/MAX15013D		-1	+0.001	+1	µA
		V_{IN_H} = 0V					
		V_{IN_L} = 0V for MAX15012A/MAX15012C/ MAX15013A/MAX15013C					
Input Resistance	R_{IN}	IN_H to GND			1		MΩ
		IN_L to V_{DD} for MAX15012B/MAX15012D/ MAX15013B/MAX15013D					
		IN_L to GND for MAX15012A/MAX15012C/ MAX15013A/MAX15013C					
Input Capacitance	C_{IN}				2.5		pF
HIGH-SIDE GATE DRIVER							
HS Maximum Voltage	V_{HS_MAX}	V_{DD} ≤ 10.5V (Note 4)		175			V
BST Maximum Voltage	V_{BST_MAX}	V_{DD} ≤ 10.5V (Note 4)		189			V
Driver Output Resistance (Sourcing)	R_{ON_HP}	V_{DD} = 12V, I_{DH} = 100mA (sourcing)	T_A = +25°C		2.5	3.3	Ω
			T_A = +125°C		3.5	4.6	
Driver Output Resistance (Sinking)	R_{ON_HN}	V_{DD} = 12V, I_{DH} = 100mA (sinking)	T_A = +25°C		2.1	2.8	Ω
			T_A = +125°C		3.2	4.2	
DH Reverse Current (Latchup Protection)		(Note 5)		400			mA
Power-Off Pulldown Clamp Voltage		V_{BST} = 0V or floating, I_{DH} = 1mA (sinking)			0.94	1.16	V
Peak Output Current (Sourcing)	I_{DH_PEAK}	C_L = 10nF, V_{DH} = 0V			2		A
Peak Output Current (Sinking)		C_L = 10nF, V_{DH} = 12V			2		A
LOW-SIDE GATE DRIVER							
Driver Output Resistance (Sourcing)	R_{ON_LP}	V_{DD} = 12V, I_{DL} = 100mA (sourcing)	T_A = +25°C		2.5	3.3	Ω
			T_A = +125°C		3.5	4.6	
Driver Output Resistance (Sinking)	R_{ON_LN}	V_{DD} = 12V, I_{DL} = 100mA (sinking)	T_A = +25°C		2.1	2.8	Ω
			T_A = +125°C		3.2	4.2	
Reverse Current at DL (Latchup Protection)		(Note 5)		400			mA
Power-Off Pulldown Clamp Voltage		V_{DD} = 0V or floating, I_{DL} = 1mA (sinking)			0.95	1.16	V
Peak Output Current (Sourcing)	I_{PK_LP}	C_L = 10nF, V_{DL} = 0V			2		A
Peak Output Current (Sinking)	I_{PK_LN}	C_L = 10nF, V_{DL} = 12V			2		A
INTERNAL BOOTSTRAP DIODE							
Forward Voltage Drop	V_F	I_{BST} = 100mA			0.91	1.11	V
Turn-On and Turn-Off Time	t_R	I_{BST} = 100mA			40		ns

175V/2A, High-Speed, Half-Bridge MOSFET Drivers

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = V_{BST} = +8V to +12.6V, V_{HS} = GND = 0V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DD} = V_{BST} = +12V and T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SWITCHING CHARACTERISTICS FOR HIGH- AND LOW-SIDE DRIVERS (V_{DD} = V_{BST} = +12V)							
Rise Time	t_R	C_L = 1000pF			7		ns
		C_L = 5000pF			33		
		C_L = 10,000pF			65		
Fall Time	t_F	C_L = 1000pF			7		ns
		C_L = 5000pF			33		
		C_L = 10,000pF			65		
Turn-On Propagation Delay Time	t_{D_ON}	Figure 1, C_L = 1000pF (Note 5)	CMOS		30	55	ns
			TTL		35	63	
Turn-Off Propagation Delay Time	t_{D_OFF}	Figure 1, C_L = 1000pF (Note 5)	CMOS		30	55	ns
			TTL		35	63	
Delay Matching Between Driver-Low and Driver-High	t_{MATCH}	C_L = 1000pF, Figure 1 (Note 5)			2	8	ns
Internal Nonoverlap					1		ns
Minimum Pulse Width Input Logic (Note 6)	$t_{PW\text{-}min}$	V_{DD} = V_{BST} = 12V			135		ns
		V_{DD} = V_{BST} = 8V			170		

Note 2: All devices are 100% tested at T_A = +125°C. Limits over temperature are guaranteed by design.

Note 3: Ensure that the V_{DD}-to-GND or BST-to-HS transient voltage does not exceed 13.2V.

Note 4: Maximum operating supply voltage (V_{DD}) reduces linearly from 12.6V to 10.5V with its maximum voltage (V_{HS_MAX}) increasing from 125V to 175V. See the *Typical Operating Characteristics* and *Applications Information* sections.

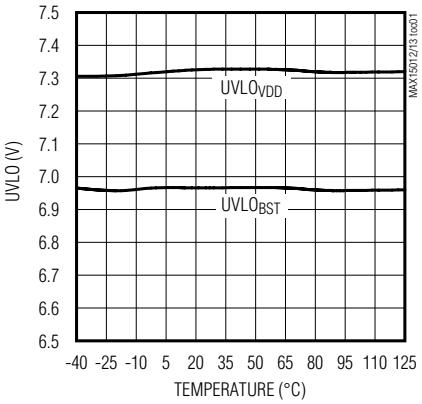
Note 5: Guaranteed by design, not production tested.

Note 6: See the *Minimum Input Pulse Width* section.

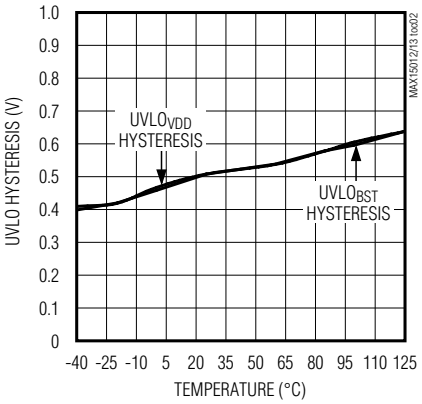
Typical Operating Characteristics

(Typical values are at V_{DD} = V_{BST} = +12V and T_A = +25°C, unless otherwise specified.)

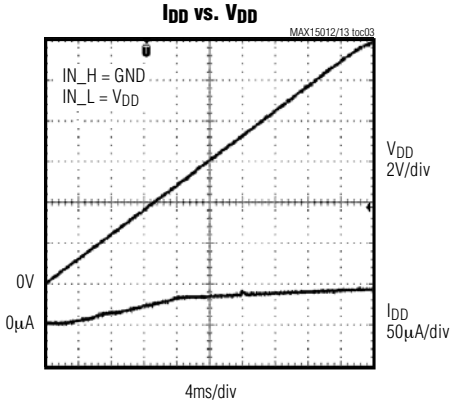
UNDERVOLTAGE LOCKOUT (V_{DD} AND V_{BST} RISING) vs. TEMPERATURE



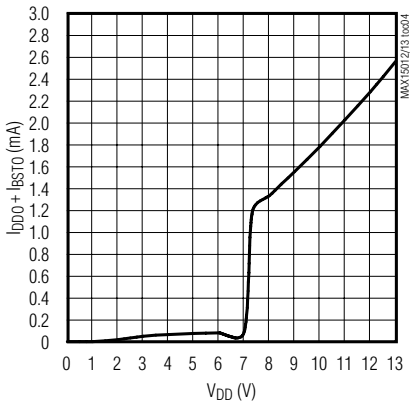
V_{DD} AND BST UNDERVOLTAGE LOCKOUT HYSTERESIS vs. TEMPERATURE



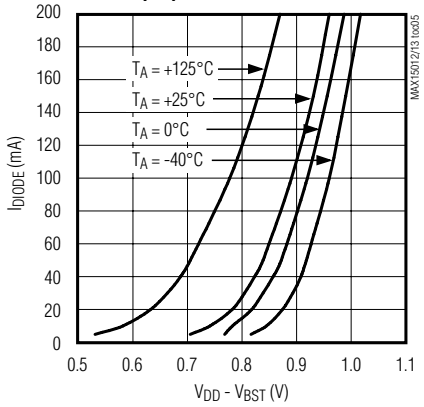
I_{DD} vs. V_{DD}



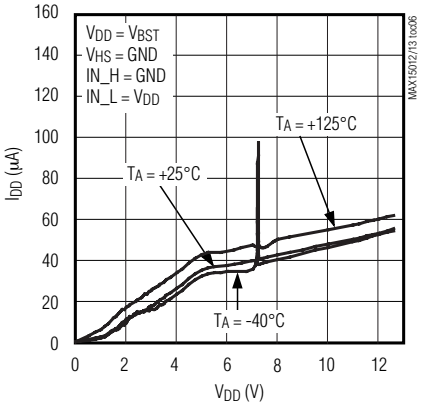
I_{DDO} + I_{BSTO} vs. V_{DD} (f_{SW} = 250kHz)



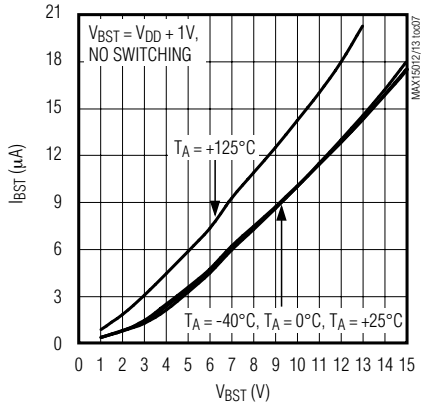
INTERNAL BST DIODE (I-V) CHARACTERISTICS



V_{DD} QUIESCENT CURRENT vs. V_{DD} (NO SWITCHING)



BST QUIESCENT CURRENT vs. BST VOLTAGE

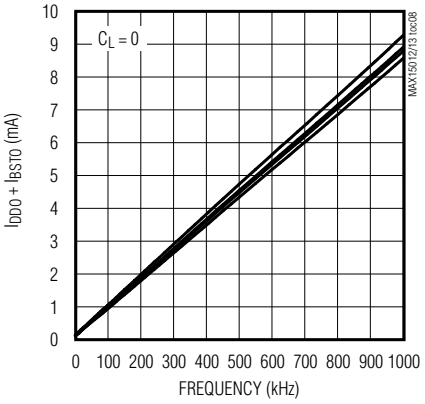


175V/2A, High-Speed, Half-Bridge MOSFET Drivers

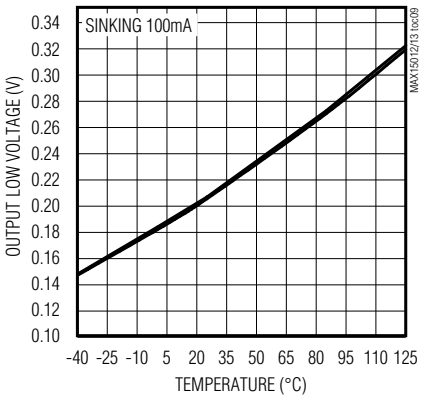
Typical Operating Characteristics (continued)

(Typical values are at V_{DD} = V_{BST} = +12V and T_A = +25°C, unless otherwise specified.)

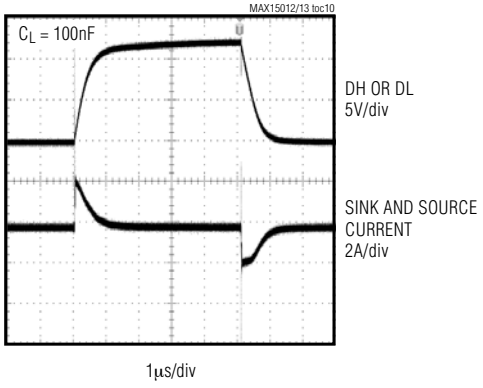
V_{DD} AND BST OPERATING SUPPLY CURRENT vs. FREQUENCY



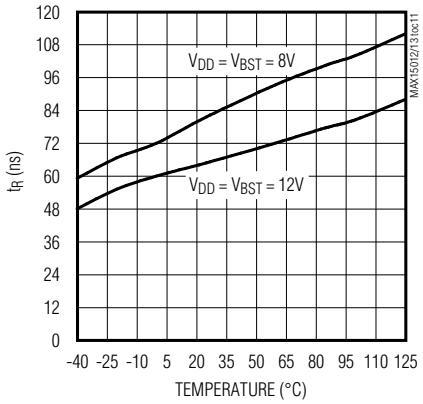
DH OR DL OUTPUT LOW VOLTAGE vs. TEMPERATURE



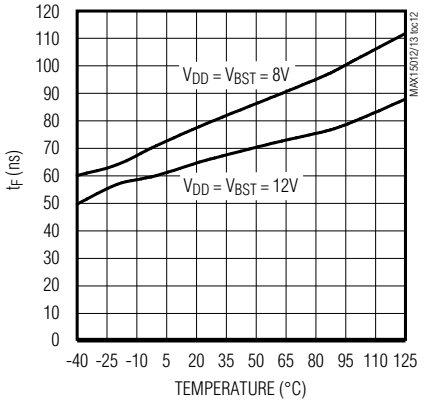
PEAK DH AND DL SOURCE/SINK CURRENT



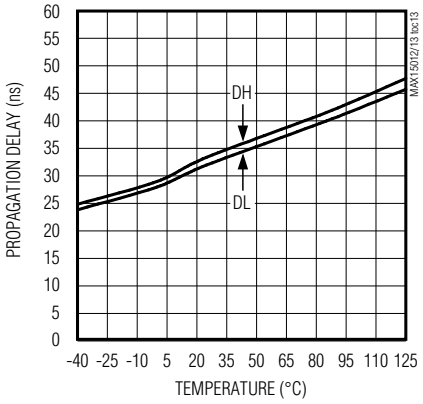
DH OR DL RISE TIME vs. TEMPERATURE (C_L = 10nF)



DH OR DL FALL TIME vs. TEMPERATURE (C_{LOAD} = 10nF)



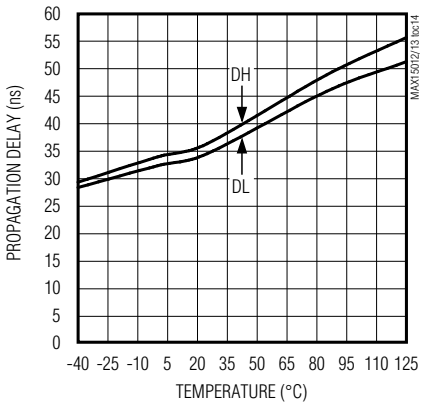
DH OR DL RISE PROPAGATION DELAY vs. TEMPERATURE



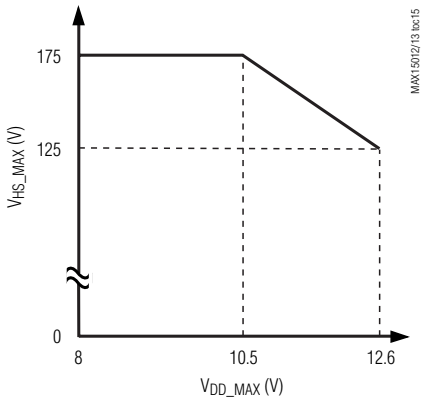
Typical Operating Characteristics (continued)

(Typical values are at V_{DD} = V_{BST} = +12V and T_A = +25°C, unless otherwise specified.)

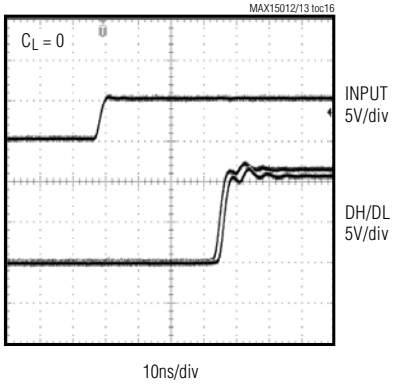
DH OR DL FALL PROPAGATION DELAY vs. TEMPERATURE



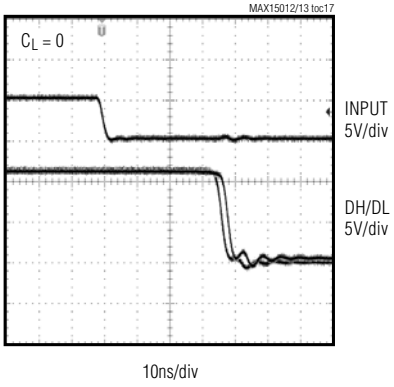
V_{HS_MAX} vs. V_{DD_MAX}



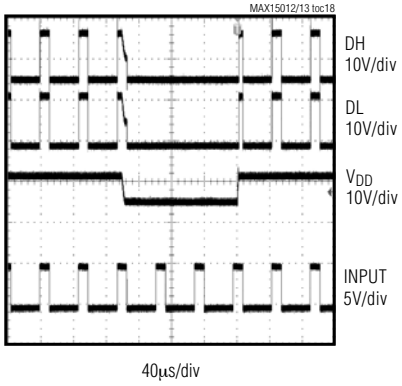
DELAY MATCHING (DH/DL RISING)



DELAY MATCHING (DH/DL FALLING)



DH/DL RESPONSE TO V_{DD} GLITCH



175V/2A, High-Speed, Half-Bridge MOSFET Drivers

Pin Description

PIN	NAME	FUNCTION
1	V_{DD}	Power Input. Bypass V_{DD} to GND with a parallel combination of 0.1µF and 1µF ceramic capacitors.
2	BST	Boost Flying Capacitor Connection. Connect a 0.1µF ceramic capacitor between BST and HS for the high-side MOSFET driver supply.
3	DH	High-Side-Gate Driver Output. Driver output for the high-side MOSFET gate.
4	HS	Source Connection for High-Side MOSFET. Also serves as a return terminal for the high-side driver.
5	IN_H	High-Side Noninverting Logic Input
6	IN_L	Low-Side Noninverting Logic Input (MAX15012A/C and MAX15013A/C). Low-side inverting logic input (MAX15012B/D and MAX15013B/D).
7	GND	Ground. Use GND as a return path to the DL driver output and IN_H/IN_L inputs.
8	DL	Low-Side-Gate Driver Output. Drives low-side MOSFET gate.
—	EP	Exposed Pad. Internally connected to GND. Externally connect the exposed pad to a large ground plane to aid in heat dissipation (MAX15012C/D and MAX15013C/D only).

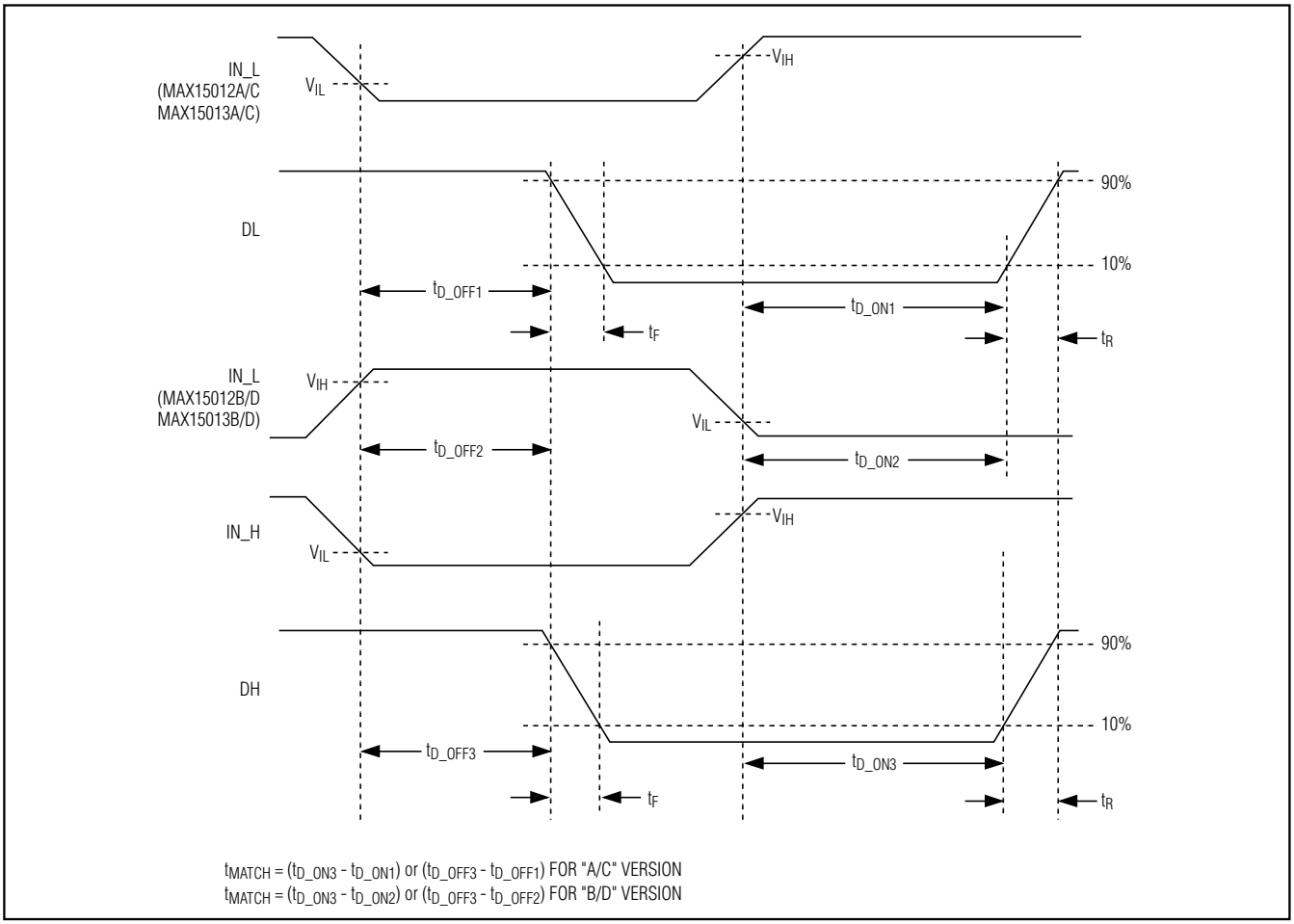


Figure 1. Timing Characteristics for Noninverting and Inverting Logic Inputs

Detailed Description

The MAX15012/MAX15013 are 175V/2A high-speed, half-bridge MOSFET drivers that operate from a supply voltage of +8V to +12.6V. The drivers are intended to drive a high-side switch without any isolation device like an optocoupler or drive transformer. The high-side driver is controlled by a TTL/CMOS logic signal referenced to ground. The 2A source and sink drive capability is achieved by using low R_{DS_ON}, p- and n-channel driver output stages. The BiCMOS process allows extremely fast rise/fall times and low propagation delays. The typical propagation delay from the logic-input signal to the driver output is 35ns with a matched propagation delay of 2ns typical. Matching these propagation delays is as important as the absolute value of the delay itself. The high 175V input voltage range allows plenty of margin above the 100V transient specification per telecom standards.

The maximum operating supply voltage (V_{DD}) must be reduced linearly from 12.6V to 10.5V when the maximum voltage (V_{HS_MAX}) increases from 125V to 175V. See the *Typical Operating Characteristics*.

Undervoltage Lockout

Both the high- and low-side drivers feature undervoltage lockout (UVLO). The low-side driver's $UVLO_{LOW}$ threshold is referenced to GND and pulls both driver outputs low when V_{DD} falls below 6.8V. The high-side driver has its own UVLO threshold ($UVLO_{HIGH}$), referenced to HS, and pulls DH low when BST falls below 6.4V with respect to HS.

During turn-on, once V_{DD} rises above its UVLO threshold, DL starts switching and follows the IN_L logic input. At this time, the bootstrap capacitor is not charged and the BST-to-HS voltage is below $UVLO_{BST}$. For synchronous buck and half-bridge converter topologies, the bootstrap capacitor can charge up in one cycle and normal operation begins in a few microseconds after the BST-to-HS voltage exceeds $UVLO_{BST}$. In the two-switch forward topology, the BST capacitor takes some time (a few hundred microseconds) to charge and increase its voltage above $UVLO_{BST}$.

The typical hysteresis for both UVLO thresholds is 0.5V. The bootstrap capacitor value should be selected carefully to avoid unintentional oscillations during turn-on and turn-off at the DH output. Choose the capacitor value about 20 times higher than the total gate capacitance of the MOSFET. Use a low-ESR-type X7R dielectric ceramic capacitor at BST (typically a 0.1µF ceramic capacitor is adequate) and a parallel combination of 1µF and 0.1µF ceramic capacitors from V_{DD} to GND. The high-side MOSFET's continuous on-time is limited due to the charge loss from the high-side driver's quiescent current. The maximum on-time is dependent on the size of C_{BST}, I_{BST} (40µA max), and $UVLO_{BST}$.

Output Driver

The MAX15012/MAX15013 have low 2.5Ω R_{DS_ON} p-channel and n-channel devices (totem pole) in the output stage. This allows for a fast turn-on and turn-off of the high gate-charge switching MOSFETs. The peak source and sink current is typically 2A. Propagation delays from the logic inputs to the driver outputs are matched to within 8ns. The internal p- and n-channel MOSFETs have a 1ns break-before-make logic to avoid any cross conduction between them. This internal break-before-make logic eliminates shoot-through currents reducing the operating supply current as well as the spikes at V_{DD}. See the *Minimum Input Pulse Width* section to understand the effects of propagation delays on DH and DL. The DL voltage is approximately equal to V_{DD}, the DH-to-HS voltage is approximately equal to V_{DD} minus a diode drop, when they are in a high state and to zero when in a low state. The driver R_{DS_ON} is lower at higher V_{DD}. Lower R_{DS_ON} means higher source and sink currents and faster switching speeds.

Internal Bootstrap Diode

An internal diode connects from V_{DD} to BST and is used in conjunction with a bootstrap capacitor externally connected between BST and HS. The diode charges the capacitor from V_{DD} when the DL low-side switch is on and isolates V_{DD} when HS is pulled high as the high-side driver turns on (see the *Typical Operating Circuit*).

The internal bootstrap diode has a typical forward voltage drop of 0.9V and has a 10ns typical turn-off/turn-on time. For lower voltage drops from V_{DD} to BST, connect an external Schottky diode between V_{DD} and BST.

Driver Logic Inputs (IN_H, IN_L)

The MAX15012A/B/C/D are CMOS (V_{DD} / 2) logic-input drivers while the MAX15013A/B/C/D have TTL-compatible logic inputs. The logic-input signals are independent of V_{DD}. For example, the IC can be powered by a 10V supply while the logic inputs are provided from a 12V CMOS logic. Also, the logic inputs are protected against voltage spikes up to 14V, regardless of the V_{DD} voltage. The TTL and CMOS logic inputs have 250mV and 1.6V hysteresis, respectively, to avoid double pulsing during transition. The logic inputs are high-impedance pins and should not be left floating. The low 2.5pF input capacitance reduces loading and increases switching speed. The noninverting inputs are pulled down to GND and the inverting inputs are pulled up to V_{DD} internally using a 1MΩ resistor. The PWM output from the controller must assume a proper state while powering up the device. With the logic inputs floating, the DH and DL outputs pull low as V_{DD} rises up above the UVLO threshold.

Minimum Input Pulse Width

The MAX15012/MAX15013 use a single-shot level-shifter architecture to achieve low propagation delay. Typical level shifter architecture causes a minimum (high or low) pulse width (t_{Dmin}) at the output that may be higher than the logic-input pulse width. For the MAX15012/MAX15013 devices, the DH minimum high pulse-width ($t_{Dmin-DH-H}$) is lower than the DL minimum low pulse width ($t_{Dmin-DL-L}$) to avoid any shoot-through in the absence of external BBM delay during the narrow pulse at low duty cycle. See Figure 2.

At high duty cycle (close to 100%), the DH minimum low pulse width ($t_{Dmin-DH-L}$) must be higher than the DL minimum low pulse width ($t_{Dmin-DL-L}$) to avoid the overlap and shoot-through. See Figure 3. In case of the MAX15012/MAX15013, there is a possibility of about 40ns overlap if an external BBM delay is not provided. It is recommended to add external delay in the INH path so that the minimum low pulse width seen at INH is always longer than t_{PW-min}. See the *Electrical Characteristics* table for the typical values of t_{PW-min}.

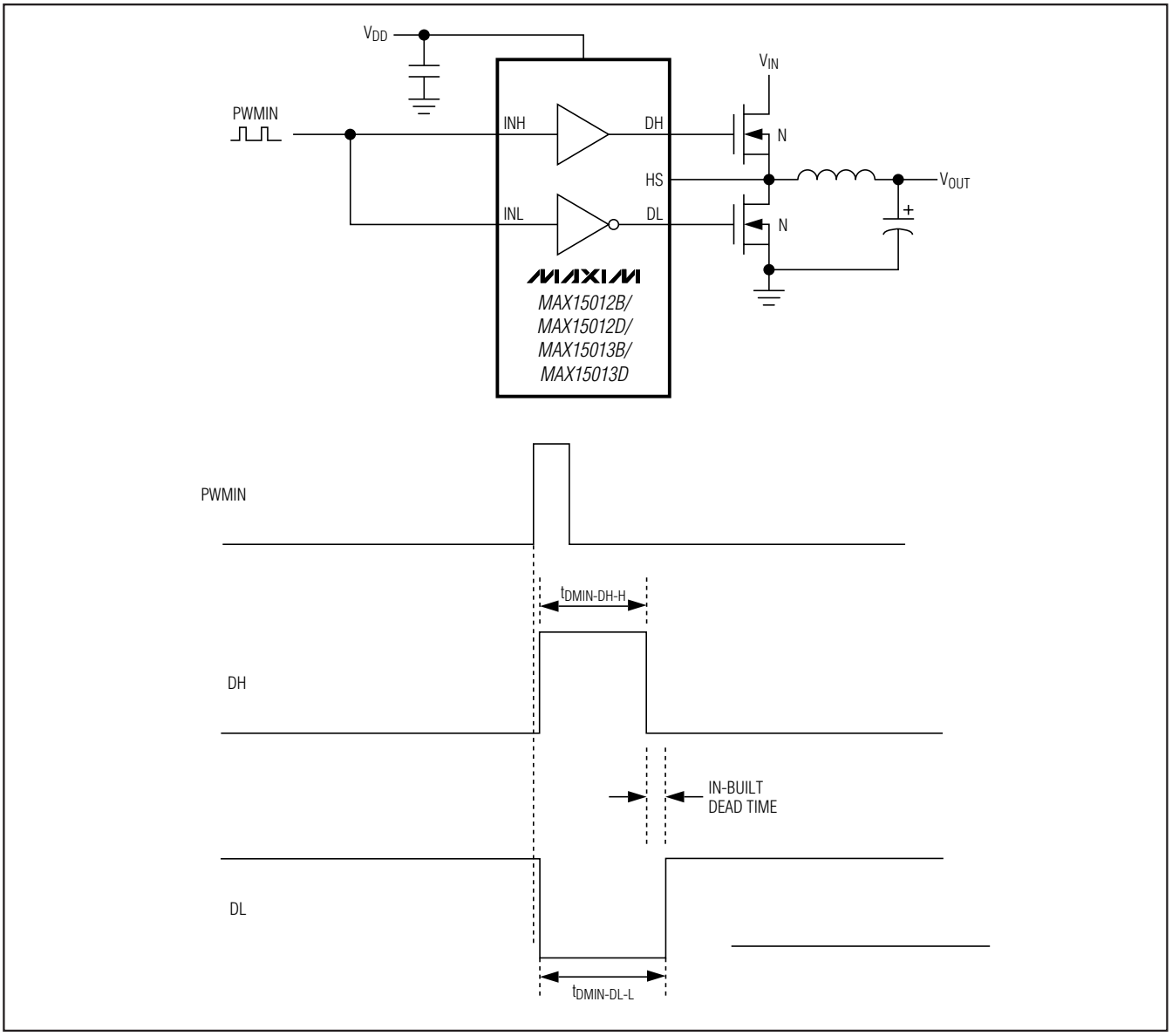


Figure 2. Minimum Pulse-Width Behavior for Narrow Duty-Cycle Input (On-Time < t_{PW-min})

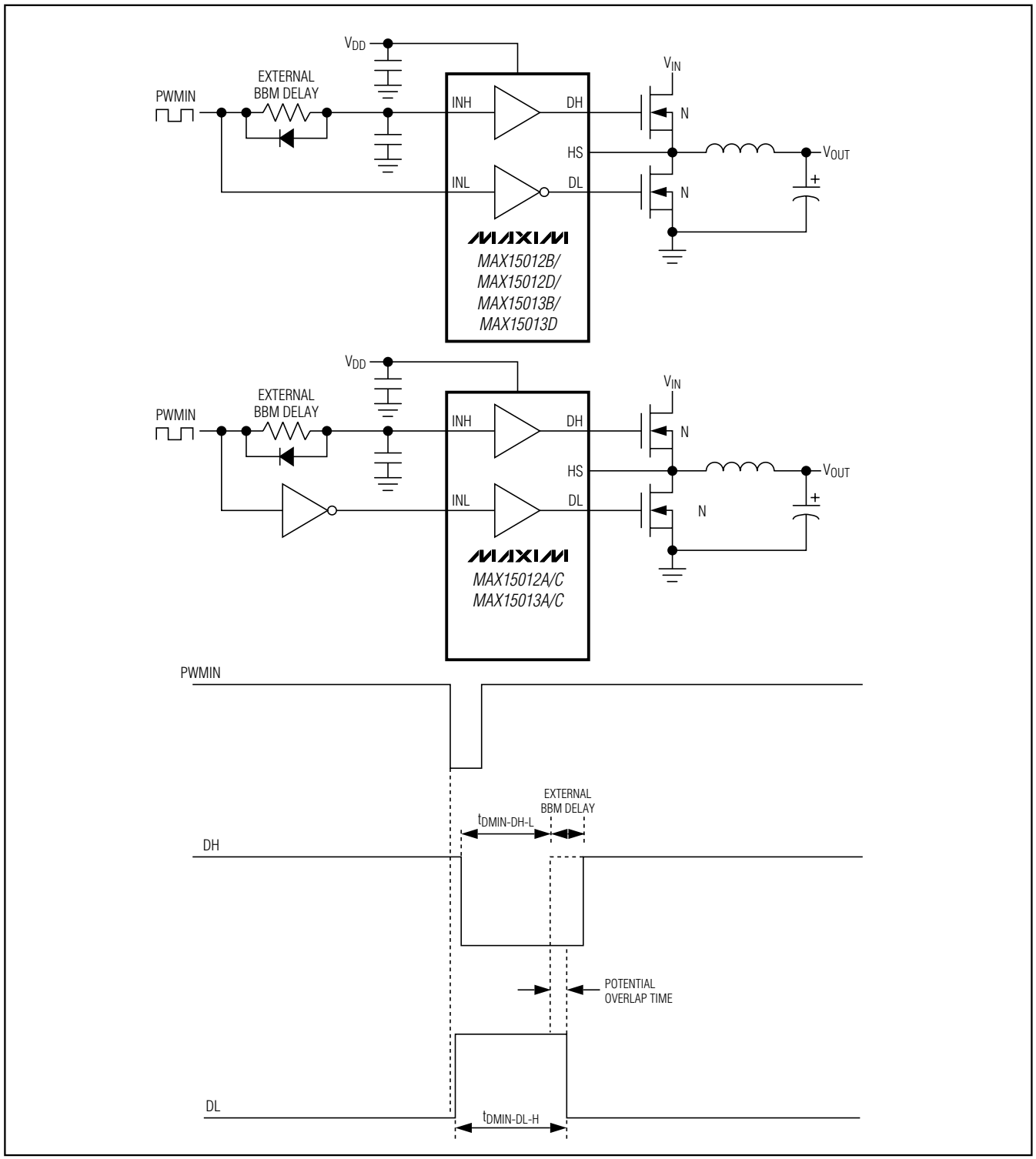


Figure 3. Minimum Pulse-Width Behavior for High Duty-Cycle Input (Off-Time < t_{PW-min})

175V/2A, High-Speed, Half-Bridge MOSFET Drivers

Applications Information

Supply Bypassing and Grounding

Pay extra attention to bypassing and grounding the MAX15012/MAX15013. Peak supply and output currents may exceed 4A when both drivers are driving large external capacitive loads in-phase. Supply drops and ground shifts create forms of negative feedback for inverters and may degrade the delay and transition times. Ground shifts due to insufficient device grounding may also disturb other circuits sharing the same AC ground return path. Any series inductance in the V_{DD}, DH, DL, and/or GND paths can cause oscillations due to the very high di/dt when switching the MAX15012/MAX15013 with any capacitive load. Place one or more 0.1µF ceramic capacitors in parallel as close to the device as possible to bypass V_{DD} to GND. Use a ground plane to minimize ground return resistance and series inductance. Place the external MOSFET as close as possible to the MAX15012/MAX15013 to further minimize board inductance and AC path resistance.

Power Dissipation

Power dissipation in the MAX15012/MAX15013 is primarily due to power loss in the internal boost diode and the nMOS and pMOS FETs.

For capacitive loads, the total power dissipation for the device is:

$$P_D = \left(C_L \times V_{DD}^2 \times f_{SW}\right) + \left(I_{DDO} + I_{BSTO}\right) \times V_{DD}$$

where C_L is the combined capacitive load at DH and DL. V_{DD} is the supply voltage and f_{SW} is the switching frequency of the converter. P_D includes the power dissipated in the internal bootstrap diode. The internal power dissipation reduces by P_{DIODE}, if an external bootstrap Schottky diode is used. The power dissipation in the internal boost diode (when driving a capacitive load) is the charge through the diode per switching period multiplied by the maximum diode forward voltage drop (V_f = 1V).

$$P_{DIODE} \cong C_{DH} \times \left(V_{DD} - 1\right) \times f_{SW} \times V_f$$

The total power dissipation when using the internal boost diode is P_D and, when using an external Schottky diode, is P_D - P_{DIODE}. The total power dissipated in the device must be kept below the maximum of 0.471W for the 8-pin SO package at T_A = +70°C ambient.

Layout Information

The MAX15012/MAX15013 drivers source and sink large currents to create very fast rise and fall edges at the gates of the switching MOSFETs. The high di/dt can cause unacceptable ringing if the trace lengths and impedances are not well controlled. Use the following PC board layout guidelines when designing with the MAX15012/MAX15013:

- It is important that the V_{DD} voltage (with respect to ground) or BST voltage (with respect to HS) does not exceed 13.2V. Voltage spikes higher than 13.2V from V_{DD} to GND or BST to HS can damage the device. Place one or more low ESL 0.1µF decoupling ceramic capacitors from V_{DD} to GND, and from BST to HS as close as possible to the part. The ceramic decoupling capacitors should be at least 20 times the gate capacitance being driven.
- There are two AC current loops formed between the device and the gate of the MOSFET being driven. The MOSFET looks like a large capacitance from gate to source when the gate is being pulled low. The active current loop is from the MOSFET driver output (DL or DH) to the MOSFET gate, to the MOSFET source, and to the return terminal of the MOSFET driver (either GND or HS). When the gate of the MOSFET is being pulled high, the active current loop is from the MOSFET driver output, (DL or DH), to the MOSFET gate, to the MOSFET source, to the return terminal of the drivers decoupling capacitor, to the positive terminal of the decoupling capacitor, and to the supply connection of the MOSFET driver. The decoupling capacitor is either the flying capacitor connected between BST and HS or the decoupling capacitor for V_{DD}. Care must be taken to minimize the physical length and the impedance of these AC current paths.

Typical Application Circuits

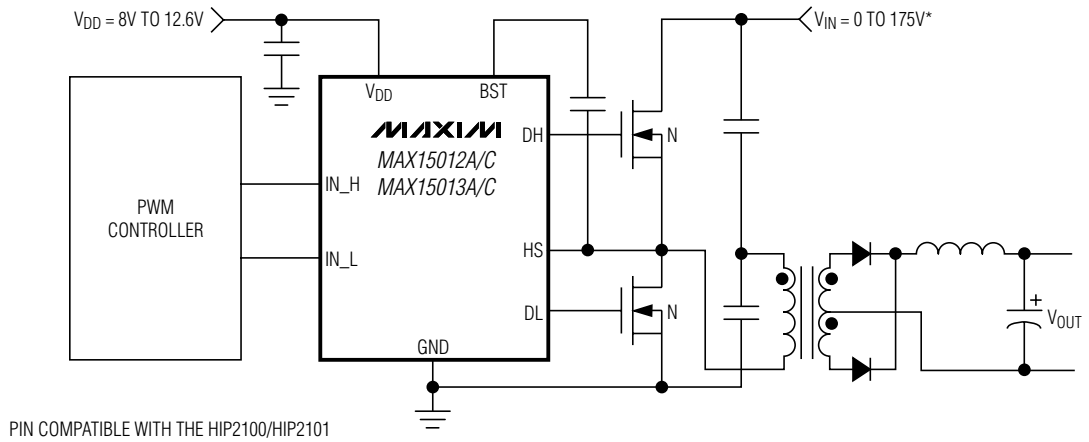


Figure 4. MAX15012A/MAX15013A Half-Bridge Conversion

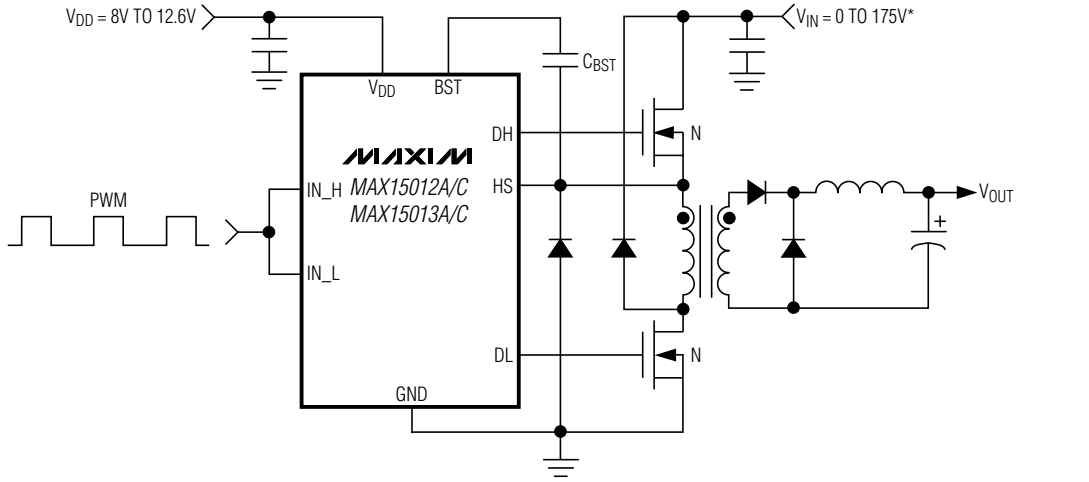
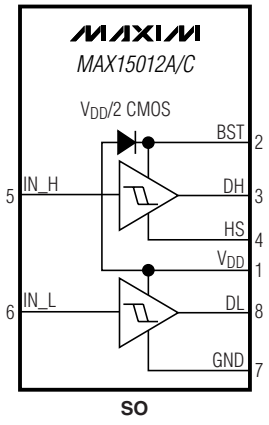
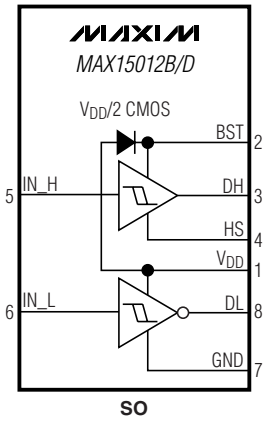


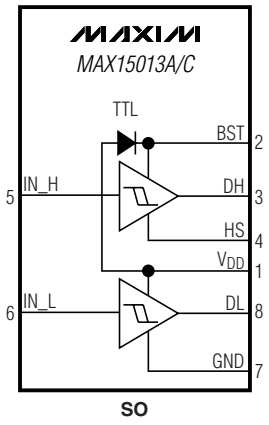
Figure 5. Two-Switch Forward Conversion

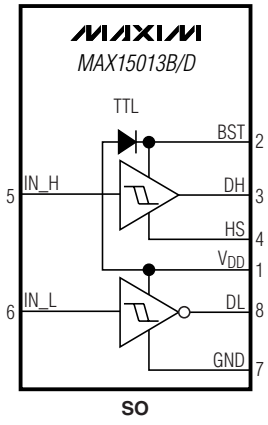
175V/2A, High-Speed, Half-Bridge MOSFET Drivers

Functional Diagrams



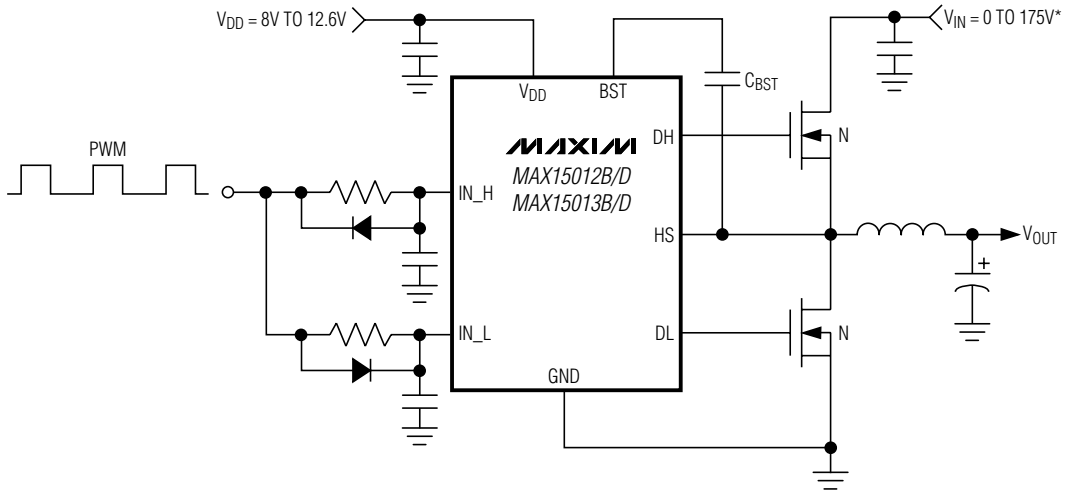






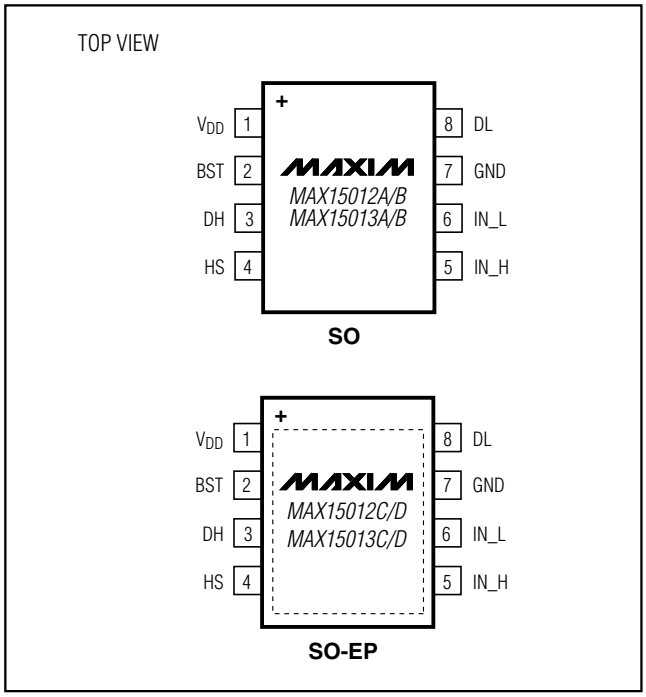
175V/2A, High-Speed, Half-Bridge MOSFET Drivers

Typical Operating Circuit



*DERATE V_{DD} IF V_{IN} INCREASES ABOVE 125V. SEE NOTE 3 IN THE *ELECTRICAL CHARACTERISTICS*.

Pin Configurations



Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX15013AASA+	-40°C to +125°C	8 SO	S8-5
MAX15013BASA+	-40°C to +125°C	8 SO	S8-5
MAX15013CASA+*	-40°C to +125°C	8 SO-EP**	S8E+14
MAX15013DASA+*	-40°C to +125°C	8 SO-EP**	S8E+14

+Denotes lead-free package.
**Future product—contact factory for availability.*
***EP = Exposed pad.*

Chip Information

TRANSISTOR COUNT: 790

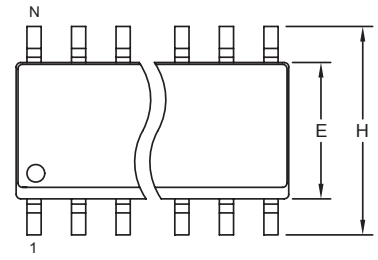
PROCESS: HV BiCMOS

175V/2A, High-Speed, Half-Bridge MOSFET Drivers

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

SOICN .EPS

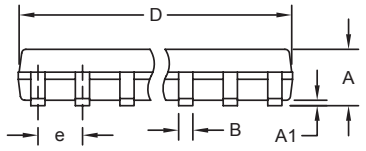


TOP VIEW

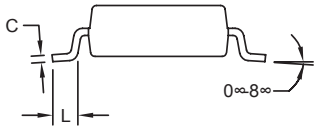
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050 BSC		1.27 BSC	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27

VARIATIONS:

	INCHES		MILLIMETERS			
DIM	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	AA
D	0.337	0.344	8.55	8.75	14	AB
D	0.386	0.394	9.80	10.00	16	AC



FRONT VIEW



SIDE VIEW

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
4. CONTROLLING DIMENSION: MILLIMETERS.
5. MEETS JEDEC MS012.
6. N = NUMBER OF PINS.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

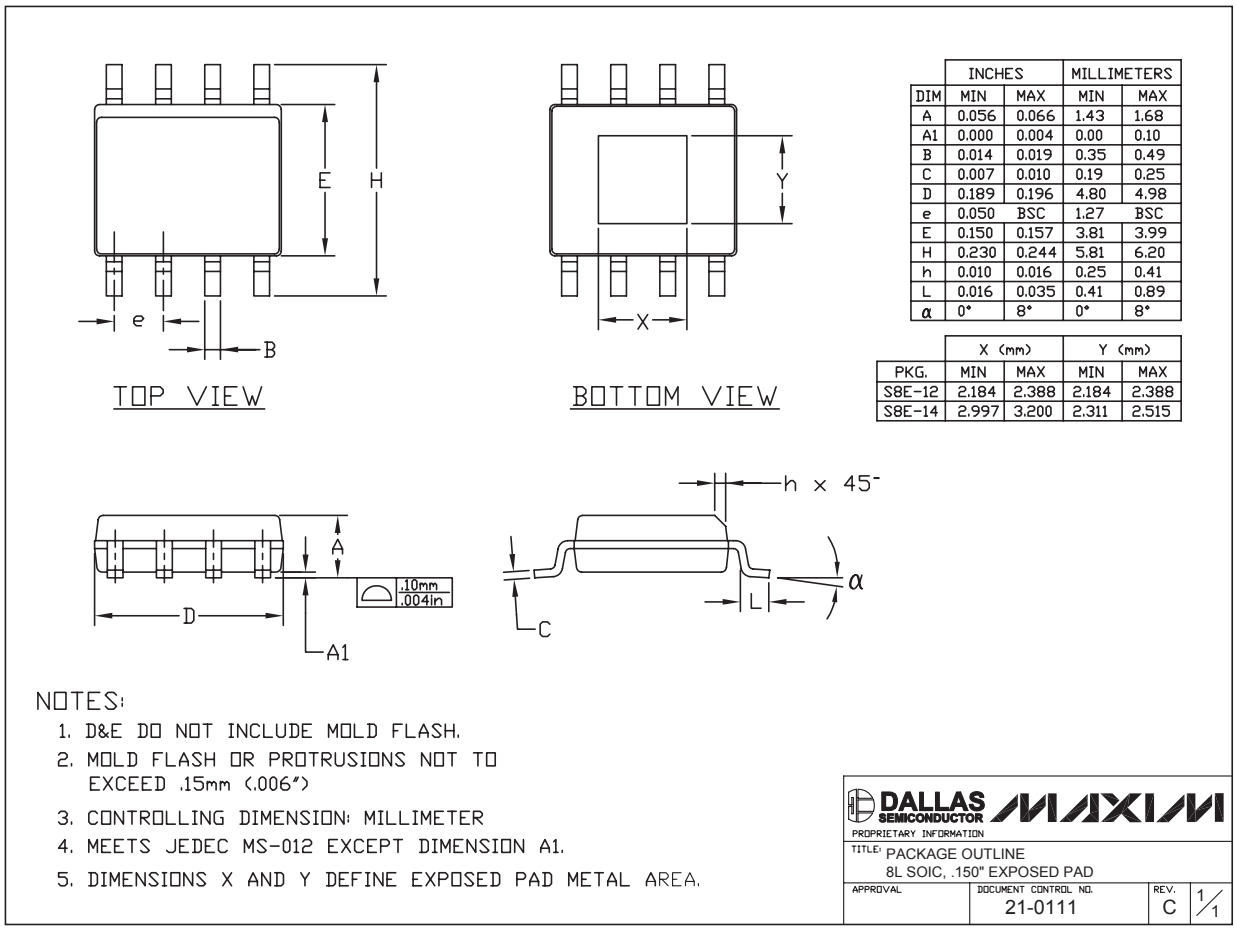
TITLE: PACKAGE OUTLINE, .150" SOIC

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0041	B	1/1

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

8L, SOIC EXP. PAD.EPS



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.056	0.066	1.43	1.68
A1	0.000	0.004	0.00	0.10
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
D	0.189	0.196	4.80	4.98
e	0.050	BSC	1.27	BSC
E	0.150	0.157	3.81	3.99
H	0.230	0.244	5.81	6.20
h	0.010	0.016	0.25	0.41
L	0.016	0.035	0.41	0.89
α	0°	8°	0°	8°

	X (mm)		Y (mm)	
PKG.	MIN	MAX	MIN	MAX
S8E-12	2.184	2.388	2.184	2.388
S8E-14	2.997	3.200	2.311	2.515

NOTES:

1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS-012 EXCEPT DIMENSION A1.
5. DIMENSIONS X AND Y DEFINE EXPOSED PAD METAL AREA.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE 8L SOIC, .150" EXPOSED PAD

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0111	C	1/1

175V/2A, High-Speed, Half-Bridge MOSFET Drivers

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/06	Initial release	—
1	12/07	Added exposed paddle versions of the MAX15012A/B and MAX15013A/B, added Figures 2 and 3 and added SO-EP package outline	1–4, 8–11, 13–17