ANALOG DEVICES

2 A, Low Dropout, CMOS Linear Regulator

Preliminary Technical Data

ADP1740/ADP1741

FEATURES

Maximum output current: 2 A
Input voltage range: 1.6 V to 3.6 V
Low shutdown current: <1 μA
Low dropout voltage: 200 mV @ 2 A load
Initial accuracy: ±1%
Accuracy over line, load, and temperature: ±2.5%
7 fixed output voltage options with soft start (ADP1740):
   0.75 V to 2.5 V
Adjustable output voltage options with soft start (ADP1741):
   0.75 V to 3.0 V
Stable with small 4.7 μF ceramic output capacitor
Excellent load/line transient response
Current limit and thermal overload protection
Power Good indicator
Logic-controlled enable

APPLICATIONS

Notebook computers
Memory components
Telecommunications equipment
Network equipment
DSP/FPGA/microprocessor supplies
Instrumentation equipment/data acquisition systems

TYPICAL APPLICATION CIRCUITS

Figure 1. ADP1740 with Fixed Output Voltage, 1.5 V

Figure 2. ADP1741 with Adjustable Output Voltage, 0.75 V to 3.0 V

GENERAL DESCRIPTION

The ADP1740/ADP1741 are CMOS, low dropout linear regulators that operate from 1.6 V to 3.6 V and provide up to 2 A of output current. Using an advanced proprietary architecture, they provide high power supply rejection and achieve excellent line and load transient response with a small 4.7 μF ceramic output capacitor.

The ADP1740 is available in seven fixed output voltage options. The ADP1741 is an adjustable output voltage version, which
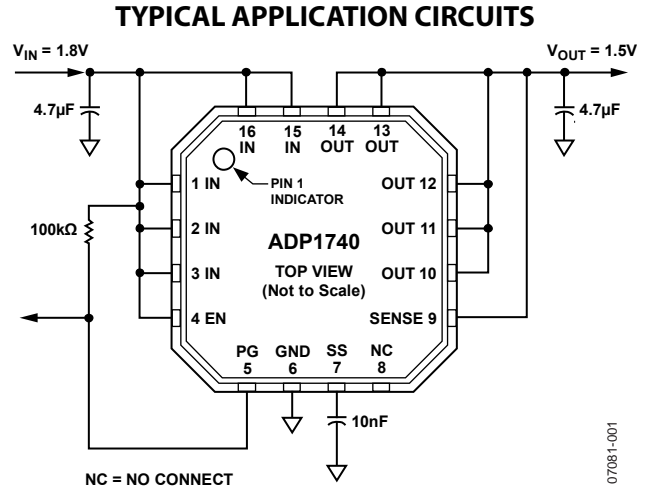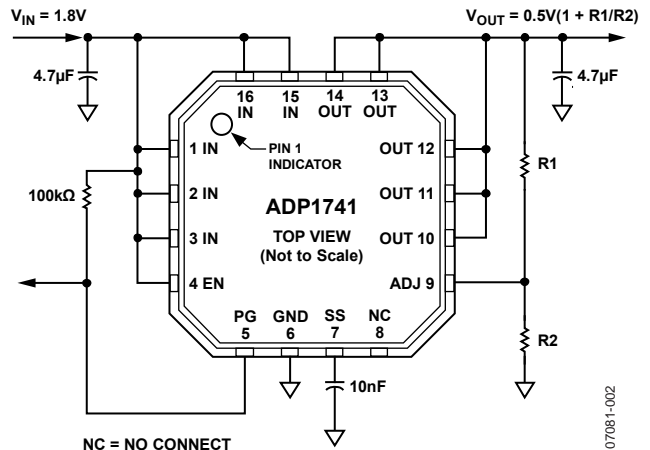
allows output voltages that range from 0.75 V to 3.0 V via an external divider. The ADP1740/ADP1741 allow an external soft start capacitor to be connected to program the start-up.

The ADP1740/ADP1741 are available in a 16-lead, 4 mm × 4 mm LFCSP, making them very compact solutions while providing excellent thermal performance for applications requiring up to 2 A of output current in a small, low profile footprint.

TABLE OF CONTENTS

SPECIFICATIONS

V_{IN} = (V_{OUT} + 0.4 V) or 1.8 V (whichever is greater), I_{OUT} = 10 mA, C_{IN} = C_{OUT} = 4.7 μF, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
INPUT VOLTAGE RANGE	V_{IN}	T_J = −40°C to +125°C	1.6		3.6	V
OPERATING SUPPLY CURRENT	I_{GND}	I_{OUT} = 0 mA		45		μA
		I_{OUT} = 100 mA		500		μA
		I_{OUT} = 100 mA, T_J = −40°C to +125°C			TBD	μA
		I_{OUT} = 2 A		1.3		mA
		I_{OUT} = 2 A, T_J = −40°C to +125°C			TBD	mA
SHUTDOWN CURRENT	I_{GND-SD}	EN = GND		1	3	μA
		EN = GND, T_J = −40°C to +125°C			30	μA
OUTPUT VOLTAGE ACCURACY						
Fixed Output Voltage Accuracy (ADP1740)	V_{OUT}	I_{OUT} = 10 mA	−1		+1	%
		I_{OUT} = 1 mA to 2 A	−1.5		+1.5	%
		1 mA < I_{OUT} < 2 A, T_J = −40°C to +125°C	−2.5		+2.5	%
Adjustable Output Voltage Accuracy (ADP1741)[1]	V_{OUT}	I_{OUT} = 10 mA	0.743	0.75	0.758	V
		I_{OUT} = 1 mA to 2 A	0.739		0.761	V
		1 mA < I_{OUT} < 2 A, T_J = −40°C to +125°C	0.731		0.769	V
LINE REGULATION	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = (V_{OUT} + 0.4 V) to 3.6 V, T_J = −40°C to +125°C	−0.1		+0.1	%/V
LOAD REGULATION[2]	$\Delta V_{OUT}/\Delta I_{OUT}$	I_{OUT} = 10 mA to 2 A, T_J = −40°C to +125°C			TBD	%/mA
DROPOUT VOLTAGE[3]	$V_{DROPOUT}$	I_{OUT} = 100 mA, V_{OUT} ≥ 1.8 V		15		mV
		I_{OUT} = 100 mA, V_{OUT} ≥ 1.8 V, T_J = −40°C to +125°C			40	mV
		I_{OUT} = 2 A, V_{OUT} ≥ 1.8 V		200		mV
		I_{OUT} = 2 A, V_{OUT} ≥ 1.8 V, T_J = −40°C to +125°C			350	mV
START-UP TIME[4]	$t_{START-UP}$					
ADP1740 and ADP1741		C_{SS} = 10 nF, I_{OUT} = 10 mA		4.8		ms
CURRENT LIMIT THRESHOLD[5]	I_{LIMIT}		TBD	3	TBD	A
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	TS_{SD}	T_J rising		150		°C
Thermal Shutdown Hysteresis	TS_{SD-HYS}			15		°C
PG OUTPUT LOGIC LEVEL						
PG Output Logic High	PG_{HIGH}	1.6 V ≤ V_{IN} ≤ 3.6 V, I_{OH} < 1 μA	1.0			V
PG Output Logic Low	PG_{LOW}	1.6 V ≤ V_{IN} ≤ 3.6 V, I_{OL} <2 mA			0.4	V
PG Output Delay from EN Transition Low to High		1.6 V ≤ V_{IN} ≤ 3.6 V, C_{SS} = 10 nF			TBD	ms
PG OUTPUT THRESHOLD						
PG Threshold, Output Voltage Falling	PG_{FALL}	1.6 V ≤ V_{IN} ≤ 3.6 V		−10		%
PG Threshold, Output Voltage Rising	PG_{RISE}	1.6 V ≤ V_{IN} ≤ 3.6 V		−7		%
EN INPUT						
EN Input Logic High	V_{IH}	1.6 V ≤ V_{IN} ≤ 3.6 V	1.0			V
EN Input Logic Low	V_{IL}	1.6 V ≤ V_{IN} ≤ 3.6 V			0.4	V
EN Input Leakage Current	$V_{I-LEAKAGE}$	EN = IN or GND		0.1	1	μA
SOFT START INPUT						
Soft Start Current	I_{SS}	1.6 V ≤ V_{IN} ≤ 3.6 V	TBD	1	TBD	μA
ADJ INPUT BIAS CURRENT (ADP1741)	ADJ_{I-BIAS}	1.6 V ≤ V_{IN} ≤ 3.6 V		30	100	nA
SENSE INPUT BIAS CURRENT	SNS_{I-BIAS}	1.6 V ≤ V_{IN} ≤ 3.6 V		10		μA
OUTPUT NOISE	OUT_{NOISE}	10 Hz to 100 kHz, V_{OUT} = 0.75 V		40		μV rms
		10 Hz to 100 kHz, V_{OUT} = 2.5V		80		μV rms

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
POWER SUPPLY REJECTION RATIO	PSRR	1 kHz, V_{OUT} = 0.75 V, I_{OUT} = 10 mA		70		dB
		1 kHz, V_{OUT} = 2.5 V, I_{OUT} = 10 mA		60		dB
		10 kHz, V_{OUT} = 0.75 V, I_{OUT} = 10 mA		TBD		dB
		10 kHz, V_{OUT} = 2.5 V, I_{OUT} = 10 mA		TBD		dB

[1] Accuracy when OUT is connected directly to ADJ. When OUT voltage is set by external feedback resistors, absolute accuracy in adjust mode depends on the tolerances of resistors used.

[2] Based on an end-point calculation using 10 mA and 2 A loads.

[3] Dropout voltage is defined as the input to output voltage differential when the input voltage is set to the nominal output voltage. This applies only for output voltages above 1.6 V.

[4] Start-up time is defined as the time between the rising edge of EN to OUT being at 95% of its nominal value.

[5] Current limit threshold is defined as the current at which the output voltage drops to 90% of the specified typical value. For example, the current limit for a 1.0 V output voltage is defined as the current that causes the output voltage to drop to 90% of 1.0 V, or 0.9 V.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
IN to GND	−0.3 V to +3.6 V
OUT to GND	−0.3 V to IN
EN to GND	−0.3 V to +3.6 V
SS to GND	−0.3 V to +3.6 V
PG to GND	−0.3 V to +3.6 V
SENSE/ADJ to GND	−0.3 V to +3.6 V
Storage Temperature Range	−65°C to +150°C
Operating Junction Temperature Range	−40°C to +125°C
Soldering Conditions	JEDEC J-STD-020

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

| Package Type	θ_{JA}	Unit
16-Lead LFCSP with Exposed Pad	38	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS
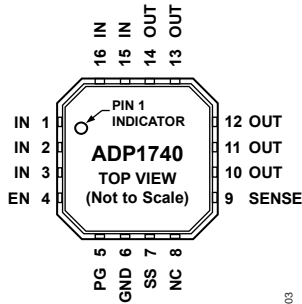
Figure 3. ADP1740 Pin Configuration
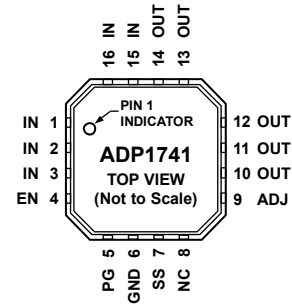
Figure 4. ADP1741 Pin Configuration

Table 4. Pin Function Descriptions

Pin No.		Mnemonic	Description
ADP1740	**ADP1741**		
1, 2, 3, 15, 16	1, 2, 3, 15, 16	IN	Regulator Input Supply. Bypass IN to GND with a 4.7 µF or greater capacitor. Note that all five pins must be connected to source
4	4	EN	Enable Input. Drive EN high to turn on the regulator; drive it low to turn off the regulator. For automatic startup, connect EN to IN.
5	5	PG	Power Good. This open-drain output requires an external pull-up resistor to IN. If part is in shutdown, current limit, thermal shutdown, or falls below 90% of the nominal output voltage, PG immediately transitions low.
6	6	GND	Ground.
7	7	SS	Soft Start. A capacitor connected to this pin determines the soft start time.
8	8	NC	Not connected. No internal connection
9	N/A	SENSE	Sense. Measures the actual output voltage at the load and feeds it to the error amplifier. Connect SENSE as close as possible to the load to minimize the effect of IR drop between the regulator output and the load.
N/A	9	ADJ	Adjust. A resistor divider from OUT to ADJ sets the output voltage.
10, 11, 12, 13, 14	10, 11, 12, 13, 14	OUT	Regulated Output Voltage. Bypass OUT to GND with a 4.7 µF or greater capacitor. Note that all five pins must be connected to load
EP	EP		Exposed pad on the bottom of the LFCSP package. EP enhances thermal performance and is electrically connected to GND inside the package. It is recommended to connect EP to the ground plane on the board.

ANALOG DEVICES

www.analog.com