Data Sheet August 15, 2007 FN7442.6

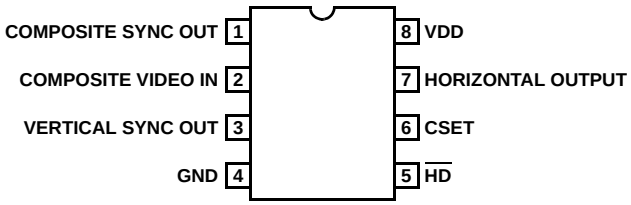
Auto-Adjusting Sync Separator for HD and SD Video

The ISL59885 video sync separator extracts sync timing information from both standard and non-standard video inputs in the presence of Macrovision pulses. The ISL59885 provides horizontal, vertical, and composite sync outputs as well as SD/HDTV detection. An auto input frequency detect feature automatically adapts to a wide range of video standards (it does not need a different RSET resistor for different frequencies). The vertical sync pulse is output on the rising edge of the first vertical serration following the vertical pre-equalizing string. For non-standard vertical inputs, a default vertical pulse is output when the vertical signal stays low for longer than the vertical sync default delay time. The horizontal output gives horizontal timing with pre/post equalizing pulses. Fixed 70mV sync tip slicing provides sync edge detection when the video input level is between $0.5V_{P-P}$ and $2V_{P-P}$.

The ISL59885 is available in an 8 Ld SOIC package and is specified for operation over the full -40°C to +85°C temperature range.

Pinout

ISL59885
(8 LD SOIC)
TOP VIEW



Features

- NTSC, PAL, SECAM, HDTV, non-standard video sync separation
- Fixed 70mV slicing of video input levels from $0.5V_{P-P}$ to $2V_{P-P}$
- Single 3V to 5V supply
- Composite sync output
- Vertical output
- Horizontal output
- HDTV detection
- Macrovision compatible
- Available in 8 Ld SOIC package
- Pb-free available (RoHS compliant)

Applications

- High definition video equipment

Demo Board

- A dedicated demo board is available

Ordering Information

PART NUMBER	PART MARKING	PACKAGE	PKG. DWG. #
ISL59885IS*	59885 IS	8 Ld SOIC	MDP0027
ISL59885ISZ* (Note)	59885 ISZ	8 Ld SOIC (Pb-free)	MDP0027

*Add “-T7” or “-T13” suffix for tape and reel. Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Absolute Maximum Ratings (T_A = +25°C)

V_{DD} Supply 7V
Pin Voltages . . . . . -0.5V to V_{CC} +0.5V
Operating Ambient Temperature Range . . . . . -40°C to +85°C

Thermal Information

Operating Junction Temperature . . . . . +150°C
Storage Temperature . . . . . -65°C to +150°C
Power Dissipation 400mW
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

DC Electrical Specifications

V_{DD} = 3.3V, T_A = +25°C, C_{SET} = 56nF, unless otherwise specified.

PARAMETER	DESCRIPTION	MIN (Note 1)	TYP	MAX (Note 1)	UNIT
I_{DD}, Quiescent	V_{DD} = 3.3V	1.5	2.2	4	mA
Clamp Voltage	Pin 2, I_{LOAD} = -100µA	1.35	1.5	1.65	V
Clamp Discharge Current	Pin 2 = 2V	6	15	30	µA
Clamp Charge Current	Pin 2 = 1V	-9	-7.2	-5.2	mA
V_{OL} Output Low Voltage	I_{OL} = 1.6mA		0.24	0.5	V
V_{OH} Output High Voltage	I_{OH} = -40µA	3	3.2		V
	I_{OH} = -1.6mA	2.5	3.0		V

Dynamic Characteristics

PARAMETER	DESCRIPTION	MIN (Note 1)	TYP	MAX (Note 1)	UNIT
Comp Sync Prop Delay, t_{CS}	(See Figure 9)		35	75	ns
Horizontal Sync Delay, t_{HS}	(See Figure 9)		40	80	ns
Horizontal Sync Width, t_{HS-PW}	(See Figure 9)	3.8	5.2	6.2	µs
Vertical Sync Width, t_{VS}	Normal or default trigger, 50% to 50% (see Figure 7)	230	280	350	µs
Vertical Sync Default Delay, t_{VSD}	(See Figure 10)	28	50	68	µs
Input Dynamic Range	Video input amplitude to maintain slice level spec, V_{DD} = 3.3V	0.5		2	V_{P-P}
Slice Level	V_{SLICE} above V_{CLAMP}	50	70	90	mV
$\overline{HD}$ Pin Level	720p, 1080i, 1080p		0		V

NOTE:

1. Parts are 100% tested at +25°C. Over-temperature limits established by characterization and are not production tested.

Pin Descriptions

PIN NUMBER	PIN NAME	PIN FUNCTION
1	Composite Sync Out	Composite sync pulse output; sync pulses start on a falling edge and end on a rising edge.
2	Composite Video In	AC coupled composite video input; sync tip must be at the lowest potential (positive picture phase).
3	Vertical Sync Out	Vertical sync pulse output; the falling edge of vertical sync is the start of the vertical period.
4	Gnd	Supply ground
5	$\overline{HD}$	Low when input horizontal frequency is greater than 20kHz.
6	CSET	(An external capacitor to ground); bypass pin for internal bias generator.
7	Horizontal Output	Horizontal output; falling edge active
8	VDD	Positive supply

Typical Performance Curves

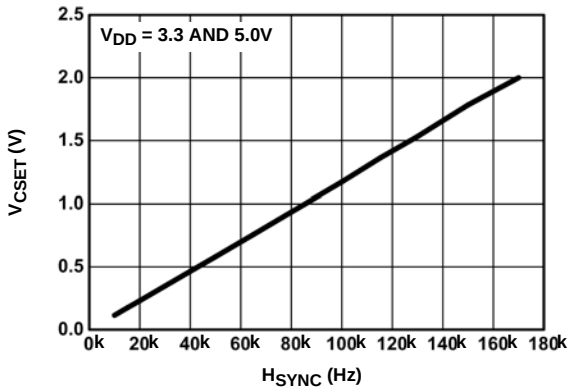


FIGURE 1. H_{SYNC} vs V_{CSET} (R_{SET} = OPEN)

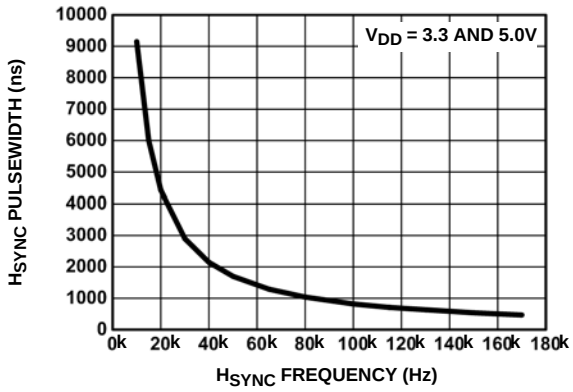


FIGURE 2. H_{SYNC} PULSEWIDTH vs H_{SYNC} FREQUENCY (R_{SET} = OPEN)

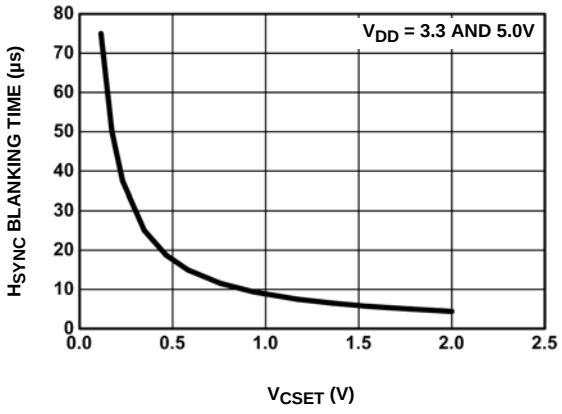


FIGURE 3. H_{SYNC} vs V_{CSET} (R_{SET} = OPEN)

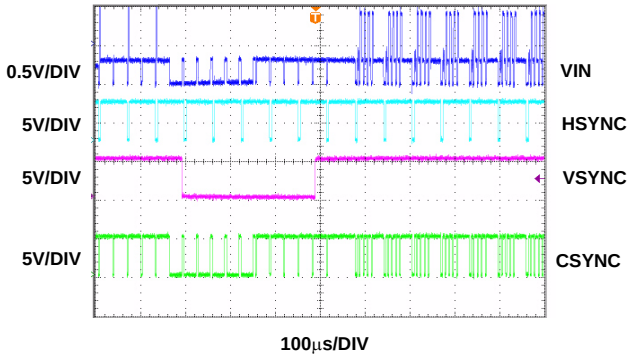


FIGURE 4. MACROVISION COMPATIBILITY (NTSC)

Typical Performance Curves (Continued)

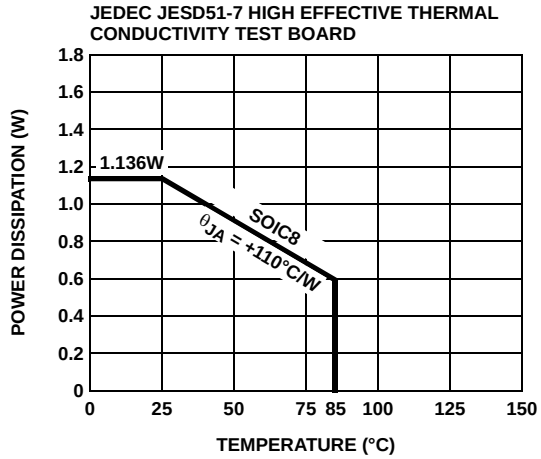


FIGURE 5. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

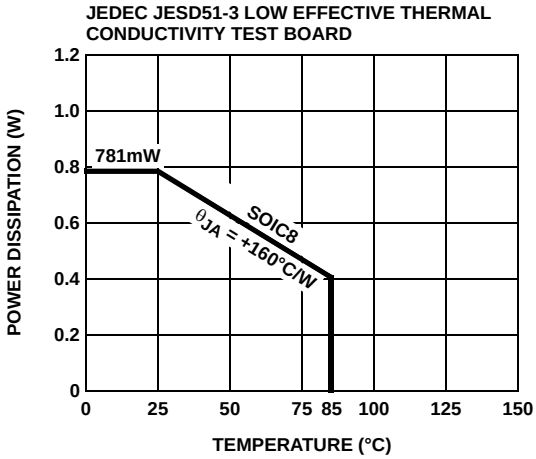
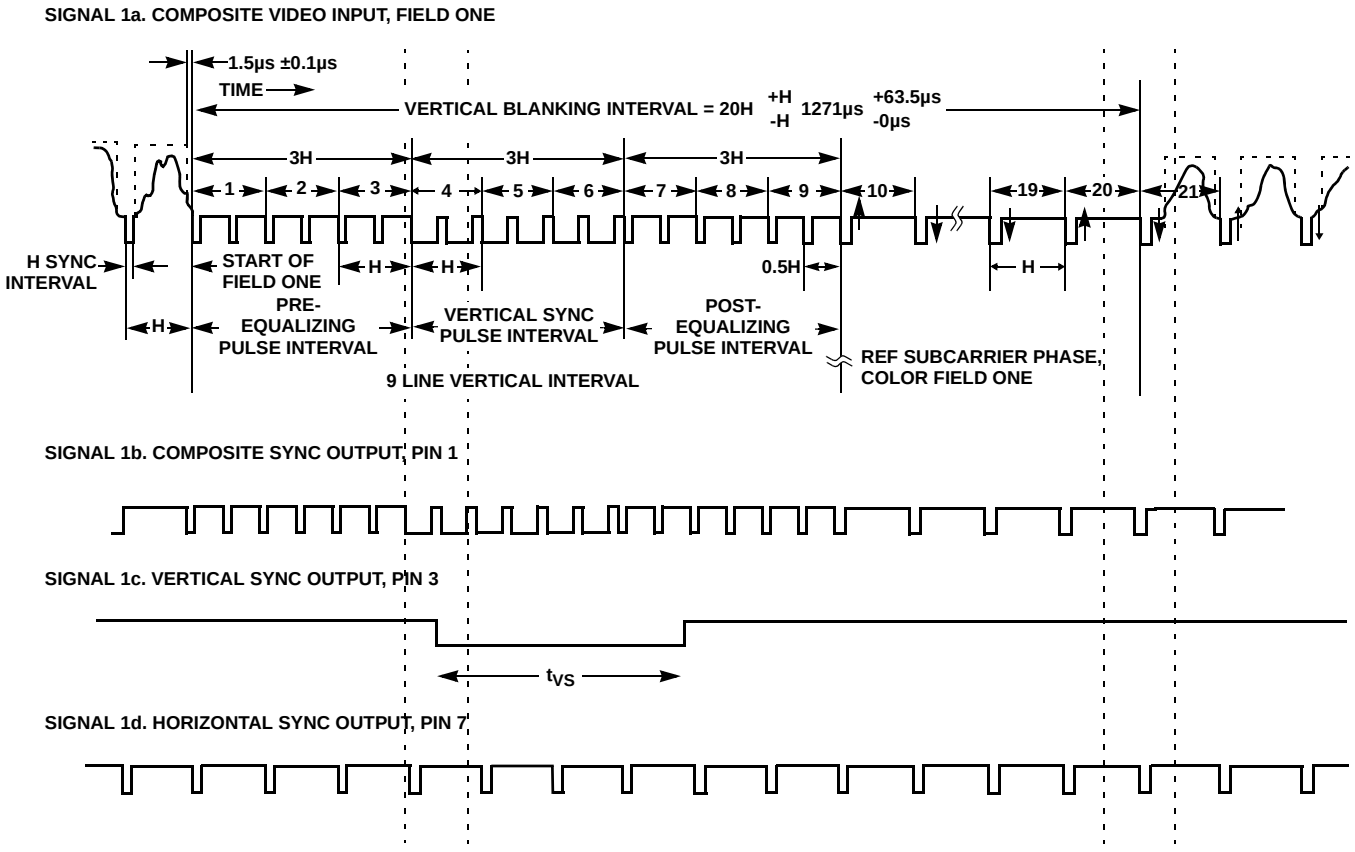


FIGURE 6. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE



NOTES:

2. The composite sync output reproduces all the video input sync pulses, with a propagation delay.
3. Vertical sync leading edge is coincident with the first vertical serration pulse leading edge with a propagation delay.
4. Horizontal sync output produces the true “H” pulses of nominal width of 5µs. It has the same delay as the composite sync.

FIGURE 7. TIMING DIAGRAM

CONDITIONS: V_{DD} = 3.3V/5V, T_A = +25°C

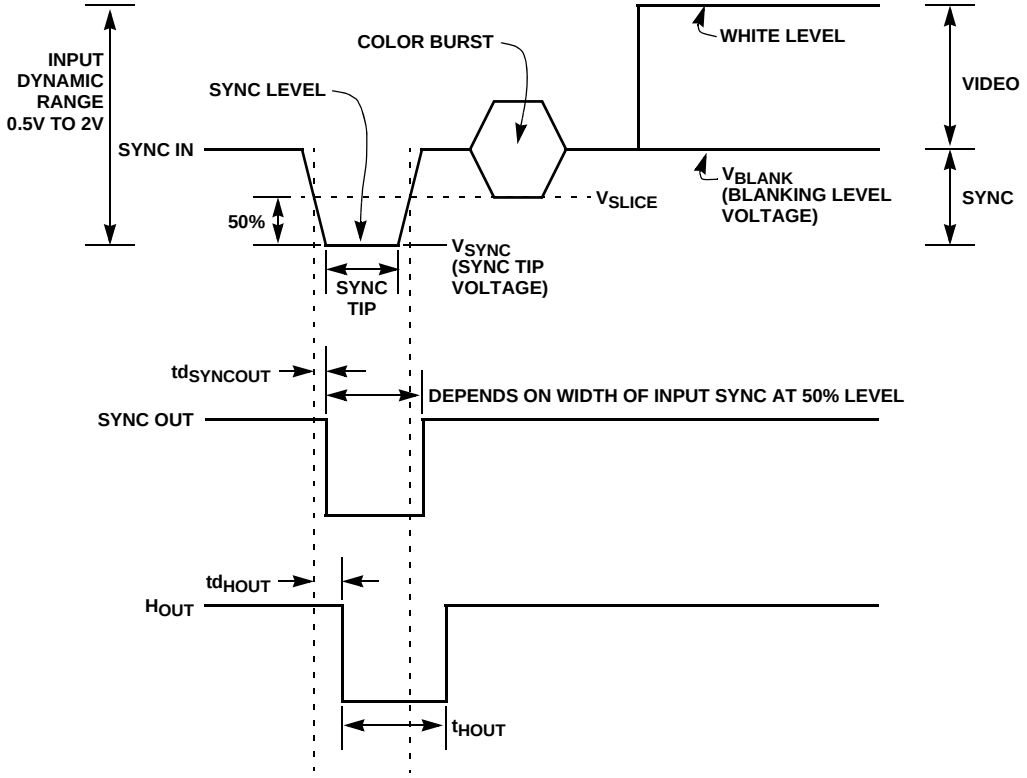


FIGURE 8. HORIZONTAL INTERVAL 525/625 LINE COMPOSITE

PARAMETER	DESCRIPTION	CONDITIONS	TYP (Note 5)	UNIT
$td_{SYNCOUT}$	SYNCOUT Timing Relative to Input	(See Figure 8)	65	ns
td_{HOUT}	HOUT Timing Relative to Input	(See Figure 8)	470	ns
t_{HOUT}	Horizontal Output Width	(See Figure 8)	5.2	µs

NOTE:

5. Delay variation is less than 2.5ns over-temperature range.

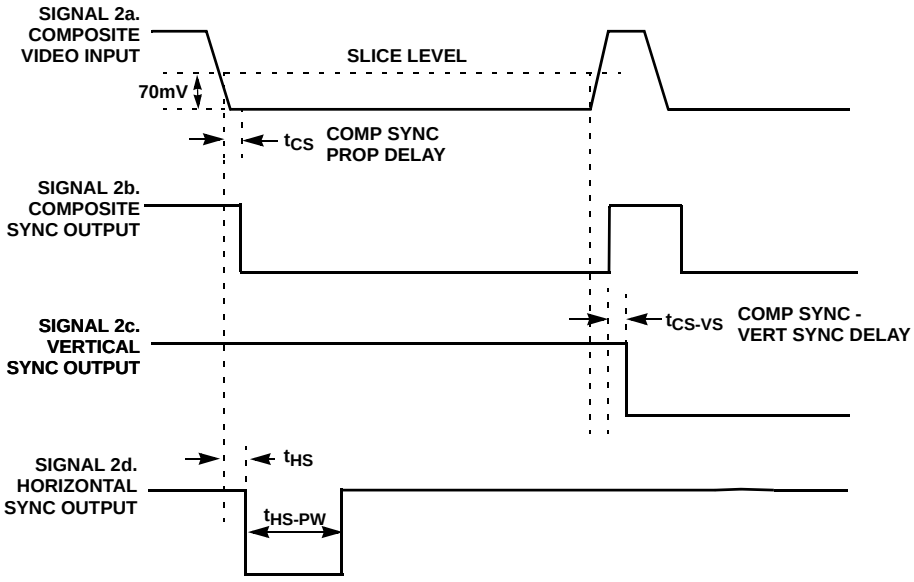


FIGURE 9. STANDARD VERTICAL TIMING

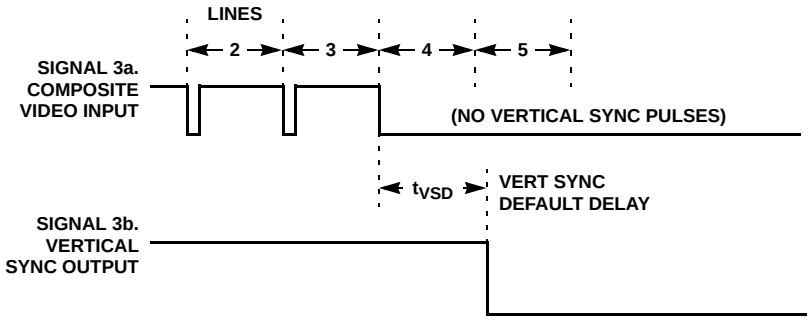
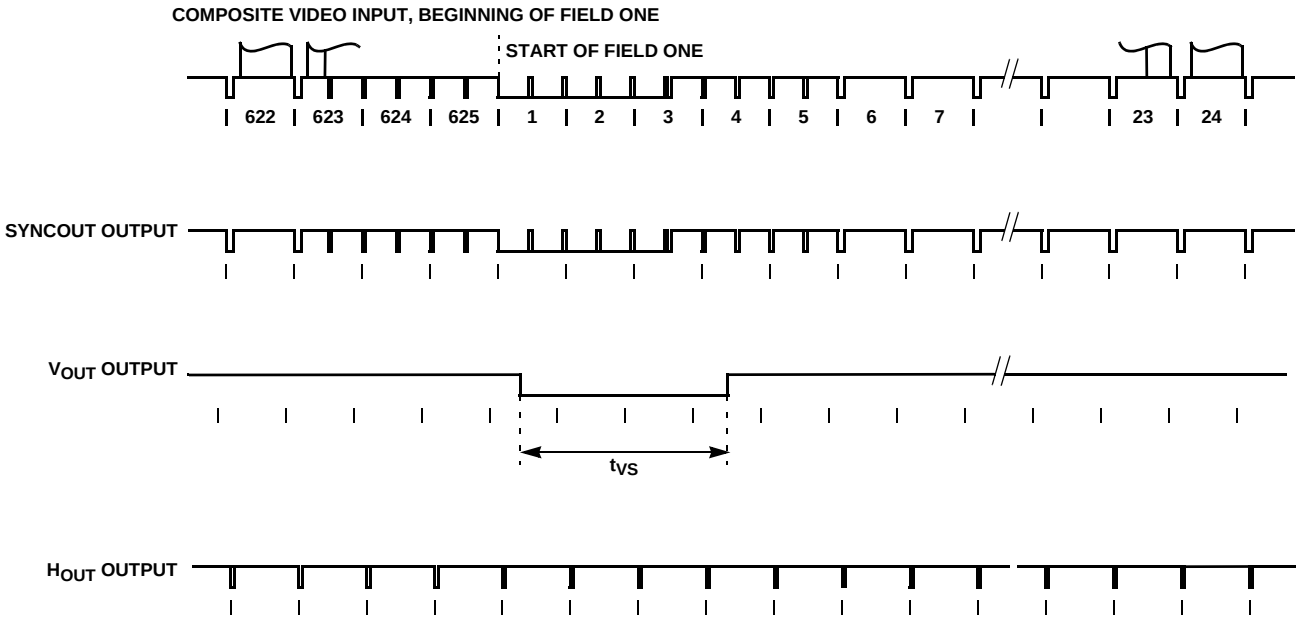


FIGURE 10. NON-STANDARD VERTICAL TIMING



NOTES:

6. The composite sync output reproduces all the video input sync pulses, with a propagation delay.
7. Vertical sync leading edge is coincident with the first vertical serration pulse leading edge, with a propagation delay.

FIGURE 11. EXAMPLE OF VERTICAL INTERVAL (625)

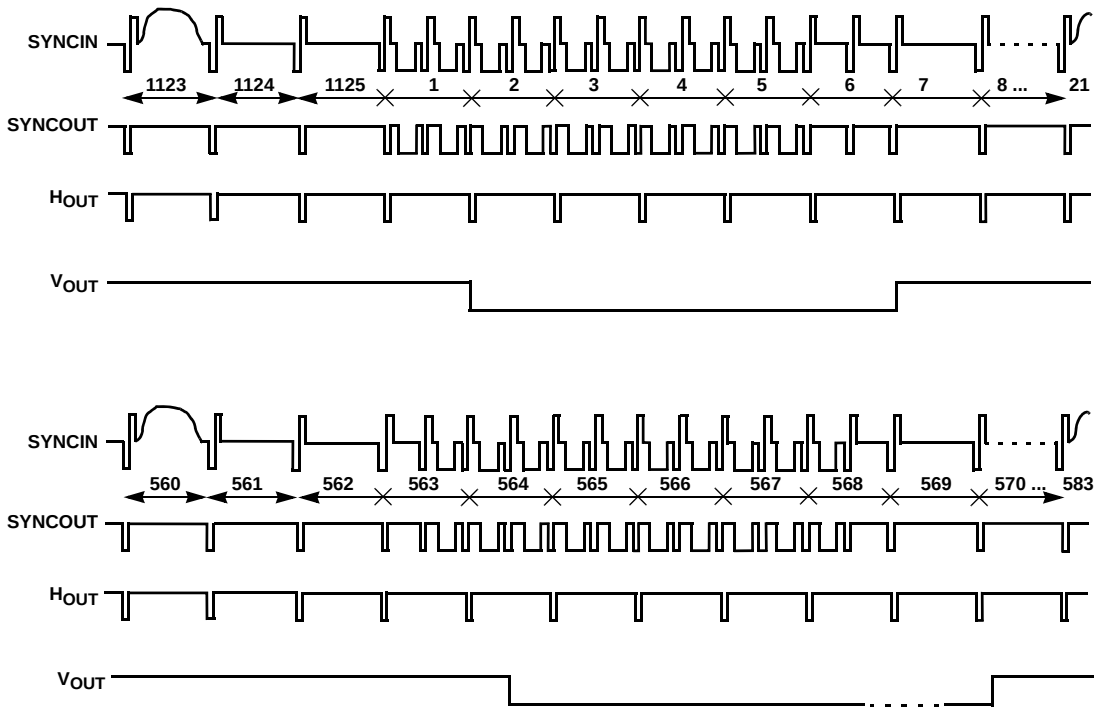


FIGURE 12. EXAMPLE OF HDTV 1080I/30 LINE COMPOSITE VIDEO: INTERLACED

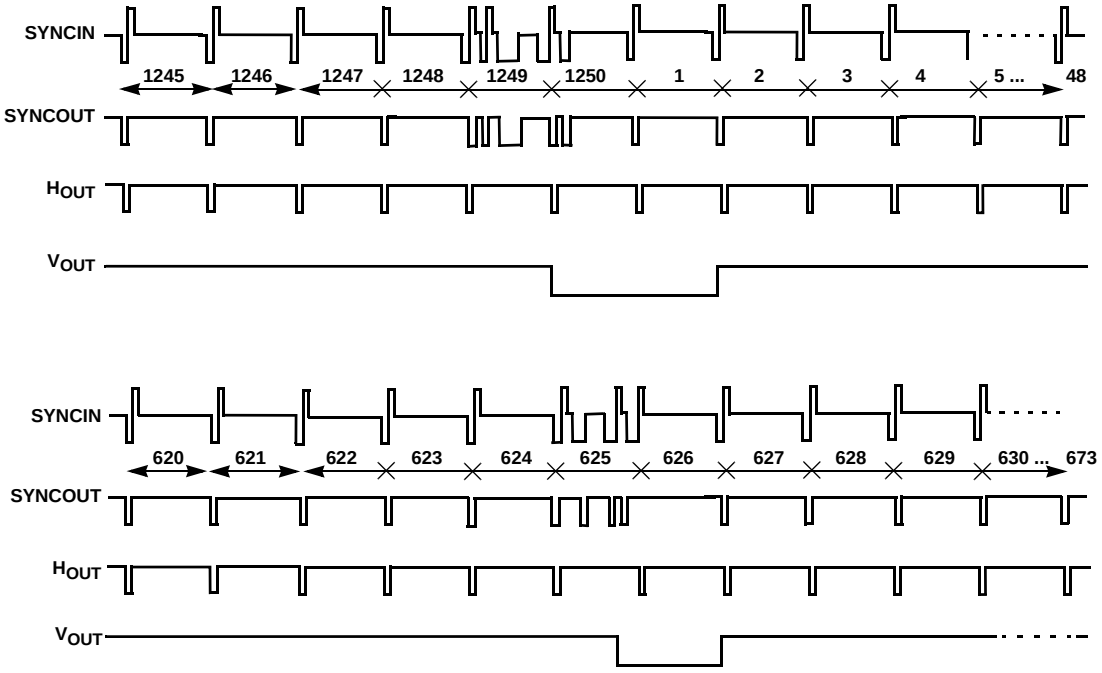


FIGURE 13. HDTV 1080I/25 LINE COMPOSITE VIDEO: INTERLACED (1250 LINES)

CONDITIONS: V_{DD} = 3.3V/5V, T_A = +25°C

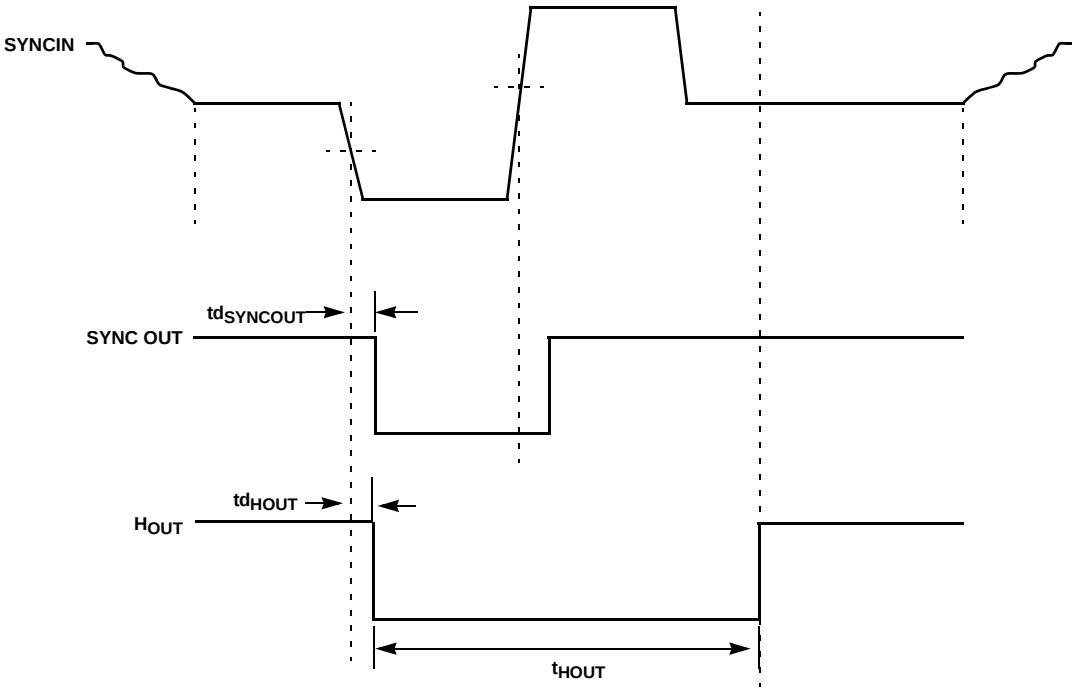


FIGURE 14. HORIZONTAL INTERVAL (HDTV) (720p)

H Timing for HDTV, No Filter (using 720p input signal)

PARAMETER	DESCRIPTION	CONDITIONS	TYP @ 3.3V (Note 8)	TYP @ 5V (Note 8)	UNIT
$td_{SYNCOUT}$	SYNCOUT Timing Relative to Input	(See Figure 14)	56	50	ns
td_{HOUT}	HOUT Timing Relative to Input	(See Figure 14)	48	36	ns
t_{HOUT}	Horizontal Output Width	(See Figure 14)	1.90	1.90	µs

NOTE:

8. Delay variation is less than 2.5ns over-temperature range.

CONDITIONS: V_{DD} = 3.3V/5V, T_A = +25°C

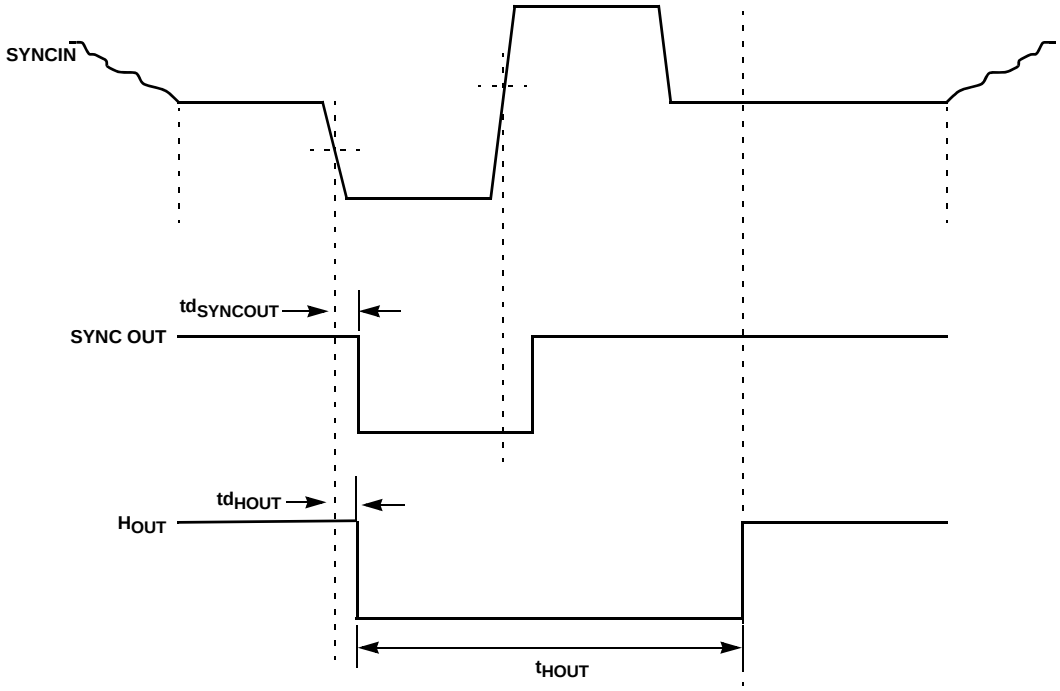


FIGURE 15. HORIZONTAL INTERVAL (HDTV) (720p)

H Timing for HDTV, With Filter (using 720p input)

PARAMETER	DESCRIPTION	CONDITIONS	TYP @ 3.3V (Note 9)	TYP @ 5V (Note 9)	UNIT
$td_{SYNCOUT}$	SYNCOUT Timing Relative to Input	(See Figure 15)	120	110	ns
td_{HOUT}	HOUT Timing Relative to Input	(See Figure 15)	112	100	ns
t_{HOUT}	Horizontal Output Width	(See Figure 15)	200	200	ns

NOTE:

9. Delay variation is less than 2.5ns over-temperature range.

Applications Information

Video In

The “Simplified Block Diagram” is shown on page 12.

An AC coupled video signal is input to Video In pin 2 via C_1, nominally 0.1µF. Clamp charge current will prevent the signal on pin 2 from going any more negative than Sync Tip Ref, about 1.5V. This charge current is nominally about 1mA. A clamp discharge current of about 10µA is always attempting to discharge C_1 to Sync Tip Ref, thus charge is lost between sync pulses that must be replaced during sync pulses. The droop voltage that will occur can be calculated from IT = CV, where V is the droop voltage, I is the discharge current, t is the time between sync pulses (sync period - sync tip width), and C is C_1.

An NTSC video signal has a horizontal frequency of 15.73kHz, and a sync tip width of 4.7µs. This gives a period of 63.6µs and a time t = 58.9µs. The droop voltage will then be V = 5.9mV. This is less than 2% of a nominal sync tip amplitude of 286mV. The charge represented by this droop is replaced in a time given by t = CV/I, where I = clamp charge current = 5.3mA. Here t = 590ns, about 12% of the sync pulse width of 4.7µs. It is important to choose C_1 large enough so that the droop voltage does not approach the switching threshold of the internal comparator.

Composite Sync

The Composite Sync output is simply a reproduction of the input signal with the active video removed. The sync tip of the Composite video signal is clamped to 1.5V at pin 2 and then slices at 70mV above the sync tip reference. The output signal is buffered out to pin 1. When loss of sync, the Composite Sync output is held low.

Vertical Sync

A low-going Vertical Sync pulse is output during the start of the vertical cycle of the incoming video signal. The vertical cycle starts with a pre-equalizing phase of pulses with a duty cycle of about 93%, followed by a vertical serration phase that has a duty cycle of about 15%. Vertical Sync is clocked out of the ISL59885 on the first rising edge during the vertical serration phase. In the absence of vertical serration pulses, a vertical sync pulse will be forced out after the vertical sync default delay time, approximately 60µs after the last falling edge of the vertical equalizing phase.

Horizontal Sync

The horizontal circuit senses the composite sync edges and produces the true horizontal pulses of nominal width 5.2µs. The leading edge is triggered from the leading edge of the input H sync with the same propagation delay as composite sync. The half line pulses present in the input signal during vertical blanking are removed with an internal 2H line eliminator circuit. This is a circuit that inhibits horizontal output pulses until 75% of the line time is reached, then the horizontal output operation is enabled again. Any signals present on the I/P signal after the true H sync will be ignored, thus the horizontal output will not be effected by MacroVision copy protection. When there is a loss of sync, the Horizontal Sync output is held high.

C_{SET}

An external C_{SET} capacitor connected from CSET pin 6 to ground. C_{SET} capacitor should be a X7R grade or better as the Y5U general use capacitors may be too leaky and cause faulty operation. The C_{SET} capacitor should be very close to the CSET pin to reduce possible board leakage. 56nF is recommended. The “C_{SET} Bias Circuit” is shown on page 12. The C_{SET} capacitor rectifies a 5µs pulse current and creates a voltage on C_{SET}. The C_{SET} voltage is converted to bias current for H_{SYNC} and V_{SYNC} timing.

Chroma Filter

A chroma filter is suggested to increase the S/N ratio of the incoming video signal. Use of the optional chroma filter is shown in Figure16. It can be implemented very simply and inexpensively with a series resistor of 100Ω and a capacitor of 570pF, which gives a single pole roll-off frequency of about 2.79MHz during NTSC or PAL. This sufficiently attenuates the 3.58MHz (NTSC) or 4.43MHz (PAL) color burst signal, yet passes the approximately 15kHz sync signals without appreciable attenuation. During HDTV, the transistor turns off and a 100pF capacitor is left to filter any noise present at the input. A chroma filter will increase the propagation delay from the composite input to the outputs.

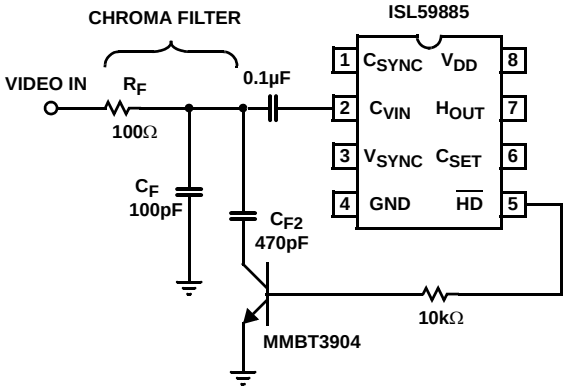
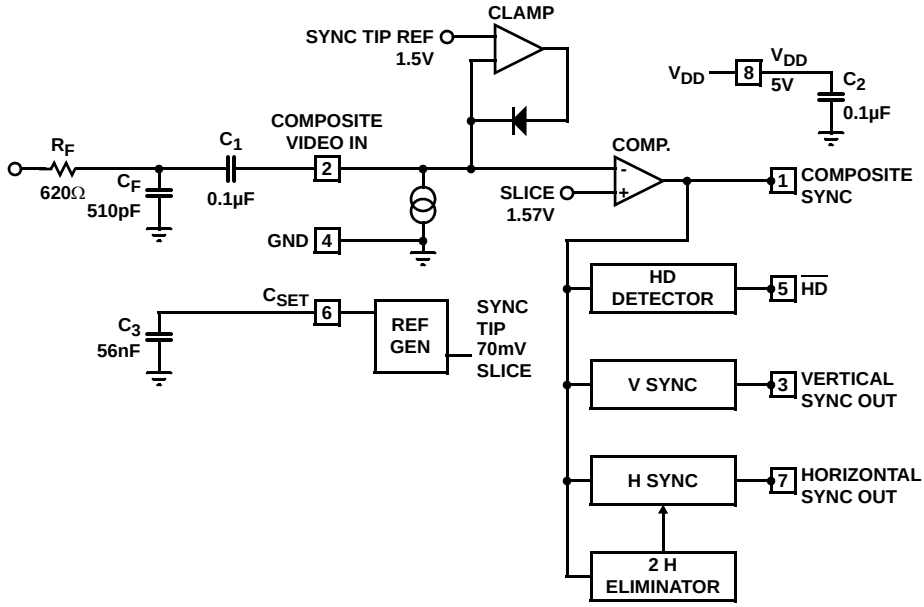


FIGURE 16. OPTIONAL CHROMA FILTER

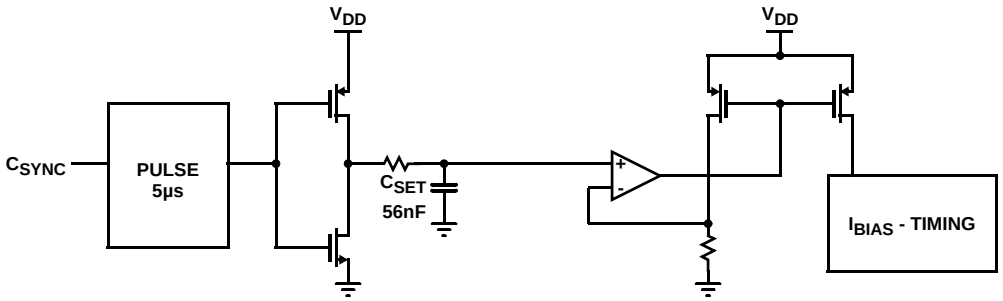
HD-Detect

High definition video is flagged by $\overline{HD}$ going low when the input horizontal frequency is greater than 20kHz.

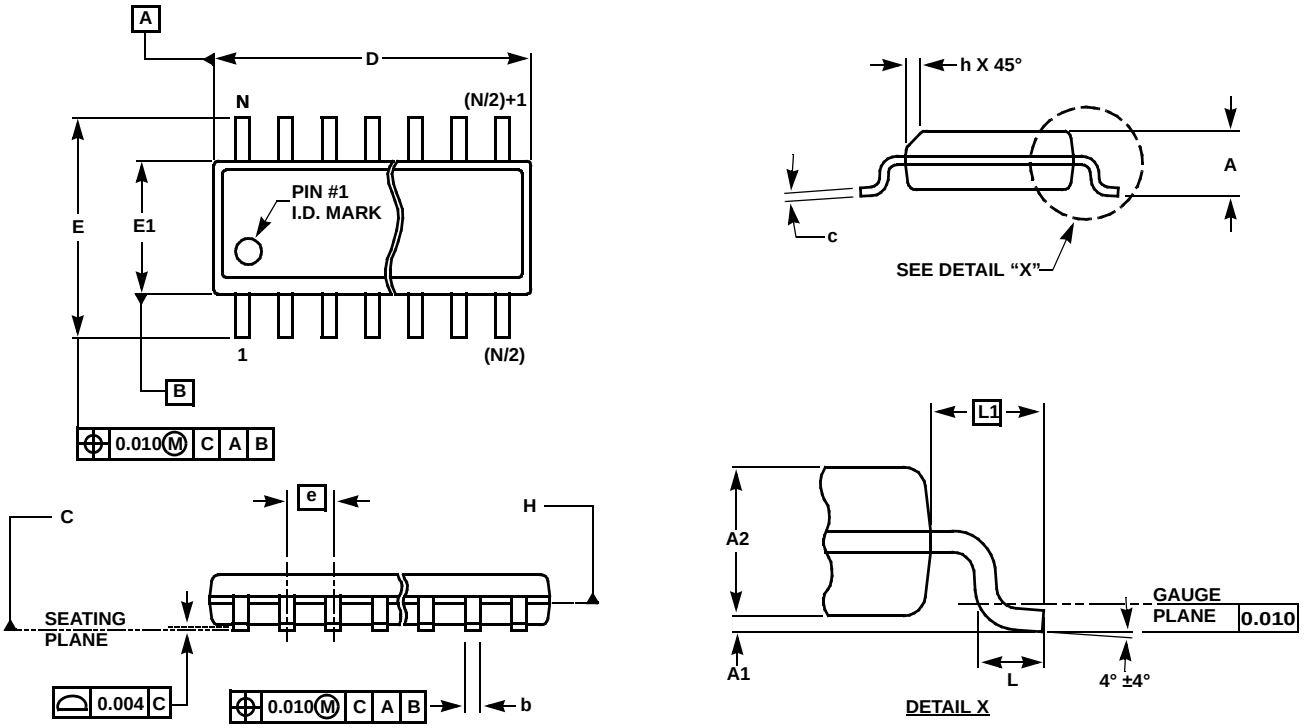
Simplified Block Diagram



C_{SET} Bias Circuit



Small Outline Package Family (SO)



MDP0027

SMALL OUTLINE PACKAGE FAMILY (SO)

SYMBOL	INCHES							TOLERANCE	NOTES
	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)		
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX	-
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	±0.003	-
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	±0.002	-
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	±0.003	-
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	±0.001	-
D	0.193	0.341	0.390	0.406	0.504	0.606	0.704	±0.004	1, 3
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	±0.008	-
E1	0.154	0.154	0.154	0.295	0.295	0.295	0.295	±0.004	2, 3
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic	-
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	±0.009	-
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic	-
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference	-
N	8	14	16	16	20	24	28	Reference	-

Rev. M 2/07

NOTES:

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994