Low Noise, Fixed Output Voltage 300mA LDO Regulator

FEATURES

- Guaranteed 300mA output
- Ultra low output noise
- Output voltage accuracy: ±2%
- Low ground current: 90µA
- Very low dropout: 380mV @ 300mA
- Zero shutdown supply current
- TTL-logic-controlled enable input
- Thermal and current limit protections
- Compatible with low ESR capacitor to achieve ultra low droop load transient response
- Ultra fast line transient response
- Low profile 5-lead SOT-25 package
- Fixed options from 1.5V to 5.0V with 100mV steps

APPLICATIONS

- Cellular and cordless phones
- PDAs
- Battery powered portable equipment
- Notebook computers
- PC peripherals
- Wireless LAN cards
- Bluetooth devices

DESCRIPTION

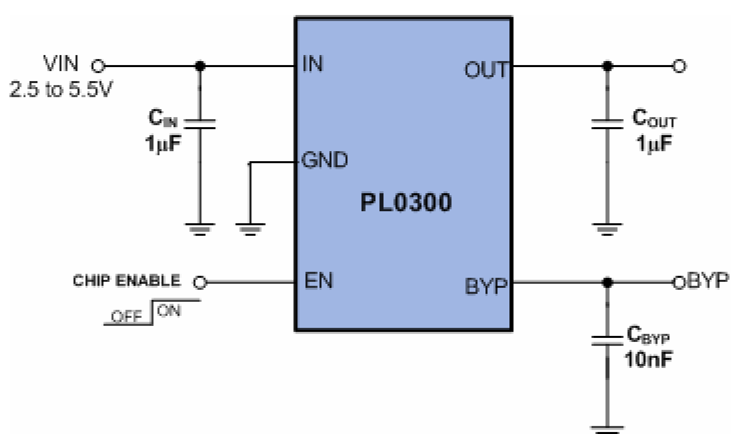
The PL0300/P is a CMOS low dropout linear regulator with ultra-low-noise output, very low dropout voltage and very low ground current.

The PL0300/P operates from a 2.5V to 5.5V input voltage range and delivers up to 300mA, with low dropout of 380mV at 300mA. Other features of the PL0300/P include short-circuit protection and thermal-shutdown protection.

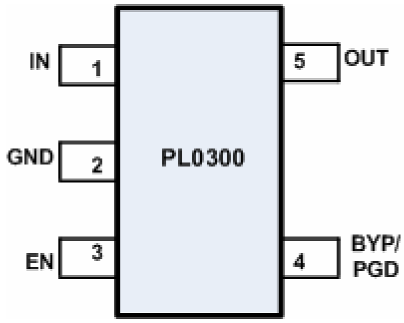
The PL0300/P is designed especially for battery-powered portable devices. Its reference bypass pin improves low noise performance which makes it ideal for noise-sensitive RF and personal communication applications. Other key application areas for the PL0300/P include handheld computers, PCMCIA cards and WLAN cards.

The PL0300/P is available in small 5-lead SOT-25 package.

TYPICAL APPLICATION CIRCUIT



PIN CONFIGURATION



PIN DESIGNATOR

Name	Pin	Type	Function
IN	1	Supply	Supply voltage. 2.5V ~ 5.5V
GND	2	Ground	Ground pin
EN	3	Logic input	Enable/Shutdown. TTL and CMOS compatible input. Logic 'H': enable, logic 'L': shutdown
BYP/ PGD	4	Bypass/PGood	Reference voltage bypass pin. Connect 0.01μF ≤ C_{BYP} ≤ 0.1μF to GND to reduce output noise. May be left open
OUT	5	Analog output	Regulator output

PIN DESCRIPTION

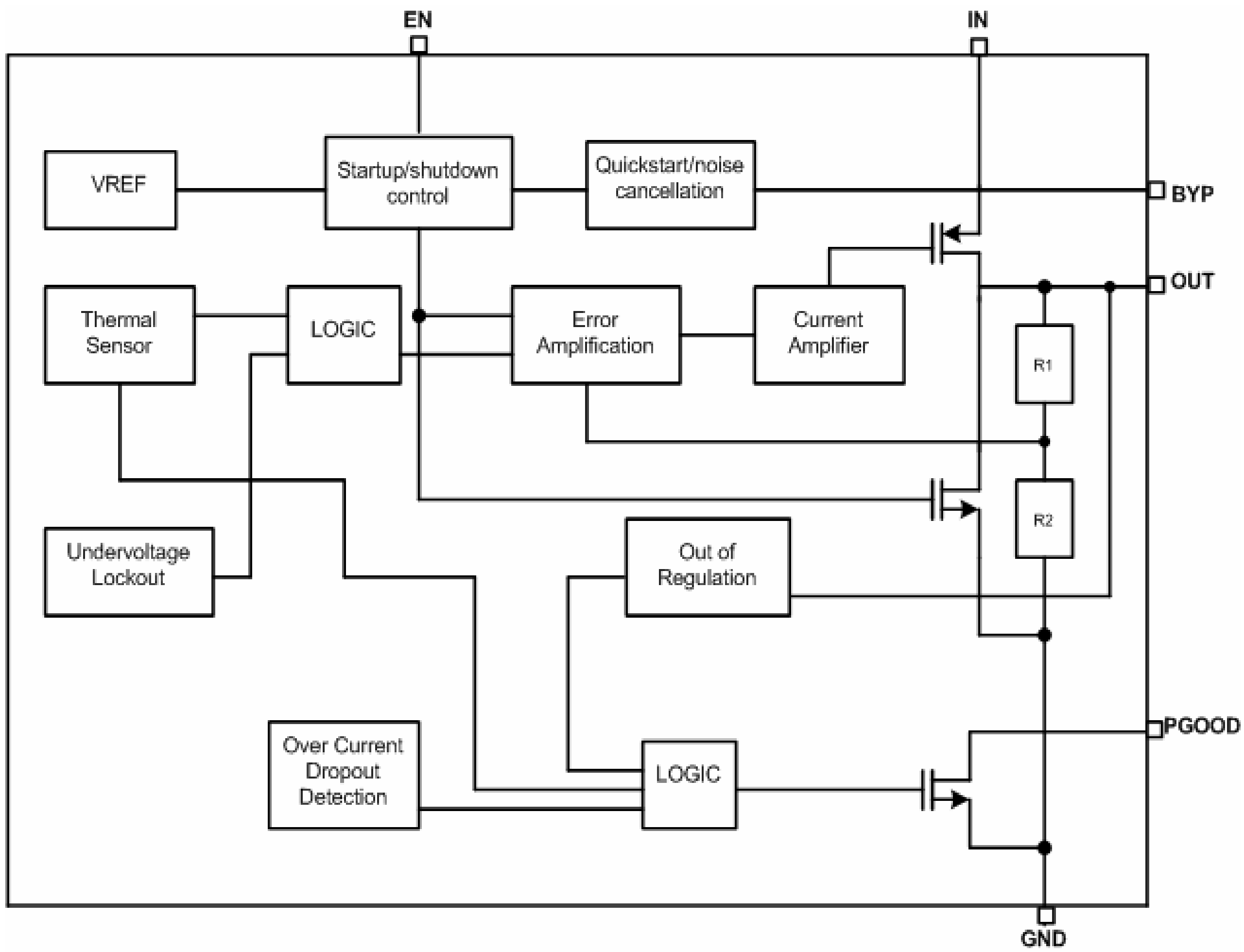
PL0300

Name	Pin	Type	Function
IN	1	Supply	Supply voltage. 2.5 ~ 5.5V
GND	2	Ground	Ground
EN	3	Logic input	TTL and CMOS compatible input. Logic 'H': enable, logic 'L': shutdown
BYP	4	Bypass	Noise filtering pin
OUT	5	Analog output	Regulator output

PL0300P

Name	Pin	Type	Function
IN	1	Supply	Supply voltage. 2.5 ~ 5.5V
GND	2	Ground	Ground
EN	3	Logic input	TTL and CMOS compatible input. Logic 'H': enable, logic 'L': shutdown
PGD	4	Power good	Monitors the output voltage and signals an error condition when the output voltage drops 10% below its nominal value
OUT	5	Analog output	Regulator output

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{IN}	DC Supply Voltage at Pin 1	-0.3 to +6.0	V
V_{EN}	Enable Input Voltage at Pin 3	-0.3 to +6.0	V
P_D	Continuous Power Dissipation	Internally limited	W
T_{STG}	Storage Temperature Range	-65 to +150	°C
$R_{\theta JA}$	Thermal Resistance, Junction-To-Air	+235	°C/W
$T_{J,MAX}$	Operating Junction Temperature	-40 to +125	°C
T_L	Lead Temperature (Soldering, 5sec)	+260	°C
ESD	ESD Capability, HBM Model	2.0	KV

ELECTRICAL CHARACTERISTICS

(All specifications are at T_A = 25°C. $V_{IN} = V_{OUT\ (NOMINAL)}$ + 1V OR 2.5V whichever is greater, $V_{EN} = V_{IN}$, $C_{IN} = C_{OUT}$ = 1μF, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN}	Supply Voltage		2.5		5.5	V
V_{OUT}	Output Voltage Accuracy	I_O = 1mA to 300mA, T_A = +25°C	-2.0		+2.0	%
		I_O = 1mA to 300mA, T_A = -40°C to 85°C	-3.0		+3.0	%
V_{DP}	Dropout Voltage (Note 1)	I_{LOAD} = 300mA		380		mV
		I_{LOAD} = 100mA		130		mV
I_{MAX}	Maximum Output Current	Continuous	300			mA $_{RMS}$
I_{LIM}	Short Circuit Current Limit	V_{OUT} < 90% of V_{NOM}		650		mA
I_Q	Shutdown Quiescent Current	V_{EN} < 0.4V		0.05	0.5	μA
I_G	Ground Pin Current	I_{LOAD} = 1mA		90	140	μA
ΔV_{LINE}	Line Regulation dV_{OUT}/dV_{IN}	$V_{IN} = V_{OUT}$ + 1V (or 2.5V, whichever is greater) to 5.5V, I_O = 1 mA	-0.15		0.15	%/V
PSRR	Ripple Rejection	f = 100Hz, C_{OUT}= 10μF, C_{BYP} = 10nF, I_{LOAD} = 1mA		65		dB
e_{NO}	Output Voltage Noise	C_{OUT} = 10μF, C_{BYP} = 10nF, f = 10Hz to 100KHz		70		$μV_{RMS}$

OVER TEMPERATURE PROTECTION

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
	Thermal Shutdown Temperature			165		°C
	Thermal Shutdown Hysteresis			15		°C

ENABLE INPUT

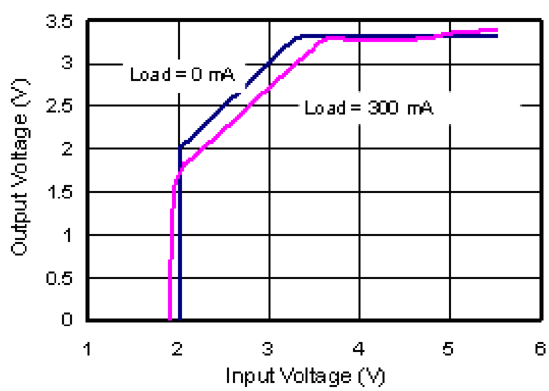
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IH}	Logic Input High Voltage		1.6			V
V_{IL}	Logic Input Low Voltage				0.4	V
I_{EN}	Logic Input Current		-0.5		0.5	µA
	Shutdown Exit Delay	V_{EN} = 0 to 5.5V, C_{BYP} = 10nF, C_{OUT} = 1µF		25		µS
	Shutdown Discharge Resistance			900		Ω

Note 1: The Dropout Voltage is defined as V_{IN} - V_{OUT}, when $V_{IN} = V_{OUT\,(NOM)}$

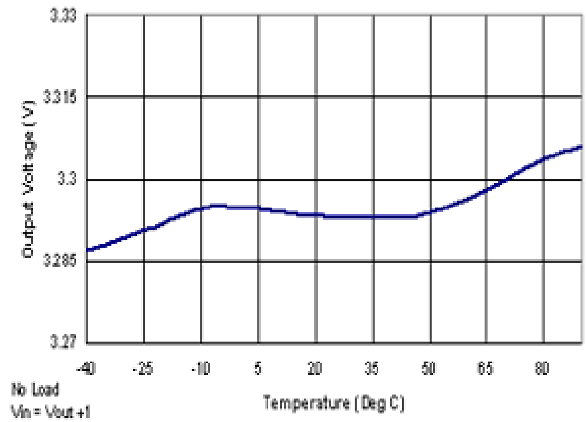
TYPICAL OPERATING CHARACTERSTICS

(All specifications are at T_A = 25°C , unless otherwise specified)

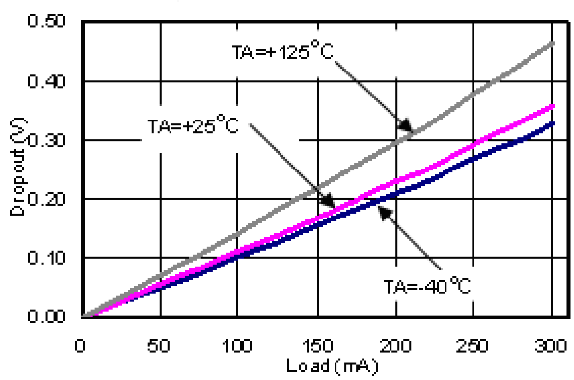
Output Voltage vs Input Voltage



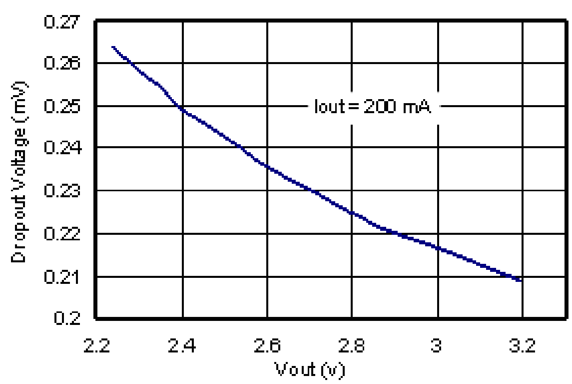
Output Voltage vs Temperature



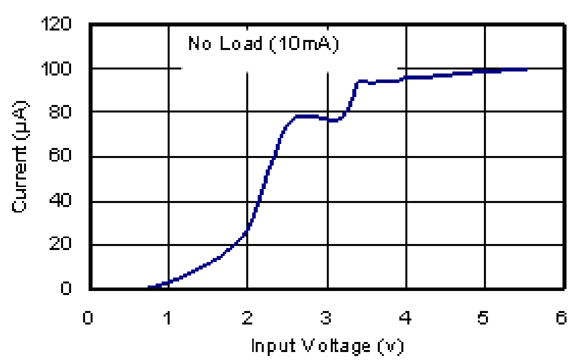
Dropout Voltage vs Load



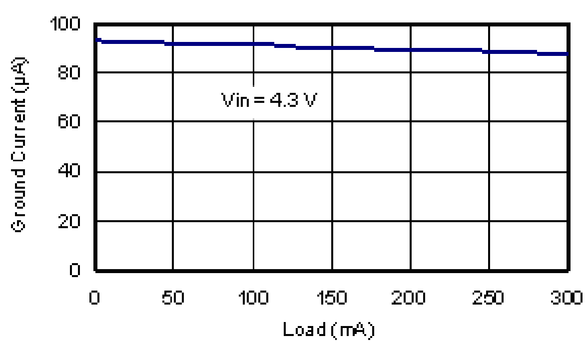
Dropout Voltage vs Output Voltage



Ground Current vs Input Voltage



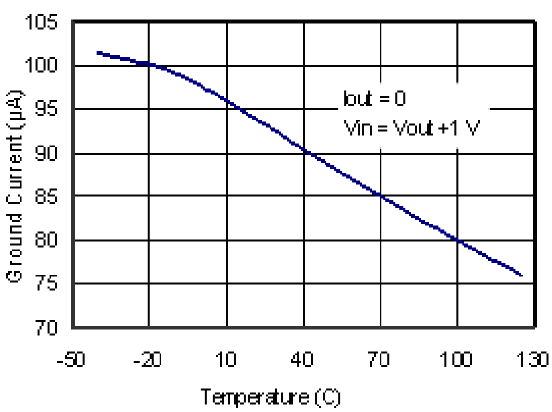
Ground Current vs Load Current



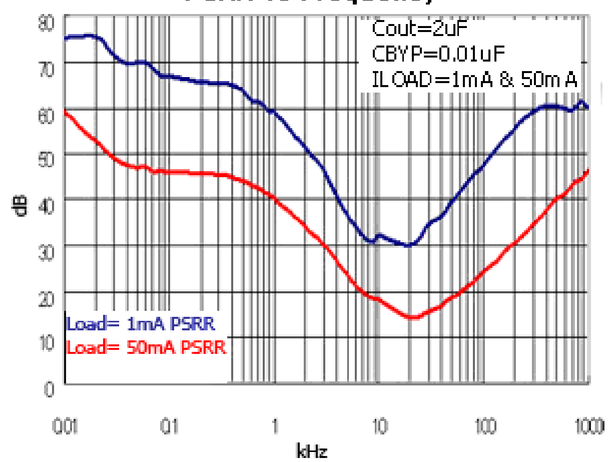
TYPICAL OPERATING CHARACTERSTICS (continued)

(All specifications are at T_A = 25°C , unless otherwise specified)

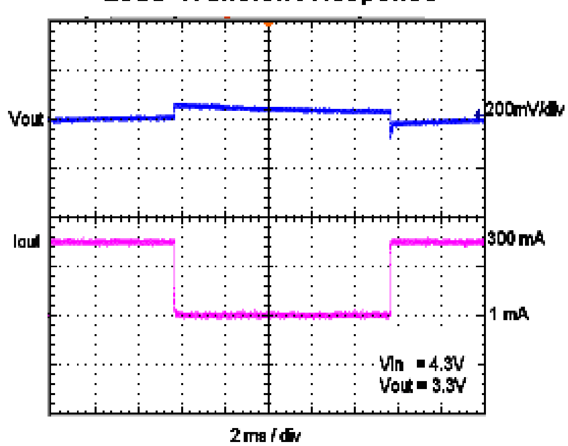
Ground Current vs Temperature



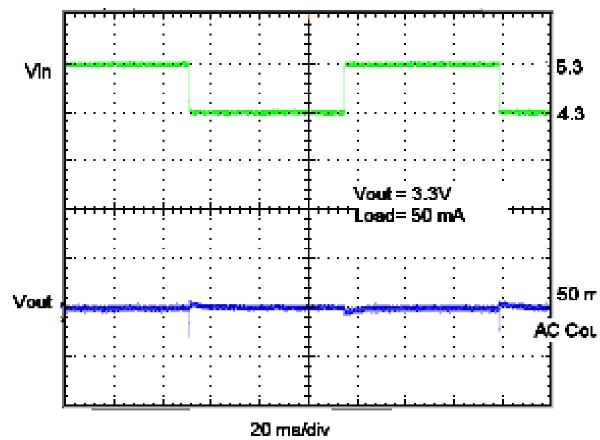
PSRR vs Frequency



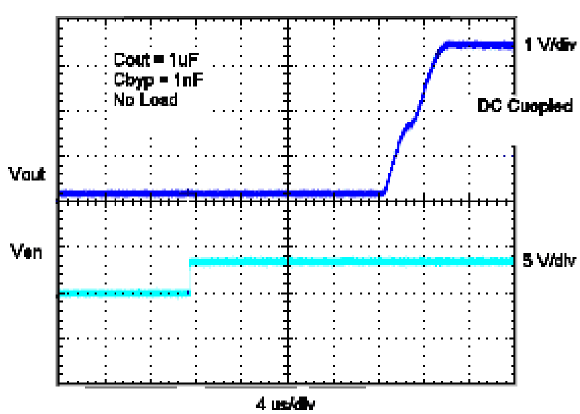
Load-Transient Response



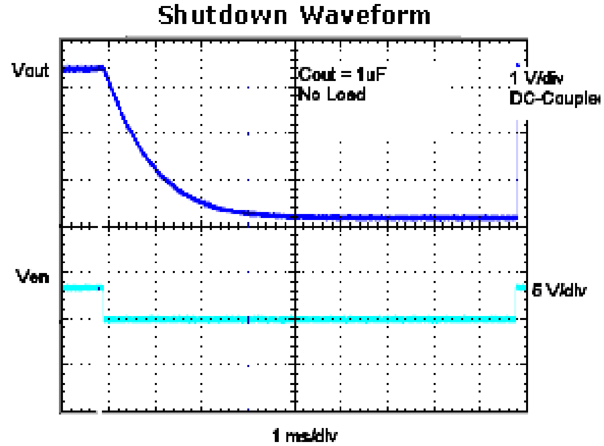
Line Transient Response



Shutdown Delay



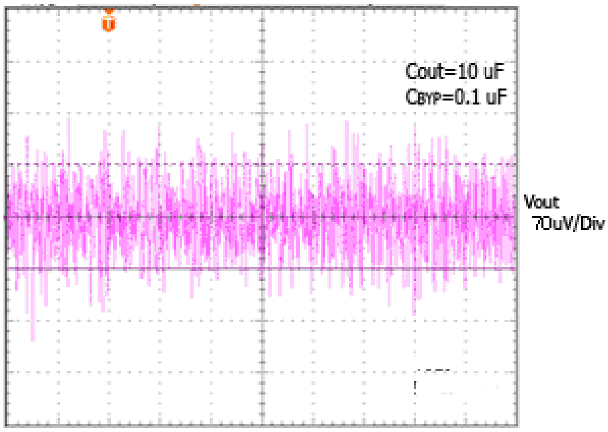
Shutdown Waveform



TYPICAL OPERATING CHARACTERSTICS (continued)

(All specifications are at T_A = 25°C , unless otherwise specified)

Noise In Time Domain



Vin =4.5V, Vout =3.3V, ILOAD =10mA

OPERATION

The PL0300/P is an ultra-low-noise, low-dropout, low-quiescent current linear regulator designed for space-restricted applications. It is available with preset output voltages ranging from 1.5V to 5.0V in 100mV increments. It can supply loads of up to 300mA. As shown in the Block Diagram, the PL0300/P consists of a highly accurate band gap core, noise bypass circuit, error amplifier, P-channel pass transistor and an internal feedback voltage divider. The PL0300/P allows for an adjustable output with an external feedback network. The 1.0V band gap reference is connected to the error amplifier's inverting input. The error amplifier compares this reference with the feedback voltage and amplifies the difference. If the feedback voltage is lower than the reference voltage, the pass transistor gate is pulled low. This allows more current to pass to the output and increases the output voltage. If the feedback voltage is too high, the pass transistor gate is pulled high, allowing less current to pass to the output. The output voltage is fed back through an internal resistor voltage-divider connected to the OUT pin. An external bypass capacitor connected to BYP (PL0300/P-BYP) reduces the noise at the output. Additional blocks include a current limiter, over temperature protection and shutdown logic.

Internal P-Channel Pass Transistor

The PL0300/P features a 1Ω (typical) P-channel MOSFET pass transistor. This provides several advantages over similar designs using a PNP pass transistor, including longer battery life. The P-channel MOSFET requires no base drive, which considerably reduces the quiescent current. PNP-based regulators waste considerable current in dropout when the pass transistor saturates. They also use high base-drive current under heavy loads.

The PL0300/P does not suffer from these problems and consumes only 90µA of quiescent current.

Current Limit

The PL0300/P includes a current limiter. It monitors the output current and controls the pass transistor's gate voltage to limit the output current under 550mA (typical). The output can be shorted to ground for an indefinite amount of time without damaging the part.

The short circuit current limit is increased to approximately 650mA (typical) when the output voltage is within 10% of the nominal output, thus improving the performance of large pulsating loads. The in-regulation current limit option provides the user to overload the device, maintaining a continuous 300mA (RMS) load.

Enable Input

The PL0300/P features an active-high Enable input (EN) pin that allows on/off control of the regulator. The PL0300/P bias current reduces to ZERO (leakage current) when it goes into shutdown. The Enable input is TTL/CMOS compatible for simple logic interfacing. When EN is 'H,' the output voltage startup rising time is typically 25µs. Connect EN pin to IN pin for normal operation.

Power Good Flag (Applicable for PL0300P)

The PL0300/P features a Power Good flag (PGD), which monitors the output voltage and signals an error condition when the output voltage drops 10% below its nominal value.

Under Voltage Lockout

When the input supply goes too low (typically below 2.0V), the PL0300/P produces an internal UVLO (Under Voltage Lockout) signal that generates a fault signal and shuts down the chip. This mechanism protects the chip from producing false logic due to low input supply.

APPLICATION INFORMATION

Quick Charging Mode
The PL0300/P has a quick charge block to get the reference up very quickly by charging the BYP capacitor with very high current when the chip comes out of shut down. This quick charge block stops charging the BYP capacitor when the reference reaches 95% of its nominal value and then the chip switches out of quick charging mode to normal operating mode.

Over Temperature Protection
Over temperature protection limits the total power dissipation in the PL0300/P. When the junction temperature exceeds T_J = +165°C, the thermal sensor signals the shutdown logic and turns off the pass transistor. The thermal sensor turns the pass transistor on again after the IC's junction temperature drops by 15°C, resulting in a pulsed output during continuous thermal-overload conditions.

Thermal-overload protection is designed to protect the PL0300/P in the event of a fault condition. For continuous operation, do not exceed the absolute maximum junction temperature rating of T_J = +150°C.

Operating Region and Power Dissipation
The PL0300/P's maximum power dissipation depends on (1) the thermal resistance of the case and circuit board, (2) the temperature difference between the die junction and ambient and (3) the rate of airflow. The power dissipation across the device is:

$$P = I_{OUT} \times (V_{IN} - V_{OUT})$$

The maximum power dissipation is:

$$P_{MAX} = (T_J - T_A)/(\theta_{JC} + \theta_{CA})$$

Where $(T_J - T_A)$ is the temperature difference between the PL0300/P die junction and the surrounding air, θ_{JC} is the thermal resistance of the package and θ_{CA} is the thermal resistance through the PC board, copper traces and other materials to the surrounding air.
The GND pin of the PL0300/P performs the dual function of providing an electrical connection to ground and channeling heat away. Connect the GND pin to ground using a large pad or ground plane.

Noise Reduction
For the PL0300/P, an external 0.01μF bypass capacitor between BYP and GND with innovative noise bypass scheme reduces the output noises dramatically, exhibiting 70μV(RMS) of output voltage noise with C_{BYP} = 0.01μF and C_{OUT} = 10μF.

Capacitor Selection And Regulator Stability
Use a 1.0μF capacitor on the PL0300/P input and a 1.0μF capacitor on the output. Large input capacitor values and lower ESR provide better noise rejection and line-transient response.

Reduce output noise and improve load-transient response, stability and power-supply rejection by using large output capacitors. Note that some ceramic dielectrics exhibit large capacitance and ESR variation with temperature. With dielectrics such as Z5U and Y5V, it may be necessary to use a 2.2μF or larger output capacitor to ensure stability at temperatures below -10°C. With X7R or X5R dielectrics, 1μF is sufficient at all operating temperatures.

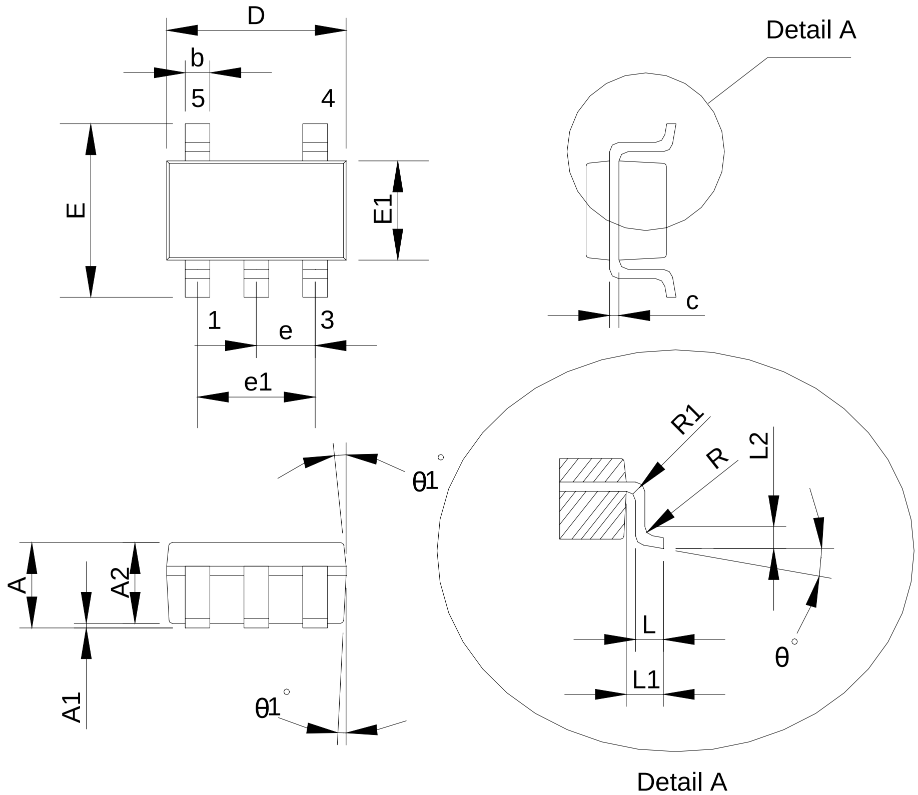
Use a 0.01μF bypass capacitor at BYP (PL0300/P-BYP) for low-output voltage noise. The leakage current going into the BYP pin should be less than 10nA.

Noise, PSRR and Transient Response
The PL0300/P is designed to deliver ultra-low noise and high PSRR, as well as low dropout and low quiescent currents in battery-powered systems. The PL0300/P PSRR is 68dB at 100Hz and 60dB at 10KHz.
When operating from sources other than batteries, improved supply-noise rejection and transient response can be achieved by increasing the values of the input and output bypass capacitors and through passive filtering techniques.

Dropout Voltage
A regulator's minimum dropout voltage determines the lowest usable supply voltage. In battery-powered systems, this determines the useful end-of-life battery voltage. Because the PL0300/P uses a P-channel MOSFET pass transistor, its dropout voltage is a function of drain-to-source on resistance (RDS_{ON}) multiplied by the load current.

PACKAGE INFORMATION

5-PIN SOT-25 OUTLINE DIMENSION



Dimension:

Symbol	Millimeter			Inch		
	Min	Typ	Max	Min	Typ	Max
A			1.45			0.057
A1			0.15			0.006
A2	0.90	1.15	1.30	0.036	0.045	0.051
b	0.30		0.50	0.011		0.020
c	0.08		0.22	0.003		0.009
D		2.90			0.114	
E		2.80			0.110	
E1		1.60			0.063	
e		0.95			0.037	
e1		1.90			0.075	
L	0.30	0.45	0.60	0.020	0.018	0.024
L1		0.60			0.024	
L2		0.25			0.010	
R	0.10			0.004		
R1	0.10		0.25	0.004		0.010
θ°	0°	4°	8°	0°	4°	8°
θ1°	5°	10°	15°	5°	10°	15°

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