# CY62148EV30 MoBL®

# 4-Mbit (512K x 8) Static RAM

## Features

- Very high speed: 45 ns
  - Wide voltage range: 2.20V – 3.60V
- Pin compatible with CY62148DV30
- Ultra low standby power
  - Typical standby current: 1 µA
  - Maximum standby current: 7 µA (Industrial)
- Ultra low active power
  - Typical active current: 2 mA @ f = 1 MHz
- Easy memory expansion with $\overline{CE}$, and $\overline{OE}$ features
- Automatic power down when deselected
- CMOS for optimum speed and power
- Available in Pb-free 36-ball VFBGA, 32-pin TSOP II and 32-pin SOIC [1] packages

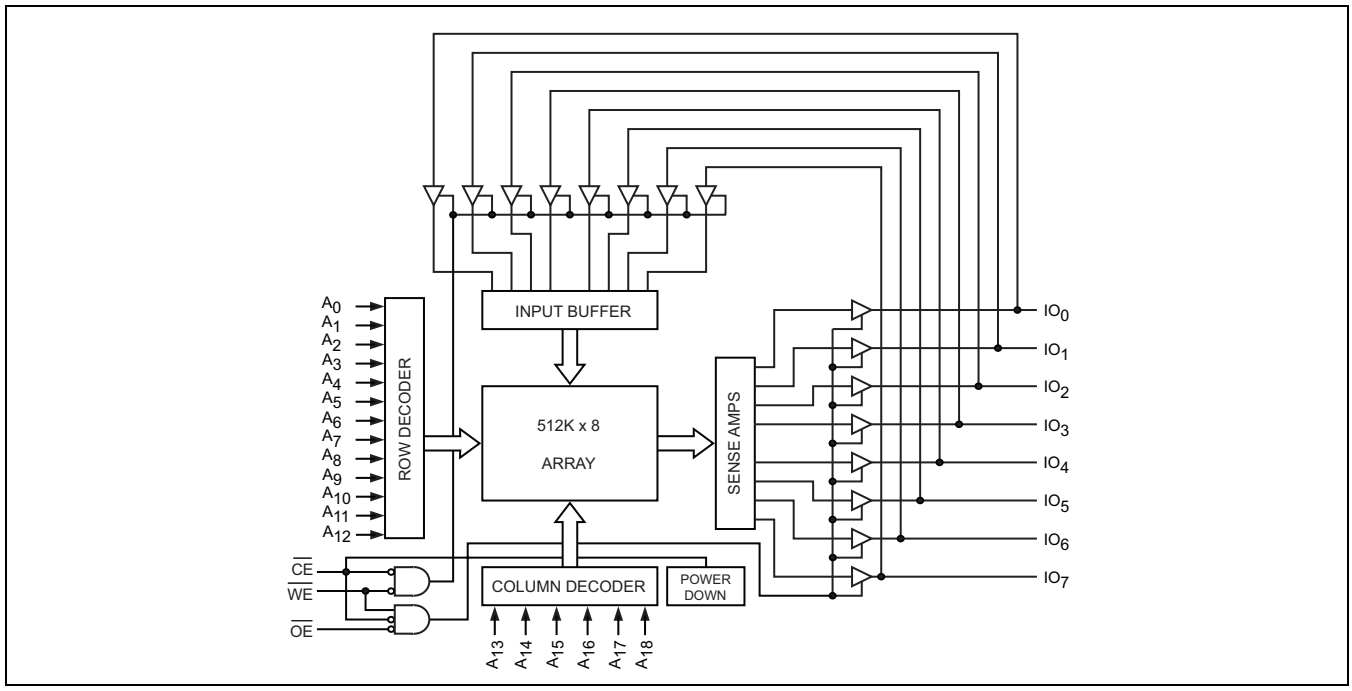
## Functional Description [2]

The CY62148EV30 is a high performance CMOS static RAM organized as 512K words by 8 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption. Placing the device into standby mode reduces power consumption by more than 99% when deselected ($\overline{CE}$ HIGH). The eight input and output pins ($IO_0$ through $IO_7$) are placed in a high impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}$ LOW and $\overline{WE}$ LOW).

To write to the device, take Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. Data on the eight IO pins ($IO_0$ through $IO_7$) is then written into the location specified on the address pins ($A_0$ through $A_{18}$).

To read from the device, take Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing Write Enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the IO pins.

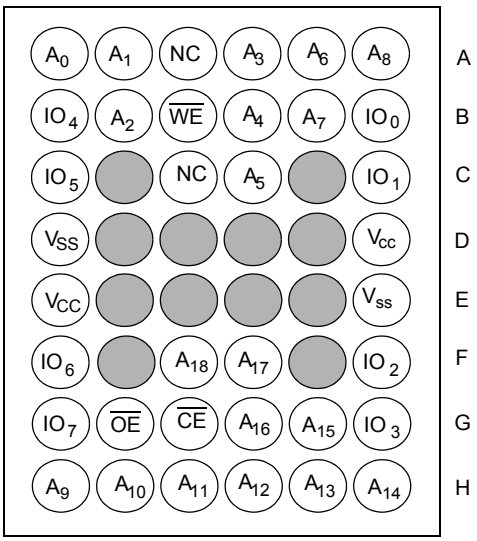
## Logic Block Diagram



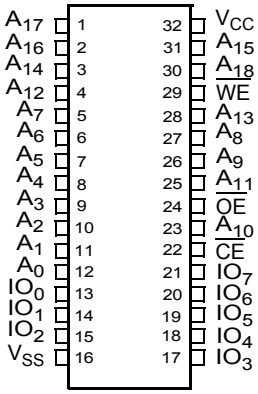

**Notes**
1. SOIC package is available only in 55 ns speed bin.
2. For best practice recommendations, refer to the Cypress application note “System Design Guidelines” at http://www.cypress.com.

## Pin Configuration [1, 3]

**36-Ball VFBGA Pinout**
**Top View**




**32-Pin SOIC/TSOP II Pinout**
**Top View**




## Product Portfolio

| Product | | Range | $V_{CC}$ Range (V) | | | Speed (ns) | Power Dissipation | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | Operating $I_{CC}$ (mA) | | | | Standby $I_{SB2}$ (µA) | |
| | | | | | | | f = 1 MHz | | f = $f_{max}$ | | | |
| | | | Min | Typ[4] | Max | | Typ[4] | Max | Typ[4] | Max | Typ[4] | Max |
| CY62148EV30LL | VFBGA | Industrial | 2.2 | 3.0 | 3.6 | 45 | 2 | 2.5 | 15 | 20 | 1 | 7 |
| | TSOP II | | | | | | | | | | | |
| CY62148EV30LL | SOIC | Industrial | 2.2 | 3.0 | 3.6 | 55 | 2 | 2.5 | 15 | 20 | 1 | 7 |

**Notes**
3. NC pins are not connected on the die.
4. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25°C$.

## Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... 55°C to +125°C

Supply Voltage to Ground Potential ..... –0.3V to $V_{CC(max)}$ + 0.3V

DC Voltage Applied to Outputs in High-Z State [5, 6] ..... –0.3V to $V_{CC(max)}$ + 0.3V

DC Input Voltage [5, 6] ..... –0.3V to $V_{CC(max)}$ + 0.3V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... > 2001V (MIL-STD-883, Method 3015)

Latch up Current ..... > 200 mA

## Operating Range

| Product | Range | Ambient Temperature | $V_{CC}$ [7] |
|---|---|---|---|
| CY62148EV30 | Industrial | –40°C to +85°C | 2.2V to 3.6V |

## Electrical Characteristics (Over the Operating Range)

| Parameter | Description | Test Conditions | | 45 ns | | | 55 ns [1] | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ[4] | Max | Min | Typ[4] | Max | |
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = –0.1 mA | | 2.0 | | | 2.0 | | | V |
| | | $I_{OH}$ = –1.0 mA, $V_{CC} \geq$ 2.70V | | 2.4 | | | 2.4 | | | V |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 0.1 mA | | | | 0.4 | | | 0.2 | V |
| | | $I_{OL}$ = 2.1 mA, $V_{CC} \geq$ 2.70V | | | | 0.4 | | | 0.4 | V |
| $V_{IH}$ | Input HIGH Voltage | $V_{CC}$ = 2.2V to 2.7V | | 1.8 | | $V_{CC}$ + 0.3V | 1.8 | | $V_{CC}$ + 0.3V | V |
| | | $V_{CC}$= 2.7V to 3.6V | | 2.2 | | $V_{CC}$ + 0.3V | 2.2 | | $V_{CC}$ + 0.3V | V |
| $V_{IL}$ | Input LOW Voltage | $V_{CC}$ = 2.2V to 2.7V | For VFBGA and TSOP II package | –0.3 | | 0.6 | | | | V |
| | | | For SOIC package | | | | –0.3 | | 0.4 [8] | V |
| | | $V_{CC}$ = 2.7V to 3.6V | For VFBGA and TSOP II package | –0.3 | | 0.8 | | | | V |
| | | | For SOIC package | | | | –0.3 | | 0.6 [8] | |
| $I_{IX}$ | Input Leakage Current | GND $\leq V_I \leq V_{CC}$ | | –1 | | +1 | –1 | | +1 | µA |
| $I_{OZ}$ | Output Leakage Current | GND $\leq V_O \leq V_{CC}$, Output Disabled | | –1 | | +1 | –1 | | +1 | µA |
| $I_{CC}$ | $V_{CC}$ Operating Supply Current | f = $f_{max}$ = $1/t_{RC}$ | $V_{CC}$ = $V_{CC(max)}$, $I_{OUT}$ = 0 mA, CMOS levels | | 15 | 20 | | 15 | 20 | mA |
| | | f = 1 MHz | | | 2 | 2.5 | | 2 | 2.5 | |
| $I_{SB1}$ | Automatic CE Power Down Current — CMOS Inputs | $\overline{CE} \geq V_{CC}$ – 0.2V, $V_{IN} \geq V_{CC}$ – 0.2V, $V_{IN} \leq$ 0.2V f = $f_{max}$ (Address and Data Only), f = 0 (OE and WE), $V_{CC}$ = 3.60V | | | 1 | 7 | | 1 | 7 | µA |
| $I_{SB2}$ [9] | Automatic CE Power Down Current — CMOS Inputs | $\overline{CE} \geq V_{CC}$ – 0.2V, $V_{IN} \geq V_{CC}$ – 0.2V or $V_{IN} \leq$ 0.2V, f = 0, $V_{CC}$ = 3.60V | | | 1 | 7 | | 1 | 7 | µA |

**Notes**

5. $V_{IL(min)}$ = –2.0V for pulse durations less than 20 ns.
6. $V_{IH(max)}$ = $V_{CC}$ + 0.75V for pulse durations less than 20 ns.
7. Full device AC operation assumes a minimum of 100 µs ramp time from 0 to $V_{CC(min)}$ and 200 µs wait time after $V_{CC}$ stabilization.
8. Under DC conditions the device meets a $V_{IL}$ of 0.8V (for $V_{CC}$ range of 2.7V to 3.6V) and 0.6V (for $V_{CC}$ range of 2.2V to 2.7V). However, in dynamic conditions Input LOW voltage applied to the device must not be higher than 0.6V and 0.4V for the above ranges. This is applicable to SOIC package only. Please refer to AN13470 for details.
9. Only chip enable ($\overline{CE}$) must be HIGH at CMOS level to meet the $I_{SB2}$ / $I_{CCDR}$ spec. Other inputs can be left floating.

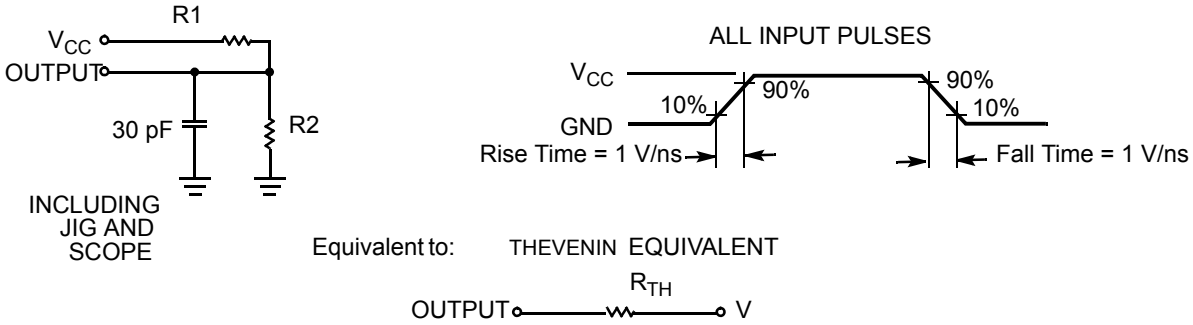
## Capacitance (For All packages) [10]

| Parameter | Description | Test Conditions | Max | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $T_A$ = 25°C, f = 1 MHz, $V_{CC} = V_{CC(typ)}$ | 10 | pF |
| $C_{OUT}$ | Output Capacitance | | 10 | pF |

## Thermal Resistance [10]

| Parameter | Description | Test Conditions | VFBGA Package | TSOP II Package | SOIC Package | Unit |
|---|---|---|---|---|---|---|
| $\Theta_{JA}$ | Thermal Resistance (Junction to Ambient) | Still Air, soldered on a 3 x 4.5 inch, two-layer printed circuit board | 72 | 75.13 | 55 | °C/W |
| $\Theta_{JC}$ | Thermal Resistance (Junction to Case) | | 8.86 | 8.95 | 22 | °C/W |

## AC Test Loads and Waveforms

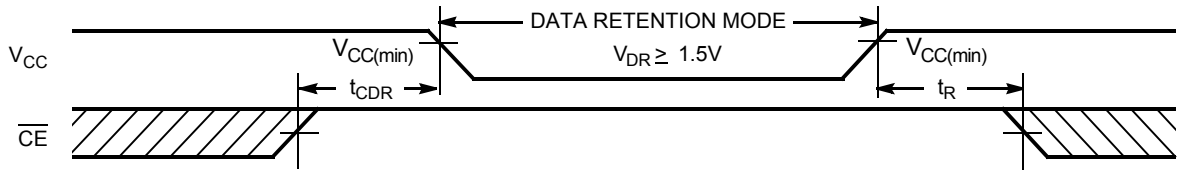



| Parameters | 2.50V | 3.0V | Unit |
|---|---|---|---|
| R1 | 16667 | 1103 | Ω |
| R2 | 15385 | 1554 | Ω |
| $R_{TH}$ | 8000 | 645 | Ω |
| $V_{TH}$ | 1.20 | 1.75 | V |

## Data Retention Characteristics (Over the Operating Range)

| Parameter | Description | Conditions | Min | Typ [4] | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DR}$ | $V_{CC}$ for Data Retention | | 1.5 | | | V |
| $I_{CCDR}$ [9] | Data Retention Current | $V_{CC}$ = 1.5V, $\overline{CE} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ | | 0.8 | 7 | µA |
| $t_{CDR}$ [10] | Chip Deselect to Data Retention Time | | 0 | | | ns |
| $t_R$ [11] | Operation Recovery Time | | $t_{RC}$ | | | ns |

## Data Retention Waveform




**Notes**
10. Tested initially and after any design or process changes that may affect these parameters.
11. Full device AC operation requires linear $V_{CC}$ ramp from $V_{DR}$ to $V_{CC(min)} \geq 100$ µs or stable at $V_{CC(min)} \geq 100$ µs.

## Switching Characteristics (Over the Operating Range) [12]

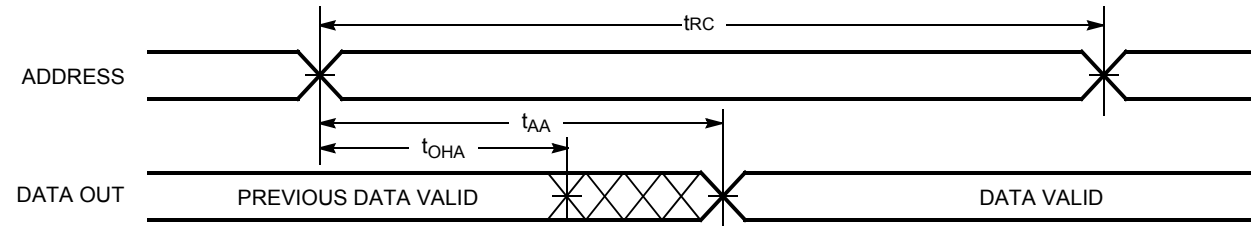
| Parameter | Description | 45 ns | | 55 ns [1] | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| **Read Cycle** | | | | | | |
| $t_{RC}$ | Read Cycle Time | 45 | | 55 | | ns |
| $t_{AA}$ | Address to Data Valid | | 45 | | 55 | ns |
| $t_{OHA}$ | Data Hold from Address Change | 10 | | 10 | | ns |
| $t_{ACE}$ | $\overline{CE}$ LOW to Data Valid | | 45 | | 55 | ns |
| $t_{DOE}$ | $\overline{OE}$ LOW to Data Valid | | 22 | | 25 | ns |
| $t_{LZOE}$ | $\overline{OE}$ LOW to Low Z [13] | 5 | | 5 | | ns |
| $t_{HZOE}$ | $\overline{OE}$ HIGH to High Z [13, 14] | | 18 | | 20 | ns |
| $t_{LZCE}$ | $\overline{CE}$ LOW to Low Z [13] | 10 | | 10 | | ns |
| $t_{HZCE}$ | $\overline{CE}$ HIGH to High Z [13, 14] | | 18 | | 20 | ns |
| $t_{PU}$ | $\overline{CE}$ LOW to Power Up | 0 | | 0 | | ns |
| $t_{PD}$ | $\overline{CE}$ HIGH to Power Up | | 45 | | 55 | ns |
| **Write Cycle** [15] | | | | | | |
| $t_{WC}$ | Write Cycle Time | 45 | | 55 | | ns |
| $t_{SCE}$ | $\overline{CE}$ LOW to Write End | 35 | | 40 | | ns |
| $t_{AW}$ | Address Setup to Write End | 35 | | 40 | | ns |
| $t_{HA}$ | Address Hold from Write End | 0 | | 0 | | ns |
| $t_{SA}$ | Address Setup to Write Start | 0 | | 0 | | ns |
| $t_{PWE}$ | $\overline{WE}$ Pulse Width | 35 | | 40 | | ns |
| $t_{SD}$ | Data Setup to Write End | 25 | | 25 | | ns |
| $t_{HD}$ | Data Hold from Write End | 0 | | 0 | | ns |
| $t_{HZWE}$ | $\overline{WE}$ LOW to High Z [13, 14] | | 18 | | 20 | ns |
| $t_{LZWE}$ | $\overline{WE}$ HIGH to Low Z [13] | 10 | | 10 | | ns |

**Notes**

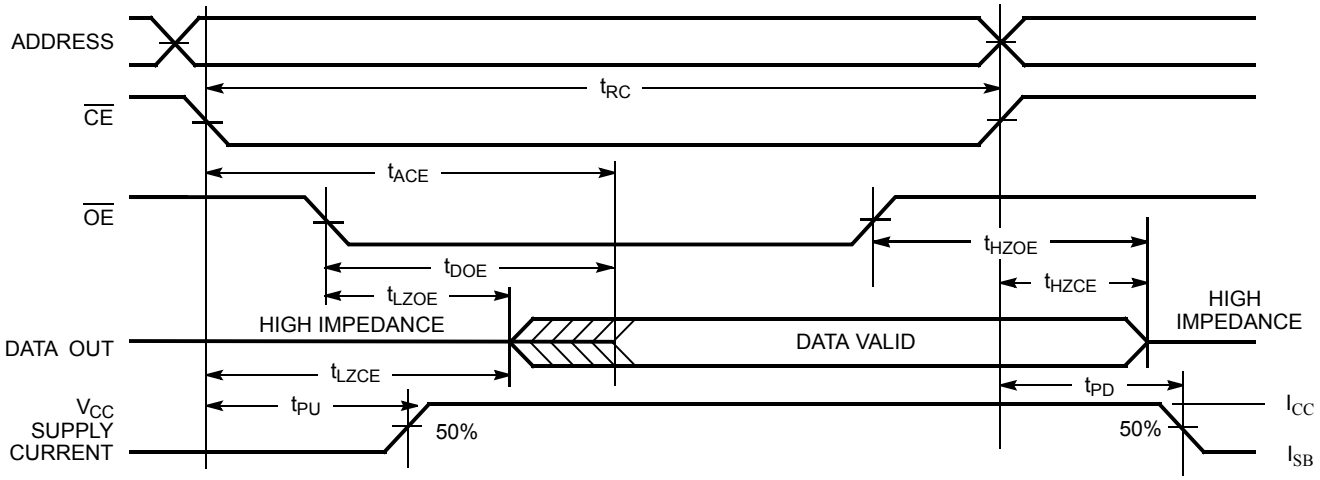
12. Test Conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less (1 V/ns), timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified $I_{OL}/I_{OH}$ as shown in the "AC Test Loads and Waveforms" on page 4.
13. At any given temperature and voltage condition, $t_{HZCE}$ is less than $t_{LZCE}$, $t_{HZOE}$ is less than $t_{LZOE}$, and $t_{HZWE}$ is less than $t_{LZWE}$ for any given device.
14. $t_{HZOE}$, $t_{HZCE}$, and $t_{HZWE}$ transitions are measured when the output enter a high impedance state.
15. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = $V_{IL}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.

## Switching Waveforms

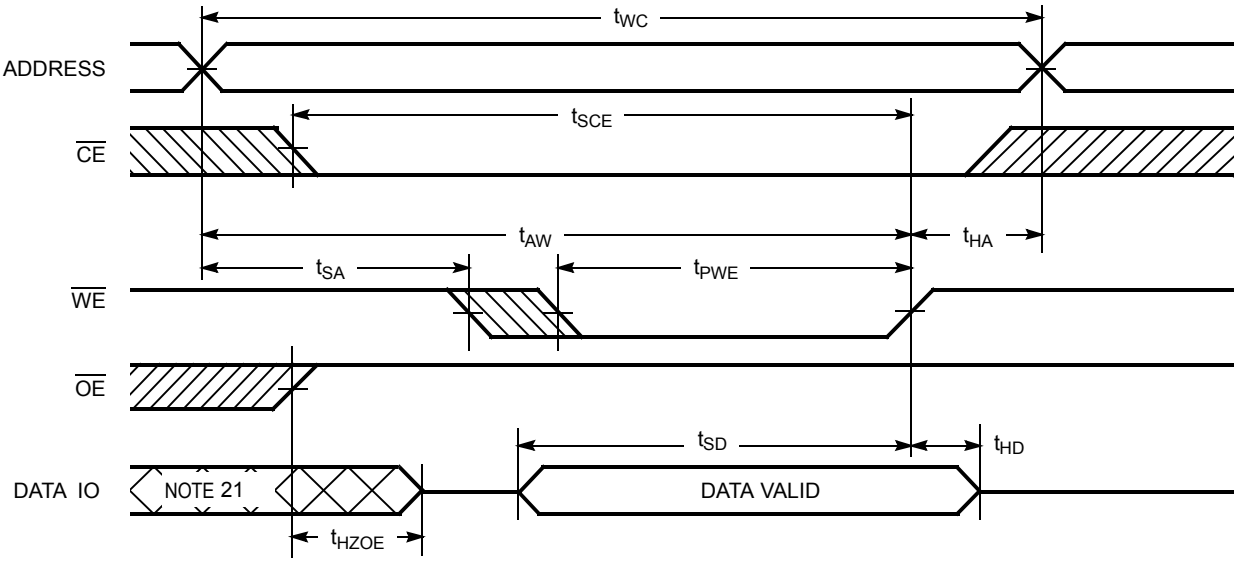
**Read Cycle No. 1** (Address Transition Controlled) [16, 17]




**Read Cycle No. 2** ($\overline{OE}$ Controlled) [17, 18]



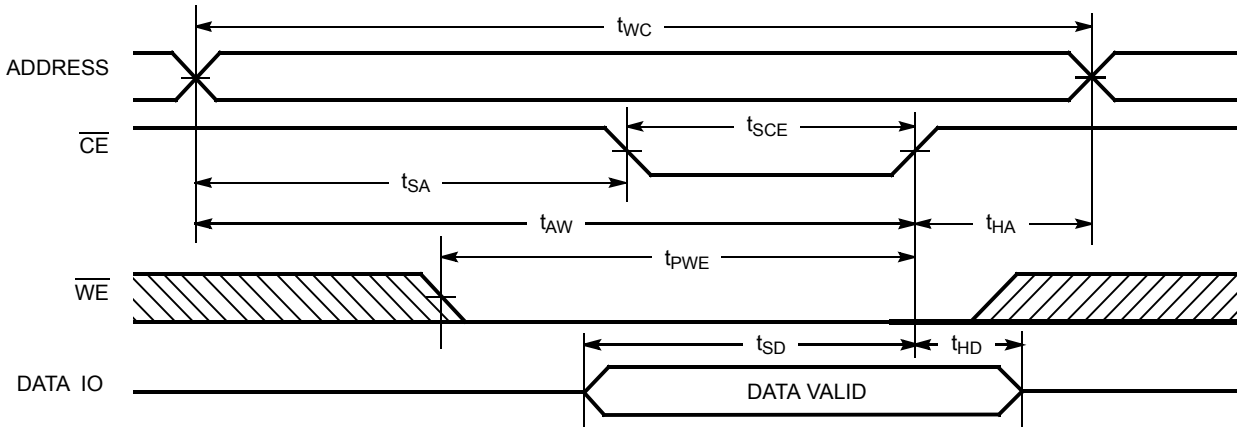

**Write Cycle No. 1** ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write) [19, 20]



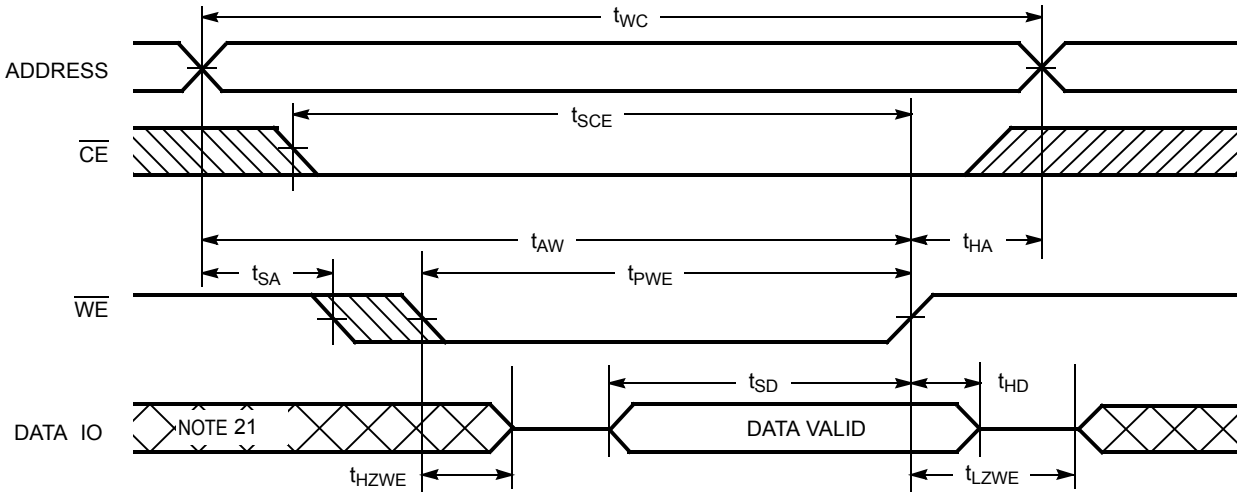

**Notes**
16. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = $V_{IL}$.
17. $\overline{WE}$ is HIGH for read cycles.
18. Address valid before or similar to $\overline{CE}$ transition LOW.
19. Data IO is high impedance if $\overline{OE}$ = $V_{IH}$.
20. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in high impedance state.
21. During this period, the IOs are in output state. Do not apply input signals.

## Switching Waveforms (continued)

**Write Cycle No. 2** ($\overline{CE}$ Controlled) [19, 20]




**Write Cycle No. 3** ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [20]




## Truth Table

| $\overline{CE}$ | $\overline{WE}$ | $\overline{OE}$ | Inputs/Outputs | Mode | Power |
|---|---|---|---|---|---|
| H | X | X | High Z | Deselect/Power down | Standby ($I_{SB}$) |
| L | H | L | Data Out | Read | Active ($I_{CC}$) |
| L | H | H | High Z | Output Disabled | Active ($I_{CC}$) |
| L | L | X | Data in | Write | Active ($I_{CC}$) |

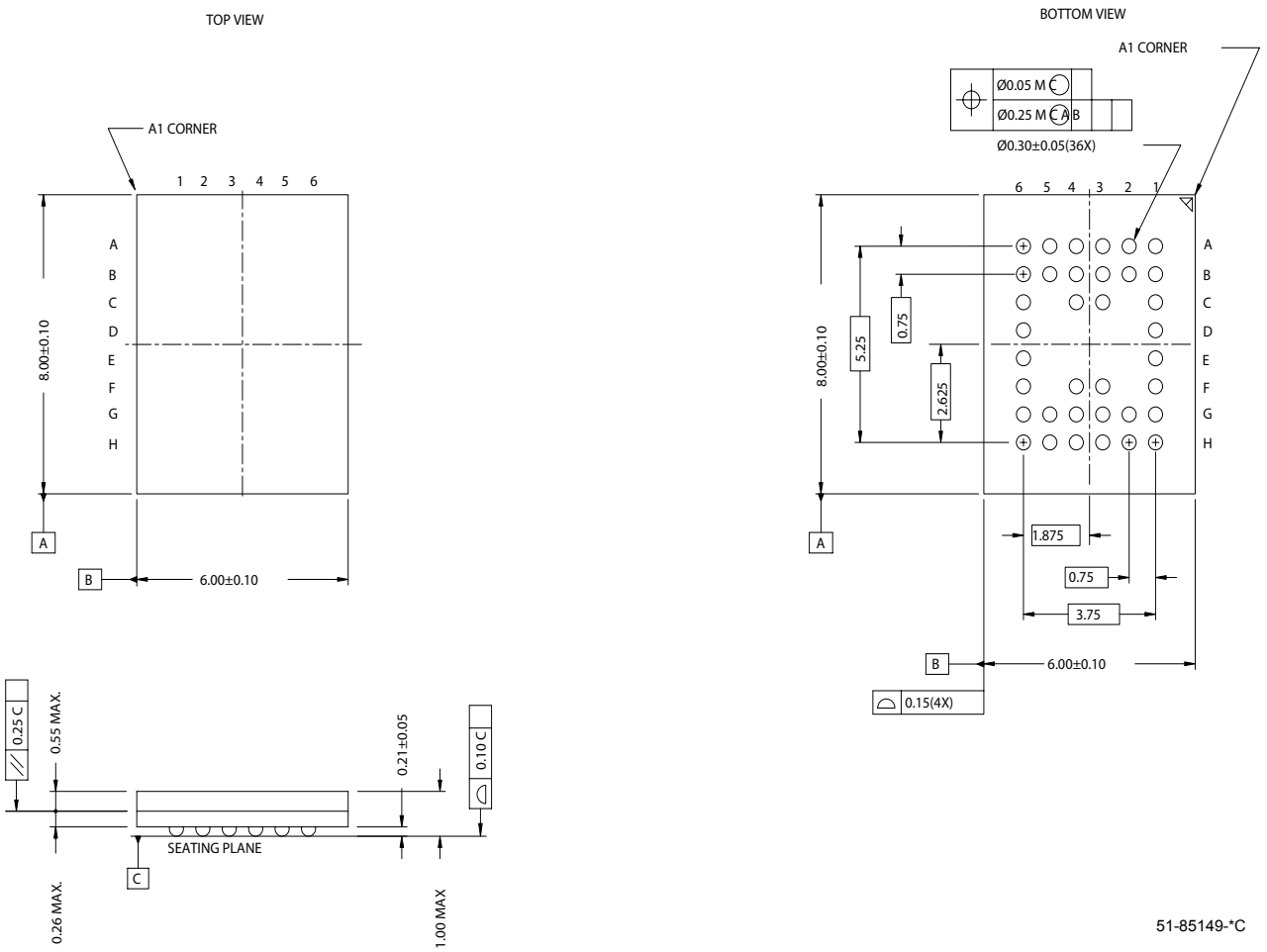
## Ordering Information

| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range |
|---|---|---|---|---|
| 45 | CY62148EV30LL-45BVXI | 51-85149 | 36-ball Very Fine Pitch Ball Grid Array (Pb-free) | Industrial |
| | CY62148EV30LL-45ZSXI | 51-85095 | 32-pin Thin Small Outline Package II (Pb-free) | |
| 55 | CY62148EV30LL-55SXI | 51-85081 | 32-pin Small Outline Integrated Circuit (Pb-free) | |

Contact your local Cypress sales representative for availability of these parts.

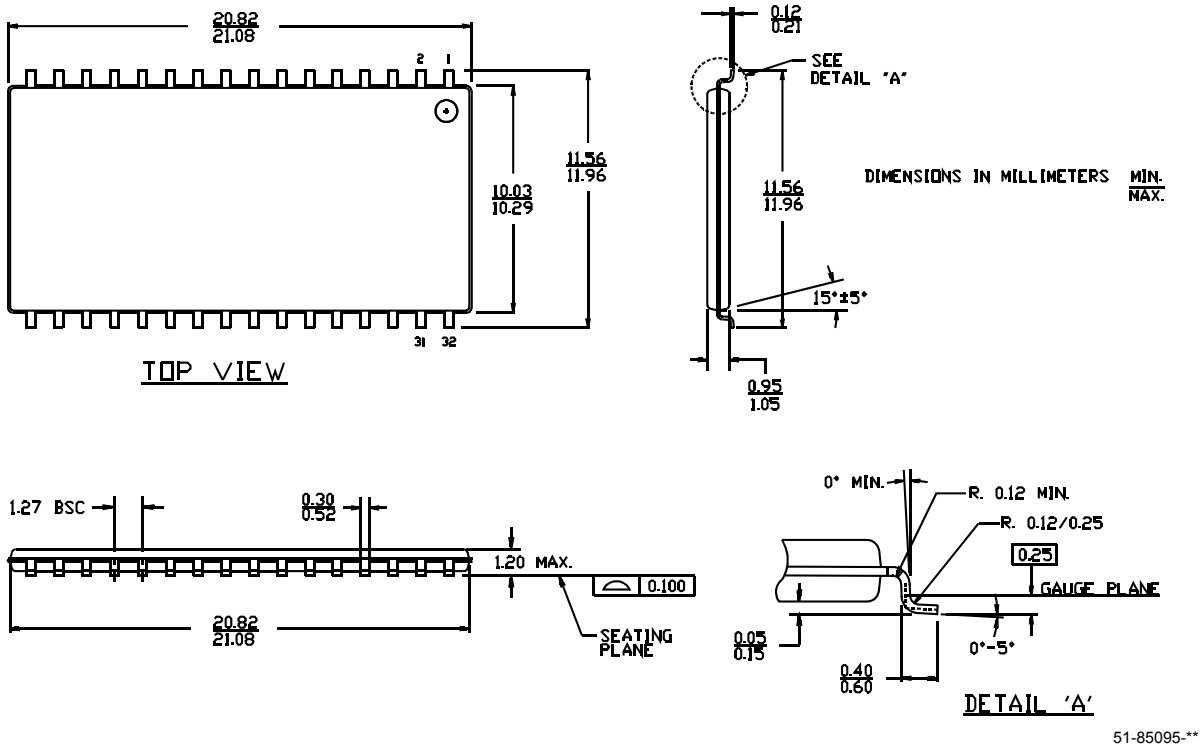
## Package Diagrams

**Figure 1. 36-ball VFBGA (6 x 8 x 1 mm), 51-85149**



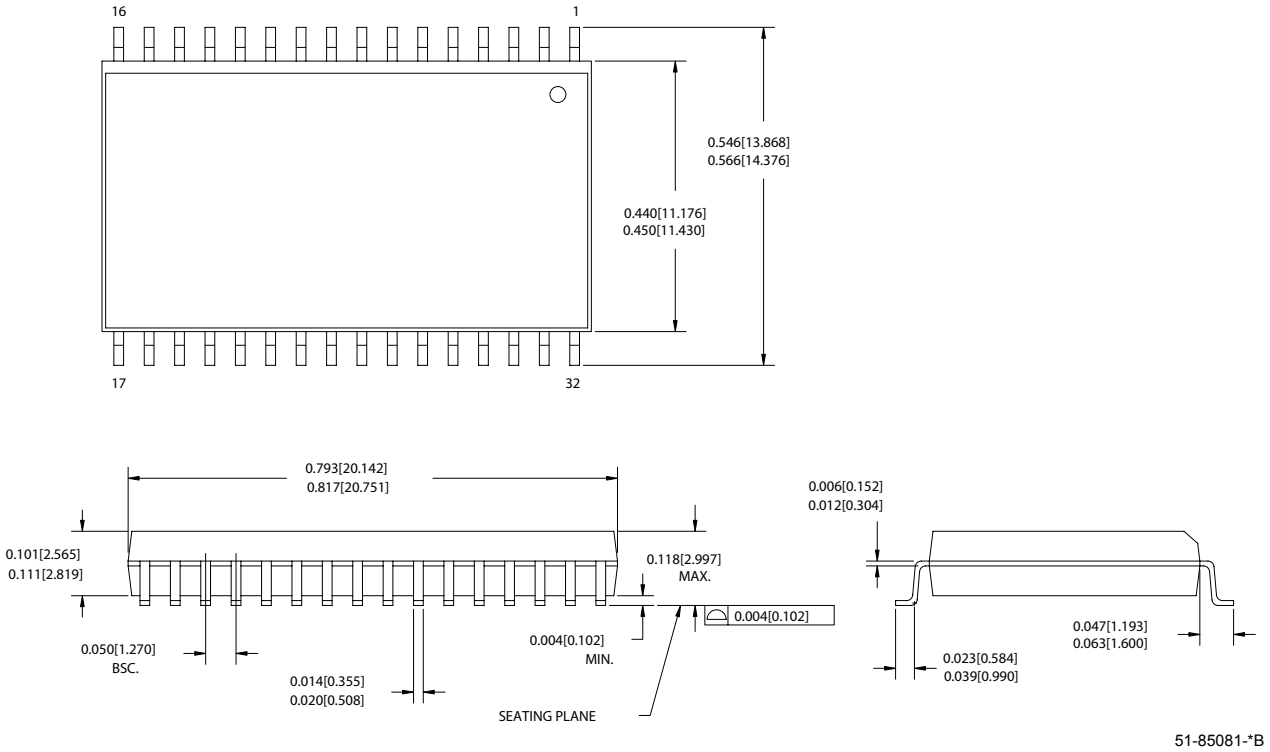
## Package Diagrams (continued)

**Figure 2. 32-pin TSOP II, 51-85095**



## Package Diagrams (continued)

**Figure 3. 32-pin (450 MIL) Molded SOIC, 51-85081**



## Document History Page

| Document Title: CY62148EV30 MoBL®, 4-Mbit (512K x 8) Static RAM<br>Document Number: 38-05576 | | | | |
|---|---|---|---|---|
| **REV.** | **ECN NO.** | **Issue Date** | **Orig. of Change** | **Description of Change** |
| ** | 223225 | See ECN | AJU | New data sheet |
| *A | 247373 | See ECN | SYT | Changed from Advance Information to Preliminary<br>Moved Product Portfolio to Page 2<br>Changed $V_{CC}$ stabilization time in footnote #7 from 100 μs to 200 μs<br>Changed $I_{CCDR}$ from 2.0 μA to 2.5 μA<br>Changed typo in Data Retention Characteristics ($t_R$) from 100 μs to $t_{RC}$ ns<br>Changed $t_{OHA}$ from 6 ns to 10 ns for both 35 ns and 45 ns Speed Bin<br>Changed $t_{HZOE}$, $t_{HZWE}$ from 12 to 15 ns for 35 ns Speed Bin and 15 to 18 ns for 45 ns Speed Bin<br>Changed $t_{SCE}$ from 25 to 30 ns for 35 ns Speed Bin and 40 to 35 ns for 45 ns Speed Bin<br>Changed $t_{HZCE}$ from 12 to 18 ns for 35 ns Speed Bin and 15 to 22 ns for 45 ns Speed Bin<br>Changed $t_{SD}$ from 15 to 18 ns for 35 ns Speed Bin and 20 to 22 ns for 45 ns Speed Bin<br>Changed $t_{DOE}$ from 15 to 18 ns for 35 ns Speed Bin<br>Changed Ordering Information to include Pb-Free Packages |
| *B | 414807 | See ECN | ZSD | Changed from Preliminary information to Final<br>Changed the address of Cypress Semiconductor Corporation on Page #1 from “3901 North First Street” to “198 Champion Court”<br>Removed 35ns Speed Bin<br>Removed “L” version of CY62148EV30<br>Changed ball C3 from DNU to NC.<br>Removed the redundant footnote on DNU.<br>Changed $I_{CC}$ (max) value from 2 mA to 2.5 mA and $I_{CC}$ (Typ) value from 1.5 mA to 2 mA at f=1 MHz<br>Changed $I_{CC}$ (Typ) value from 12 mA to 15 mA at f = $f_{max}$<br>Changed $I_{SB1}$ and $I_{SB2}$ Typ values from 0.7 μA to 1 μA and Max values from 2.5 μA to 7 μA.<br>Changed the AC test load capacitance value from 50pF to 30pF.<br>Changed $I_{CCDR}$ from 2.5 μA to 7 μA.<br>Added $I_{CCDR}$ typical value.<br>Changed $t_{LZOE}$ from 3 ns to 5 ns<br>Changed $t_{LZCE}$ and $t_{LZWE}$ from 6 ns to 10 ns<br>Changed $t_{HZCE}$ from 22 ns to 18 ns<br>Changed $t_{PWE}$ from 30 ns to 35 ns.<br>Changed $t_{SD}$ from 22 ns to 25 ns.<br>Updated the package diagram 36-pin VFBGA from *B to *C<br>Added 32-pin SOIC package diagram and pin diagram<br>Updated the ordering information table and replaced the Package Name column with Package Diagram. |
| *C | 464503 | See ECN | NXR | Included Automotive Range in product offering<br>Updated Thermal Resistance table<br>Updated the Ordering Information |
| *D | 833080 | See ECN | VKN | Added footnote #8<br>Added $V_{IL}$spec for SOIC package |
| *E | 890962 | See ECN | VKN | Removed Automotive part and its related information<br>Added footnote #2 related to SOIC package<br>Added footnote #9 related to $I_{SB2}$<br>Added AC values for 55 ns Industrial-SOIC range<br>Updated Ordering Information table |

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|---|---|---|---|---|
| **REV.** | **ECN NO.** | **Issue Date** | **Orig. of Change** | **Description of Change** |
| *F | 987940 | See ECN | VKN | Changed $V_{OL}$ spec from 0.4V to 0.2V for SOIC package at $I_{OL}$ = 0.1 mA<br>Changed $V_{IL}$ spec from 0.6V to 0.4V for SOIC package at $V_{CC}$ = 2.2V to 2.7V<br>Updated footnote #8<br>Made footnote #9 applicable for both $I_{SB2}$ and $I_{CCDR}$ |