

ASSP

Dual Serial Input PLL Frequency Synthesizer

MB15F74UV

DESCRIPTION

The Fujitsu MB15F74UV is a serial input Phase Locked Loop (PLL) frequency synthesizer with a 4000 MHz and a 2000 MHz prescalers. A 64/65 or a 128/129 for the 4000 MHz prescaler, and a 32/33 or a 64/65 for the 2000 MHz prescaler can be selected for the prescaler that enables pulse swallow operation.

The BiCMOS process is used, as a result a supply current is typically 9.0 mA at 3.0 V. The supply voltage range is from 2.7 V to 3.6 V. A refined charge pump supplies well-balanced output current with 1.5 mA and 6 mA selectable by serial date. The serial data format is the same as MB15F74UL. Fast locking is achieved for adopting the new circuit.

MB15F74UV is in the small package (BCC18) which decreases a mount area of MB15F74UV about 50% comparing with the former BCC20 (for dual PLL) .

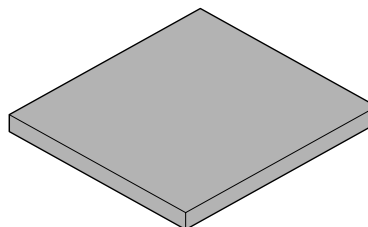
FEATURES

- High frequency operation : RF synthesizer : 4000 MHz Max
: IF synthesizer : 2000 MHz Max
- Low power supply voltage : $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$
- Ultra low power supply current : $I_{CC} = 9.0 \text{ mA Typ}$
($V_{CC} = 3.0 \text{ V}$, $T_a = +25 \text{ }^\circ\text{C}$, $SW_{IF} = SW_{RF} = 0$ in IF/RF locking state)

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PACKAGE

18-pin plastic BCC



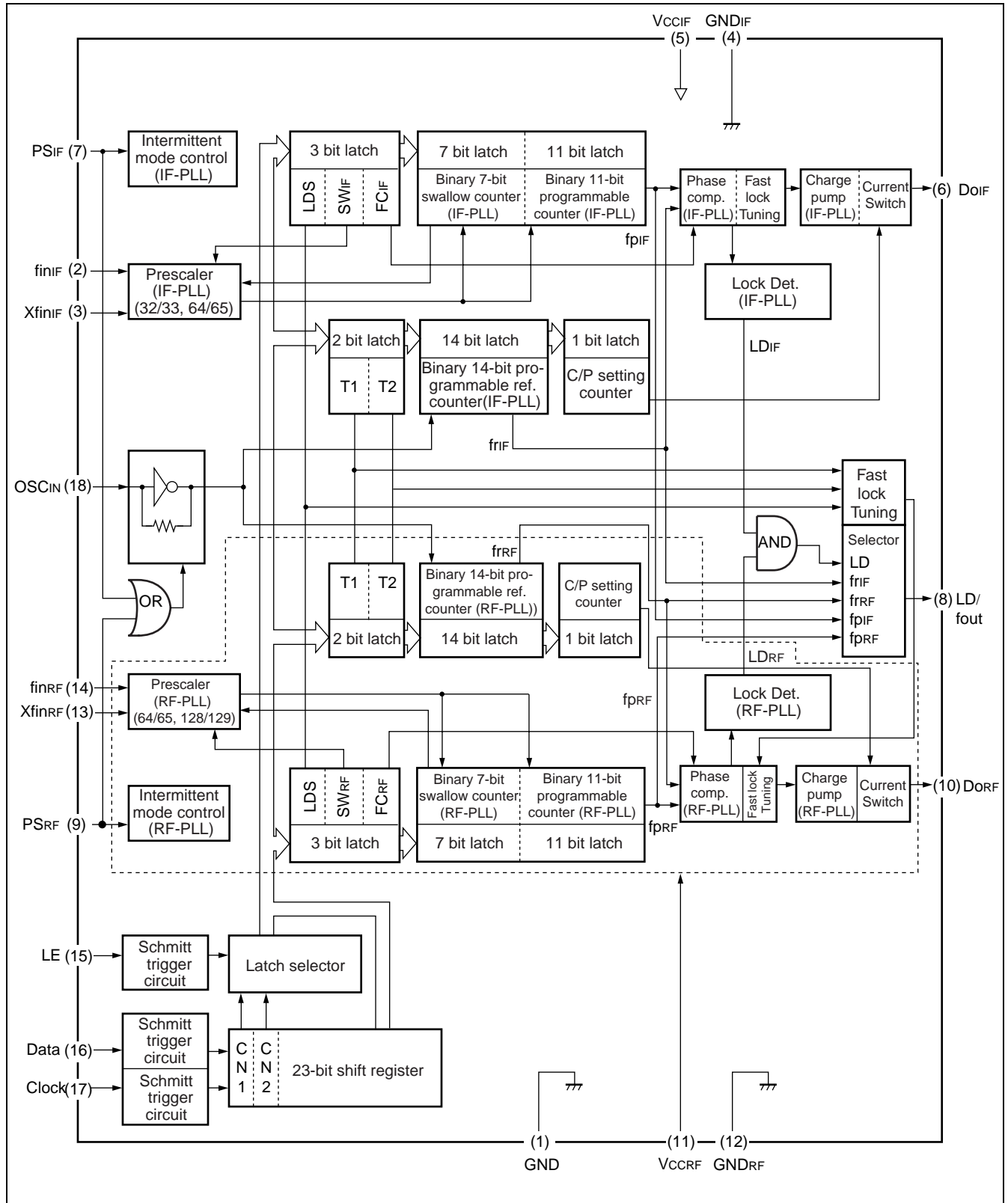
(LCC-18P-M05)

■ PIN DESCRIPTION

Pin no.	Pin name	I/O	Descriptions
1	GND	—	Ground pin for OSC input buffer and the shift register circuit.
2	fin _{IF}	I	Prescaler input pin for the IF-PLL. Connection to an external VCO should be AC coupling.
3	Xfin _{IF}	I	Prescaler complimentary input for the IF-PLL section. This pin should be grounded via a capacitor.
4	GND _{IF}	—	Ground pin for the IF-PLL section.
5	V _{CCIF}	—	Power supply voltage input pin for the IF-PLL section, the shift register and the oscillator input buffer.
6	Do _{IF}	O	Charge pump output for the IF-PLL section.
7	PS _{IF}	I	Power saving mode control pin for the IF-PLL section. This pin must be set at “L” when the power supply is started up. (Open is prohibited.) PS _{IF} = “H” ; Normal mode/PS _{IF} = “L” ; Power saving mode
8	LD/fout	O	Lock detect signal output (LD) /phase comparator monitoring output (fout) pin. The output signal is selected by LDS bit in a serial data. LDS bit = “H” ; outputs fout signal/LDS bit = “L” ; outputs LD signal
9	PS _{RF}	I	Power saving mode control for the RF-PLL section. This pin must be set at “L” when the power supply is started up. (Open is prohibited.) PS _{RF} = “H” ; Normal mode/PS _{RF} = “L” ; Power saving mode
10	Do _{RF}	O	Charge pump output for the RF-PLL section.
11	V _{CCRF}	—	Power supply voltage input pin for the RF-PLL section.
12	GND _{RF}	—	Ground pin for the RF-PLL section
13	Xfin _{RF}	I	Prescaler complimentary input pin for the RF-PLL section. This pin should be grounded via a capacitor.
14	fin _{RF}	I	Prescaler input pin for the RF-PLL. Connection to an external VCO should be via AC coupling.
15	LE	I	Load enable signal input pin (with the schmitt trigger circuit) When LE is set “H”, data in the shift register is transferred to the corresponding latch according to the control bit in a serial data.
16	Data	I	Serial data input pin (with the schmitt trigger circuit) Data is transferred to the corresponding latch (IF-ref. counter, IF-prog. counter, RF-ref. counter, RF-prog. counter) according to the control bit in a serial data.
17	Clock	I	Clock input pin for the 23-bit shift register (with the schmitt trigger circuit) One bit data is shifted into the shift register on a rising edge of the clock.
18	OSC _{IN}	I	The programmable reference divider input pin. TCXO should be connected with an AC coupling capacitor.

MB15F74UV

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Power supply voltage	V_{CC}	-0.5	4.0	V
Input voltage	V_I	-0.5	$V_{CC} + 0.5$	V
Output voltage	LD/fout	GND	V_{CC}	V
	DOIF, DORF	GND	V_{CC}	V
Storage temperature	Tstg	-55	+125	°C

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}	2.7	3.0	3.6	V	$V_{CCRF} = V_{CCIF}$
Input voltage	V_I	GND	—	V_{CC}	V	
Operating temperature	T_a	-40	—	+85	°C	

Note : • V_{CCRF} and V_{CCIF} must supply equal voltage.

Even if either RF-PLL or IF-PLL is not used, power must be supplied to V_{CCRF} and V_{CCIF} to keep them equal.

It is recommended that the non-use PLL is controlled by power saving function.

- Although this device contains an anti-static element to prevent electrostatic breakdown and the circuitry has been improved in electrostatic protection, observe the following precautions when handling the device.
 - When storing and transporting the device, put it in a conductive case.
 - Before handling the device, confirm the (jigs and) tools to be used have been uncharged (grounded) as well as yourself. Use a conductive sheet on working bench.
 - Before fitting the device into or removing it from the socket, turn the power supply off.
 - When handling (such as transporting) the device mounted board, protect the leads with a conductive sheet.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

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ELECTRICAL CHARACTERISTICS

($V_{CC} = 2.7\text{ V to }3.6\text{ V}$, $T_a = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$)

Parameter	Symbol	Condition	Value			Unit		
			Min	Typ	Max			
Power supply current	I_{CCIF}^{*1}	$f_{inIF} = 2000\text{ MHz}$ $V_{CCIF} = 3.0\text{ V}$	2.1	2.5	3.2	mA		
	I_{CCRF}^{*1}	$f_{inRF} = 2500\text{ MHz}$ $V_{CCRF} = 3.0\text{ V}$	5.7	6.5	8.4	mA		
Power saving current	I_{PSIF}	$PS_{IF} = PS_{RF} = \text{"L"}$	—	0.1^{*2}	10	μA		
	I_{PSRF}	$PS_{IF} = PS_{RF} = \text{"L"}$	—	0.1^{*2}	10	μA		
Operating frequency	f_{inIF}^{*3}	f_{inIF}	IF PLL	200	—	2000	MHz	
	f_{inRF}^{*3}	f_{inRF}	RF PLL	2000	—	4000	MHz	
	OSC_{IN}	f_{OSC}	—	3	—	40	MHz	
Input sensitivity	f_{inIF}	P_{finIF}	IF PLL, $50\ \Omega$ system	-15	—	+2	dBm	
	f_{inRF}	P_{finRF}	RF PLL, $50\ \Omega$ system	-10	—	+2	dBm	
Input available voltage	OSC_{IN}	V_{OSC}	—	0.5	1.0	1.5	V_{P-P}	
"H" level input voltage	Data LE	V_{IH}	Schmitt trigger input	$0.7 V_{CC} + 0.4$	—	—	V	
"L" level input voltage	Clock	V_{IL}	Schmitt trigger input	—	—	$0.3 V_{CC} - 0.4$	V	
"H" level input voltage	PS_{IF}	V_{IH}	—	$0.7 V_{CC}$	—	—	V	
"L" level input voltage	PS_{RF}	V_{IL}	—	—	—	$0.3 V_{CC}$	V	
"H" level input current	Data LE	I_{IH}^{*4}	—	-1.0	—	+1.0	μA	
"L" level input current	Clock PS	I_{IL}^{*4}	—	-1.0	—	+1.0	μA	
"H" level output voltage	LD/ f_{out}	V_{OH}	$V_{CC} = 3.0\text{ V}$, $I_{OH} = -1\text{ mA}$	$V_{CC} - 0.4$	—	—	V	
"L" level output voltage		V_{OL}	$V_{CC} = 3.0\text{ V}$, $I_{OL} = 1\text{ mA}$	—	—	0.4	V	
"H" level output voltage	DO_{IF}	V_{DOH}	$V_{CC} = 3.0\text{ V}$, $I_{DOH} = -0.5\text{ mA}$	$V_{CC} - 0.4$	—	—	V	
"L" level output voltage	$DORF$	V_{DOL}	$V_{CC} = 3.0\text{ V}$, $I_{DOL} = 0.5\text{ mA}$	—	—	0.4	V	
High impedance cutoff current	DO_{IF} $DORF$	I_{OFF}	$V_{CC} = 3.0\text{ V}$ $V_{OFF} = 0.5\text{ V to }V_{CC} - 0.5\text{ V}$	—	—	2.5	nA	
"H" level output current	LD/ f_{out}	I_{OH}^{*4}	$V_{CC} = 3.0\text{ V}$	—	—	-1.0	mA	
"L" level output current		I_{OL}	$V_{CC} = 3.0\text{ V}$	1.0	—	—	mA	
"H" level output current	DO_{IF}^{*8} $DORF$	I_{DOH}^{*4}	$V_{CC} = 3.0\text{ V}$, $V_{DOH} = V_{CC} / 2$, $T_a = +25\text{ }^\circ\text{C}$	CS bit = "1"	-8.2	-6.0	-4.1	mA
				CS bit = "0"	-2.2	-1.5	-0.8	mA
"L" level output current	DO_{IF}^{*8} $DORF$	I_{DOL}	$V_{CC} = 3.0\text{ V}$, $V_{DOL} = V_{CC} / 2$, $T_a = +25\text{ }^\circ\text{C}$	CS bit = "1"	4.1	6.0	8.2	mA
				CS bit = "0"	0.8	1.5	2.2	mA

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($V_{CC} = 2.7\text{ V to }3.6\text{ V}$, $T_a = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$)

Parameter	Symbol	Condition	Value			Unit	
			Min	Typ	Max		
Charge pump current rate	I_{DOL}/I_{DOH}	I_{DOMT}^{*5}	$V_{DO} = V_{CC} / 2$	—	3	10	%
	vs V_{DO}	I_{DOVD}^{*6}	$0.5\text{ V} \leq V_{DO} \leq V_{CC} - 0.5\text{ V}$	—	10	15	%
	vs T_a	I_{DOTA}^{*7}	$-40\text{ }^\circ\text{C} \leq T_a \leq 85\text{ }^\circ\text{C}$, $V_{DO} = V_{CC} / 2$	—	5	10	%

*1 : Conditions ; $f_{osc} = 12.8\text{ MHz}$, $T_a = +25\text{ }^\circ\text{C}$, $SW = "0"$ in locking state.

*2 : $V_{CCIF} = V_{CCRF} = 3.0\text{ V}$, $f_{osc} = 12.8\text{ MHz}$, $T_a = +25\text{ }^\circ\text{C}$, in power saving mode.

$PS_{IF} = PS_{RF} = GND$

$V_{IH} = V_{CC}$, $V_{IL} = GND$ (at CLK, Data, LE)

*3 : AC coupling. 1000 pF capacitor is connected under the condition of Min operating frequency.

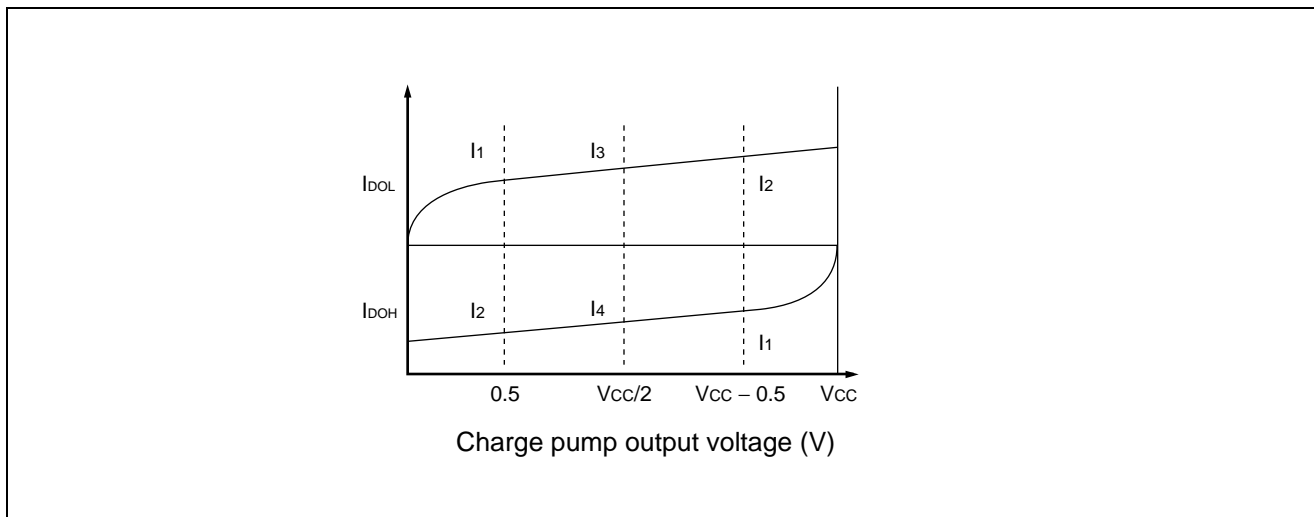
*4 : The symbol “-” (minus) means the direction of current flow.

*5 : $V_{CC} = 3.0\text{ V}$, $T_a = +25\text{ }^\circ\text{C}$ $(|I_3| - |I_4|) / [(|I_3| + |I_4|) / 2] \times 100\text{ }(\%)$

*6 : $V_{CC} = 3.0\text{ V}$, $T_a = +25\text{ }^\circ\text{C}$ $[(|I_2| - |I_1|) / 2] / [(|I_1| + |I_2|) / 2] \times 100\text{ }(\%)$ (Applied to both I_{DOL} and I_{DOH})

*7 : $V_{CC} = 3.0\text{ V}$, $[(|I_{DO(+85\text{ }^\circ\text{C})}| - |I_{DO(-40\text{ }^\circ\text{C})}|) / 2] / [(|I_{DO(+85\text{ }^\circ\text{C})}| + |I_{DO(-40\text{ }^\circ\text{C})}|) / 2] \times 100\text{ }(\%)$ (Applied to both I_{DOL} and I_{DOH})

*8 : When Charge pump current is measured, set $LDS = "0"$, $T1 = "0"$ and $T2 = "1"$.



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FUNCTIONAL DESCRIPTION

1. Pulse swallow function

$$f_{VCO} = [(P \times N) + A] \times f_{osc} \div R$$

f_{VCO} : Output frequency of external voltage controlled oscillator (VCO)

P : Preset divide ratio of dual modulus prescaler (32 or 64 for IF-PLL, 64 or 128 for RF-PLL)

N : Preset divide ratio of binary 11-bit programmable counter (3 to 2,047)

A : Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$, $A < N$)

f_{osc} : Reference oscillation frequency (OSC_{IN} input frequency)

R : Preset divide ratio of binary 14-bit programmable reference counter (3 to 16,383)

2. Serial Data Input

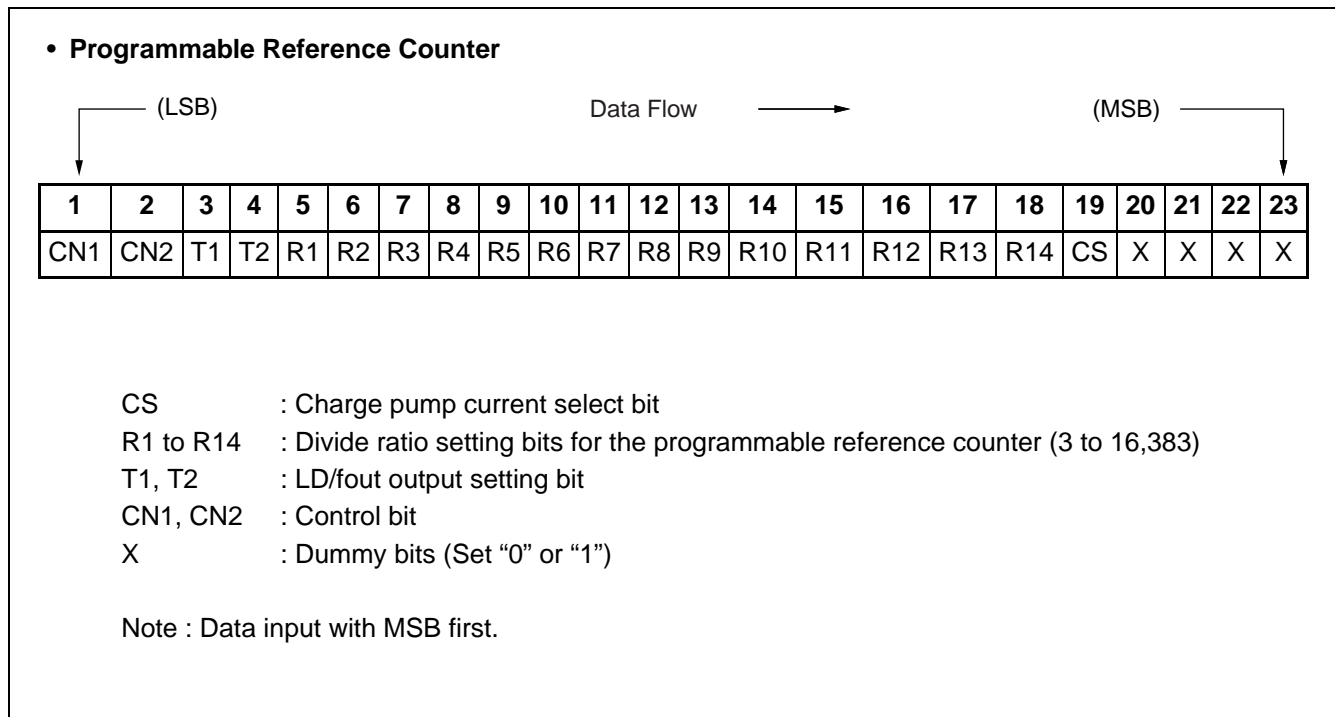
The serial data is entered using three pins, Data pin, Clock pin, and LE pin. Programmable dividers of IF/RF-PLL sections, programmable reference dividers of IF/RF-PLL sections are controlled individually.

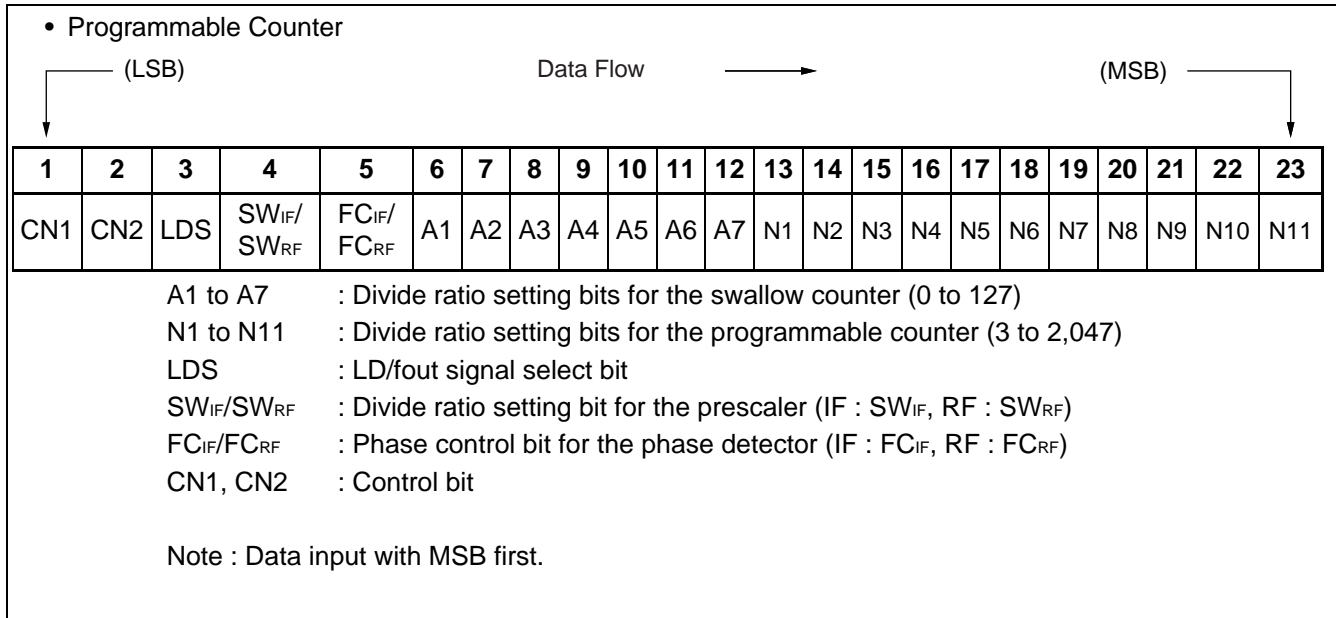
The serial data of binary data is entered through Data pin.

On rising edge of Clock, one bit of the serial data is transferred into the shift register. On a rising edge of load enable signal, the data stored in the shift register is transferred to one of latches depending upon the control bit data setting.

	The programmable reference counter for the IF-PLL	The programmable reference counter for the RF-PLL	The programmable counter and the swallow counter for the IF-PLL	The programmable counter and the swallow counter for the RF-PLL
CN1	0	1	0	1
CN2	0	0	1	1

(1) Shift Register Configuration





(2) Data setting

• Binary 14-bit Programmable Reference Counter Data Setting

Divide ratio	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1
3	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note : Divide ratio less than 3 is prohibited.

• Binary 11-bit Programmable Counter Data Setting

Divide ratio	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1
3	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

Note : Divide ratio less than 3 is prohibited

• Binary 7-bit Swallow Counter Data Setting

Divide ratio	A7	A6	A5	A4	A3	A2	A1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

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- Prescaler Data Setting

Divide ratio	SW = "1"	SW = "0"
Prescaler divide ratio IF-PLL	32/33	64/65
Prescaler divide ratio RF-PLL	64/65	128/129

- Charge Pump Current Setting

Current value	CS
±6.0 mA	1
±1.5 mA	0

- LD/fout output Selectable Bit Setting

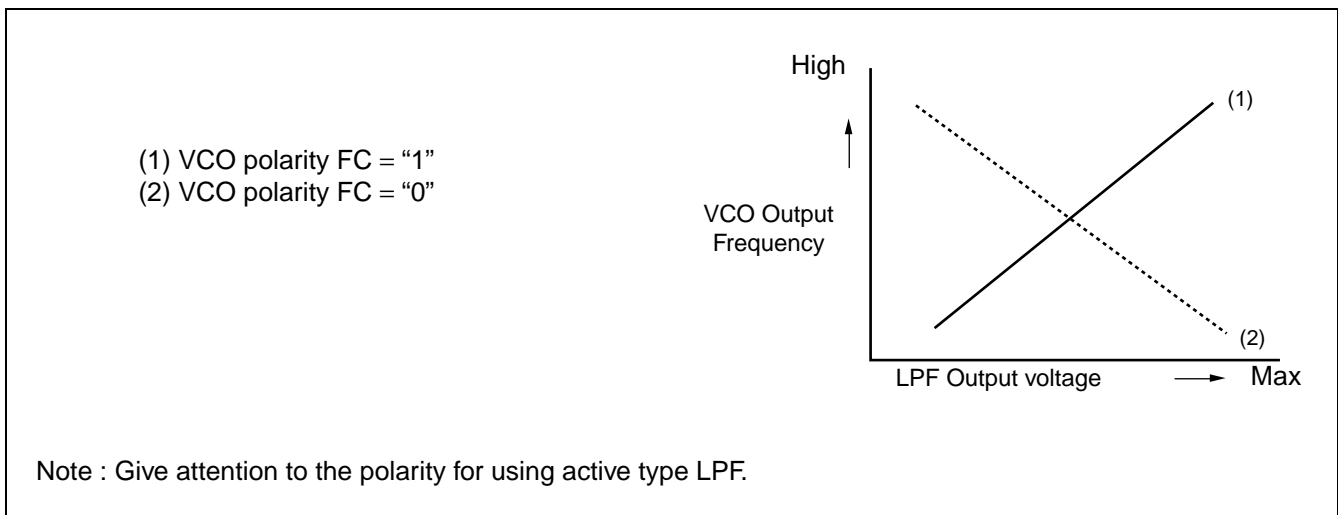
LD/fout pin state		LDS	T1	T2
LD output		0	0	0
		0	1	0
		0	1	1
fout output	frIF	1	0	0
	frRF	1	1	0
	fpIF	1	0	1
	fpRF	1	1	1

- Phase Comparator Phase Switching Data Setting

Phase comparator input	FC _{IF, RF} = "1"	FC _{IF, RF} = "0"
	Do _{IF, RF}	Do _{IF, RF}
fr > fp	H	L
fr < fp	L	H
fr = fp	Z	Z

Z : High-impedance

Depending upon the VCO and LPF polarity, FC bit should be set.



3. Power Saving Mode (Intermittent Mode Control Circuit)

Status	PS pin
Normal mode	H
Power saving mode	L

The intermittent mode control circuit reduces the PLL power consumption.

By setting the PS pin low, the device enters into the power saving mode, reducing the current consumption. See the Electrical Characteristics chart for the specific value.

The phase detector output, Do, becomes high impedance.

For the dual PLL, the lock detector, LD, is as shown in the LD Output Logic table.

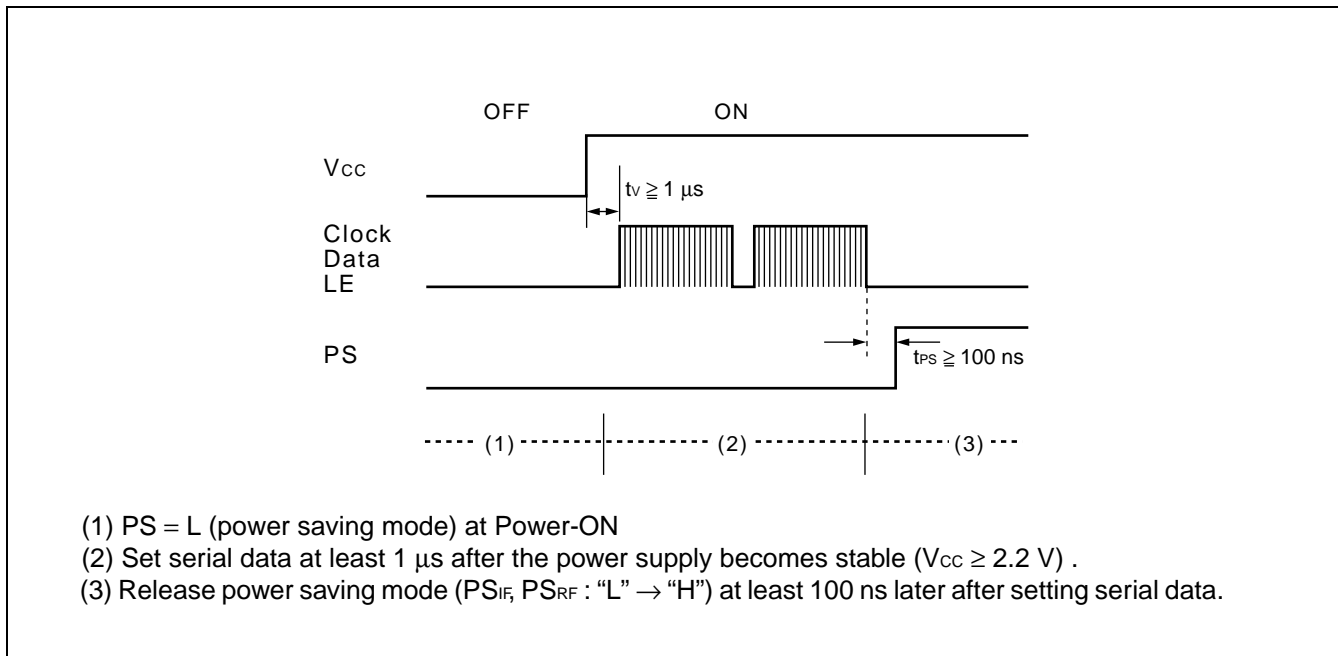
Setting the PS pin high, releases the power saving mode, and the device works normally.

The intermittent mode control circuit also ensures a smooth startup when the device returns to normal operation. When the PLL is returned to normal operation, the phase comparator output signal is unpredictable. This is because of the unknown relationship between the comparison frequency (f_p) and the reference frequency (f_r) which can cause a major change in the comparaoor output, resulting in a VCO frequency jump and an increase in lockup time.

To prevent a major VCO frequency jump, the intermittent mode control circuit limits the magnitude of the error signal from the phase detector when it returns to normal operation.

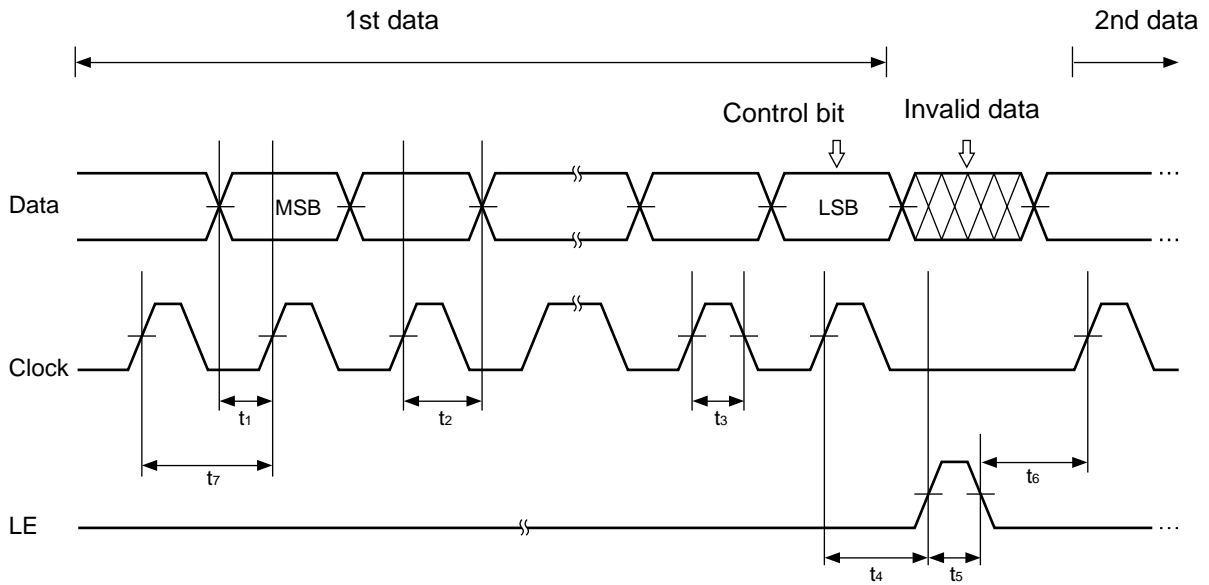
Notes : • When power (VCC) is first applied, the device must be in standby mode.

- PS pin must be set "L" at Power-ON.



4. Serial Data Data Input Timing

Divide ratio is performed through a serial interface using the Data pin, Clock pin, and LE pin. Setting data is read into the shift register at the rise of the Clock signal, and transferred to a latch at the rise of the LE signal. The following diagram shows the data input timing.

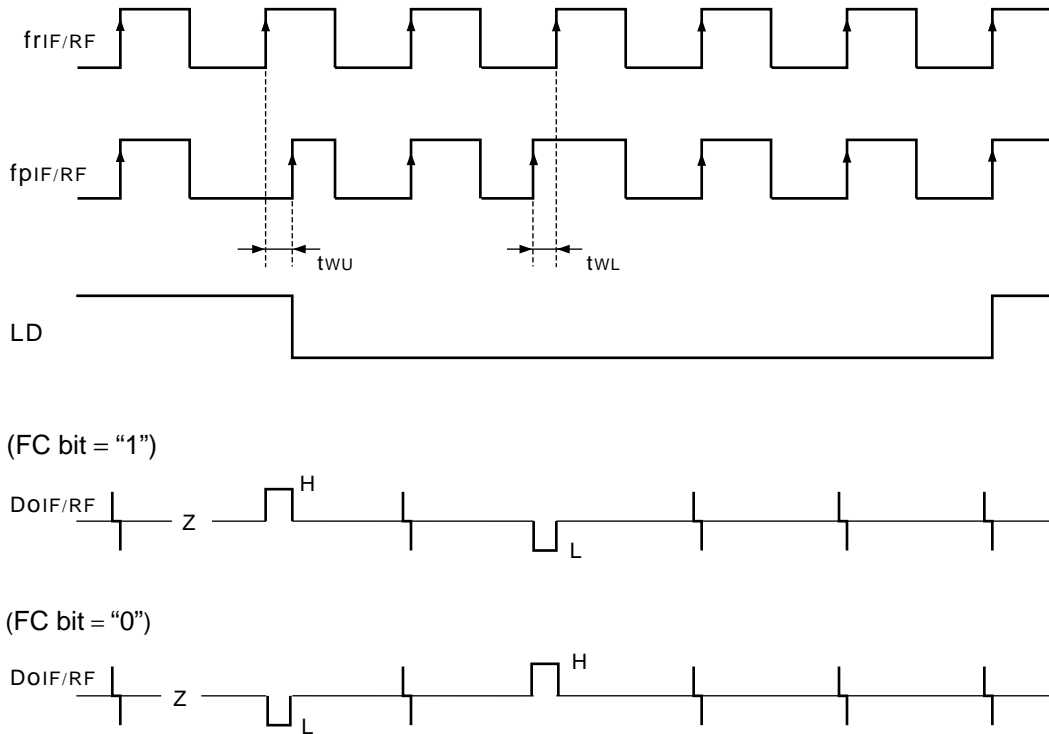


Parameter	Min	Typ	Max	Unit
t_1	20	—	—	ns
t_2	20	—	—	ns
t_3	30	—	—	ns
t_4	30	—	—	ns

Parameter	Min	Typ	Max	Unit
t_5	100	—	—	ns
t_6	20	—	—	ns
t_7	100	—	—	ns

Note : LE should be "L" when the data is transferred into the shift register.

■ PHASE COMPARATOR OUTPUT WAVEFORM



• LD Output Logic

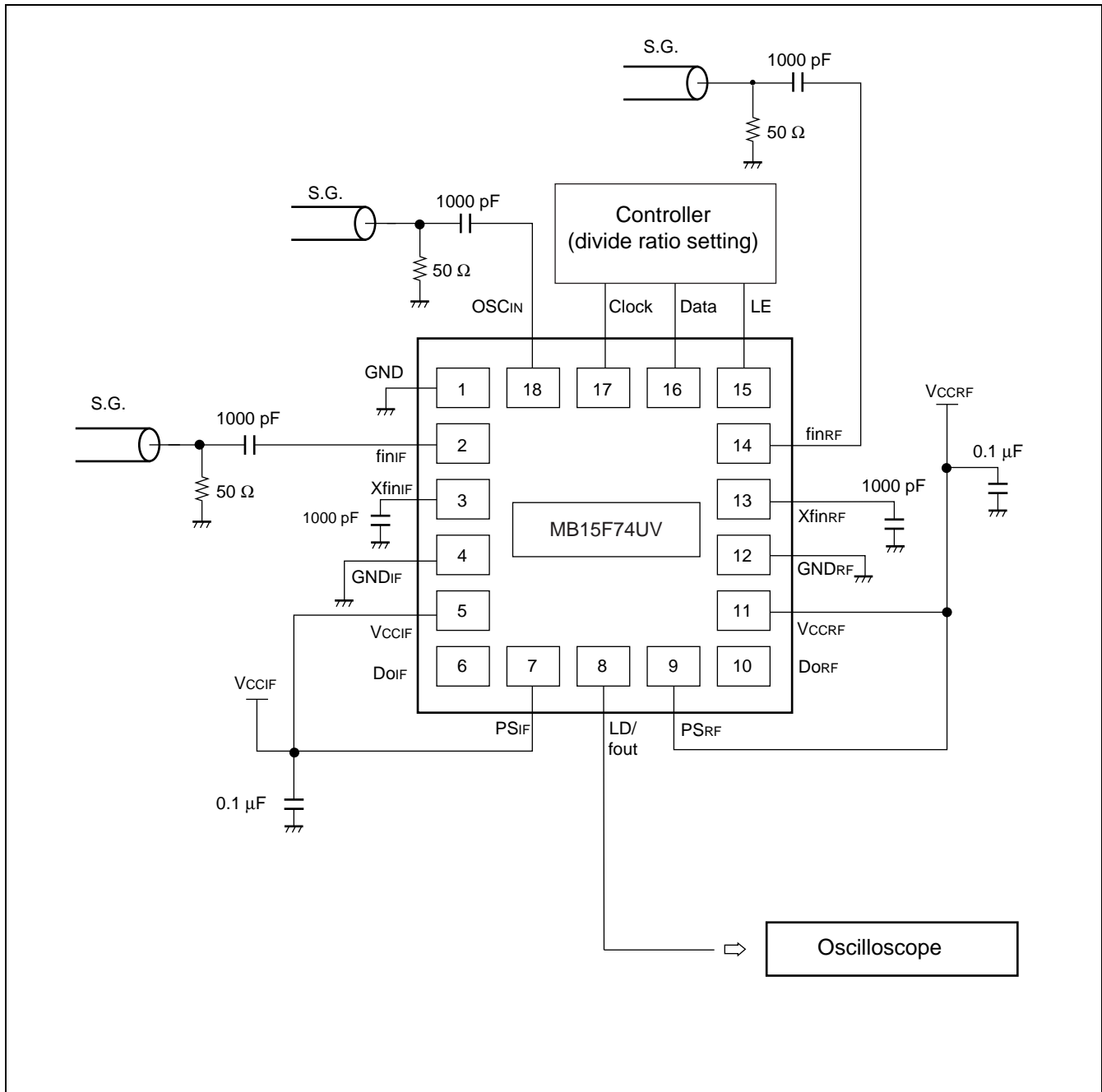
IF-PLL section	RF-PLL section	LD output
Locking state/Power saving state	Locking state/Power saving state	H
Locking state/Power saving state	Unlocking state	L
Unlocking state	Locking state/Power saving state	L
Unlocking state	Unlocking state	L

Notes : • Phase error detection range = -2π to $+2\pi$

- Pulses on DoIF/RF signals during locking state are output to prevent dead zone.
- LD output becomes low when phase error is t_{WU} or more.
- LD output becomes high when phase error is t_{WL} or less and continues to be so for three cycles or more.
- t_{WU} and t_{WL} depend on OSC_{IN} input frequency as follows.
 - $t_{WU} \geq 2/f_{osc}$: e.g. $t_{WU} \geq 156.3$ ns when $f_{osc} = 12.8$ MHz
 - $t_{WU} \leq 4/f_{osc}$: e.g. $t_{WU} \leq 312.5$ ns when $f_{osc} = 12.8$ MHz

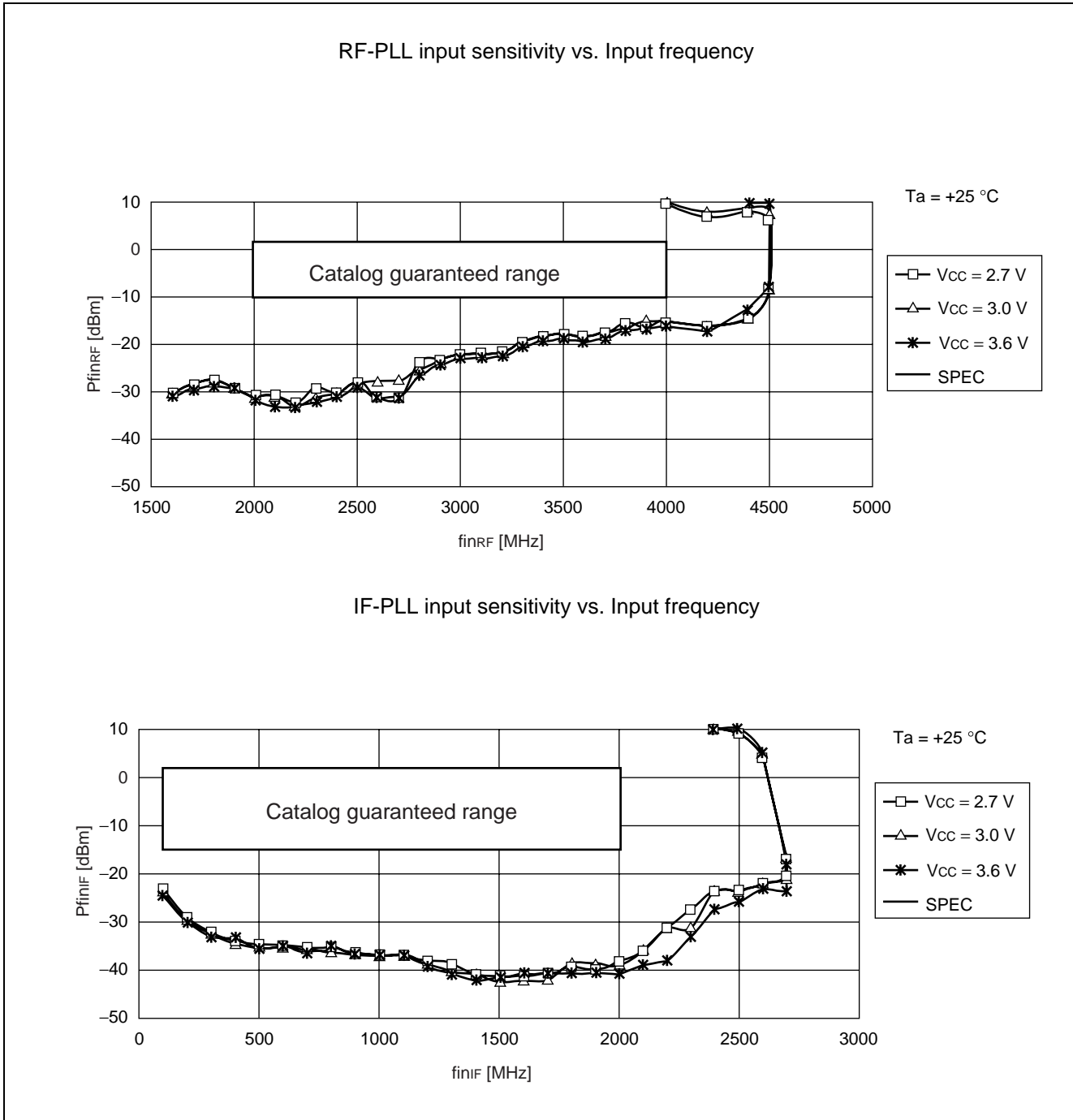
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TEST CIRCUIT (for Measuring Input Sensitivity f_{in}/OSC_{IN})



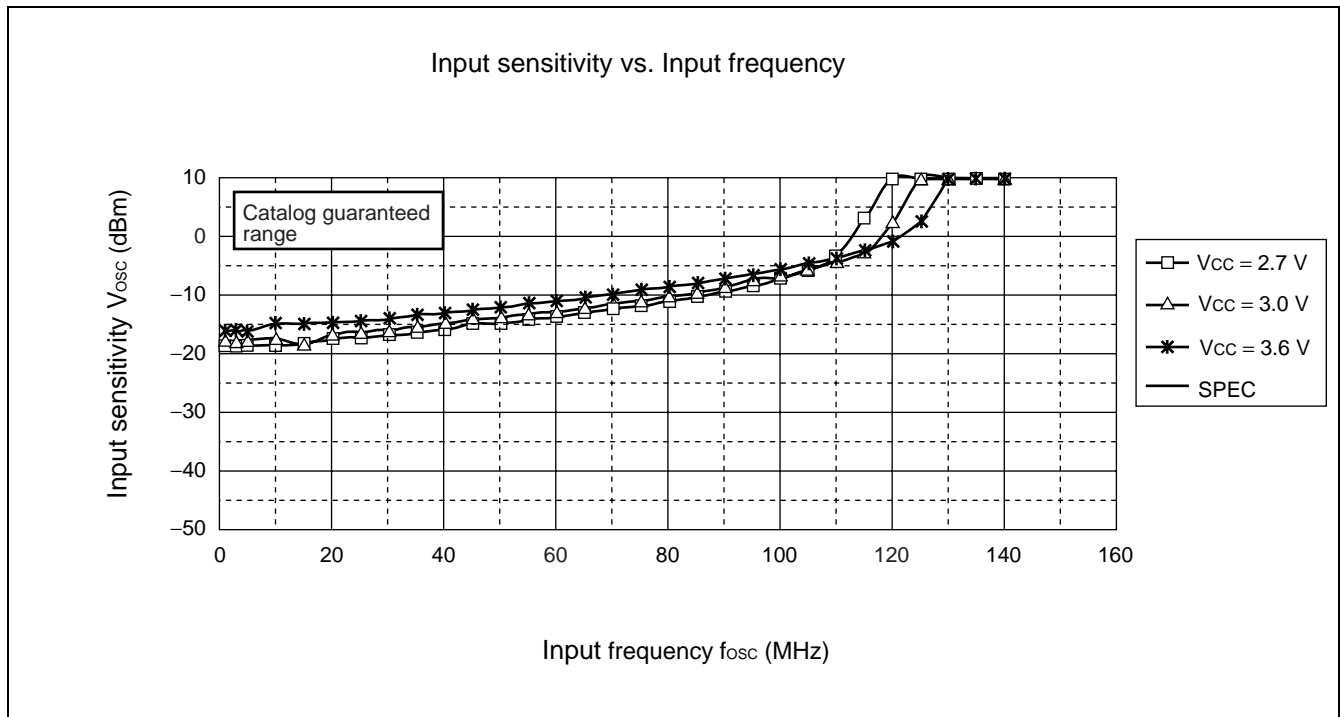
TYPICAL CHARACTERISTICS

1. fin input sensitivity



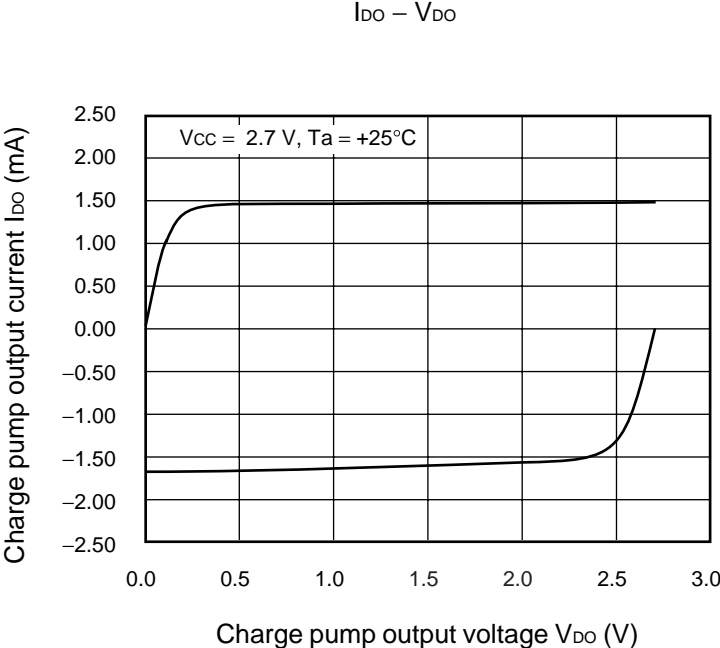
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2. OSC_{IN} input sensitivity

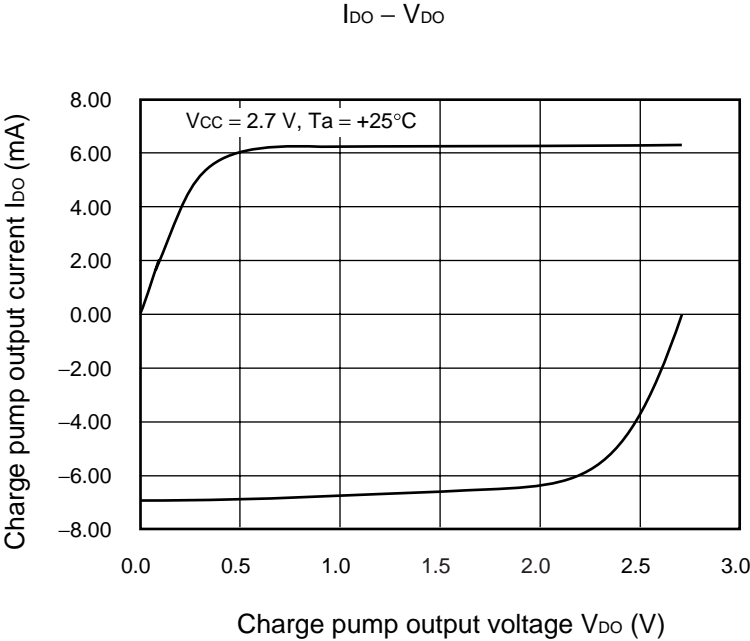


3. RF/IF-PLL Do output current

- 1.5 mA mode

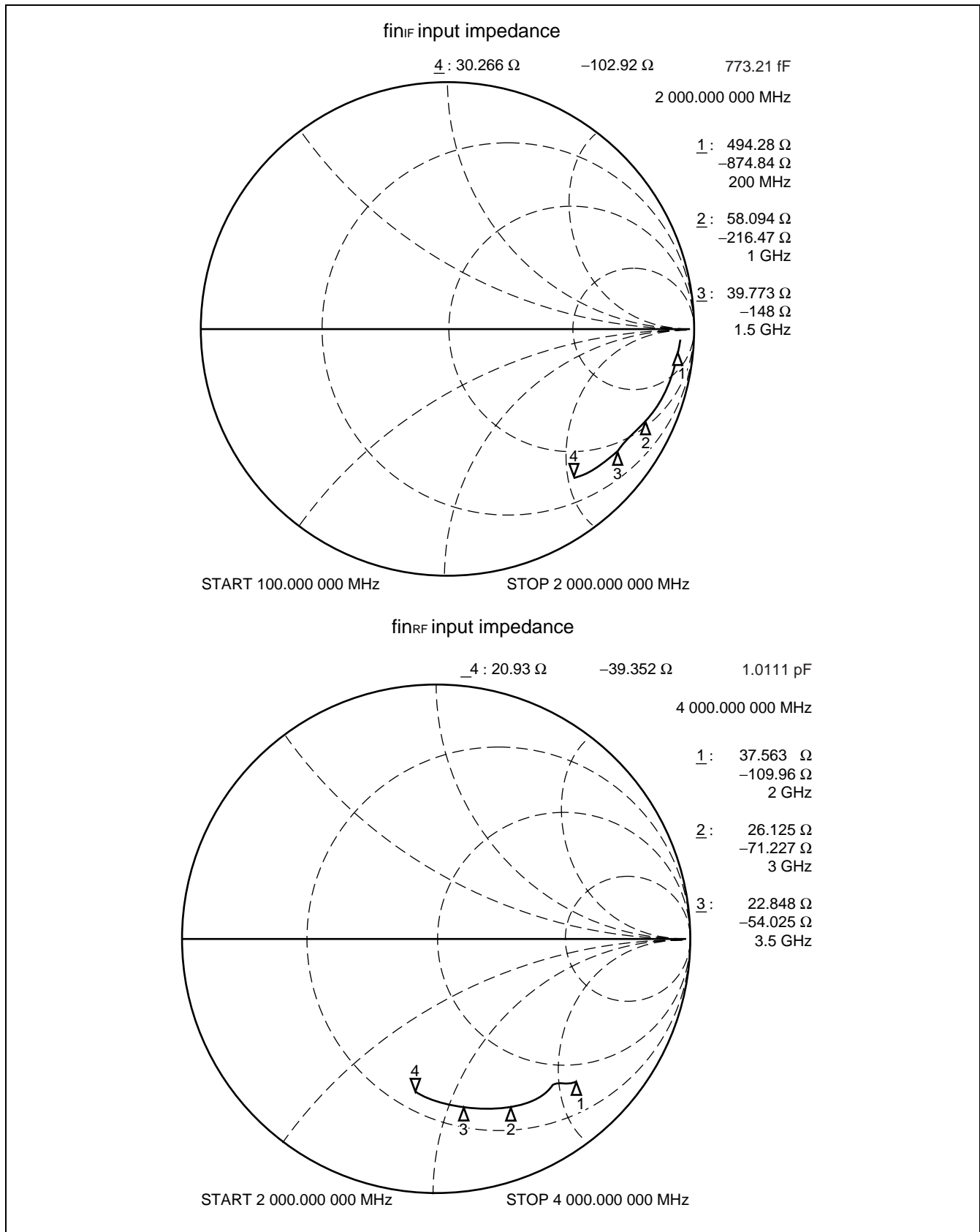


- 6.0 mA mode

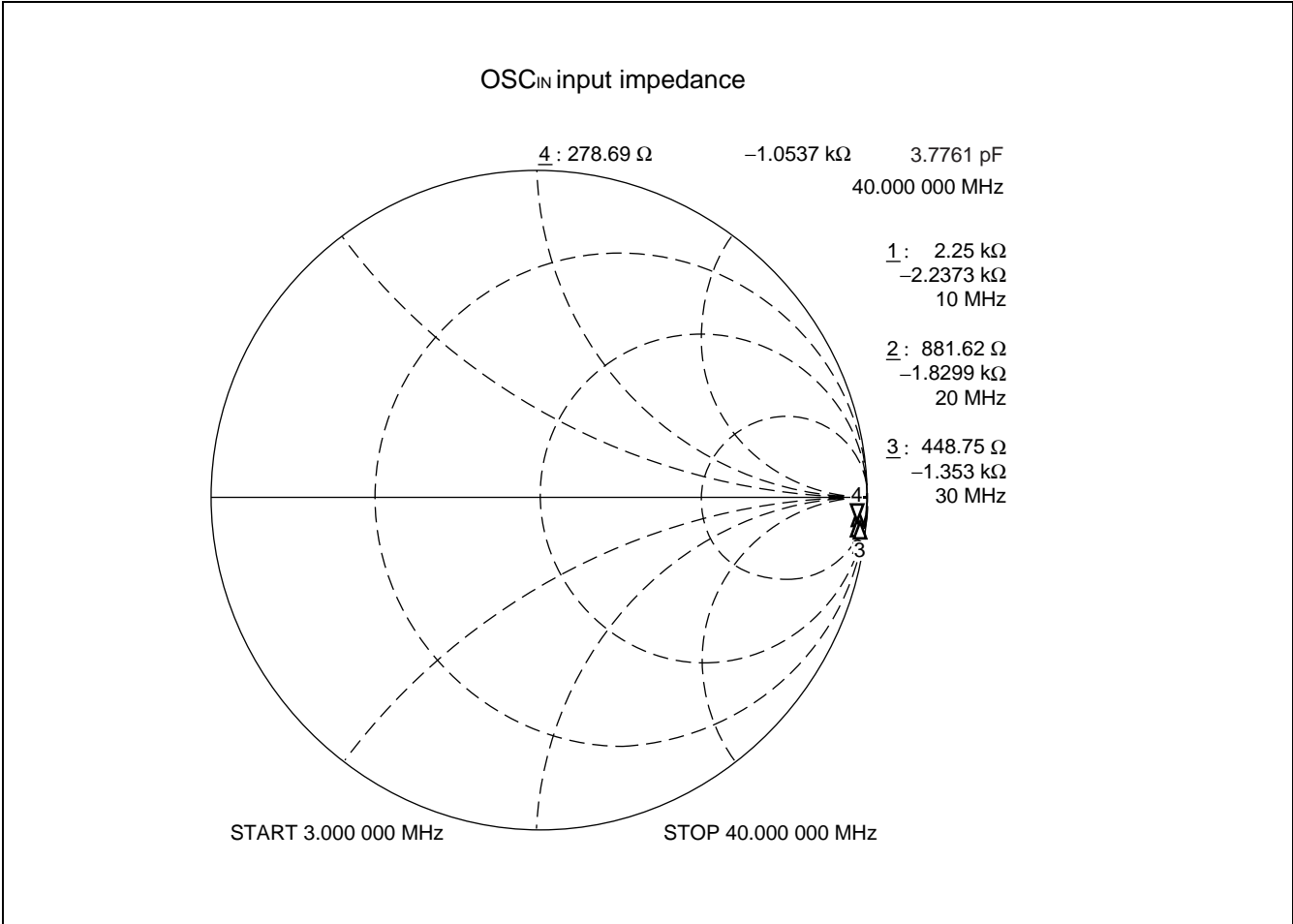


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4. fin input impedance



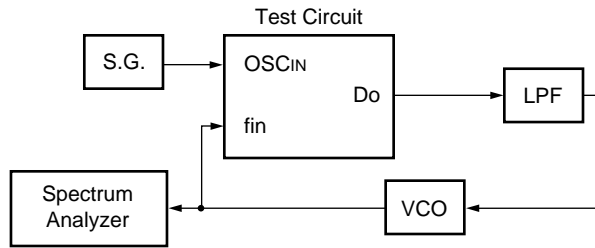
5. OSC_{IN} input impedance



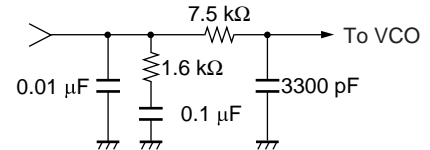
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REFERENCE INFORMATION

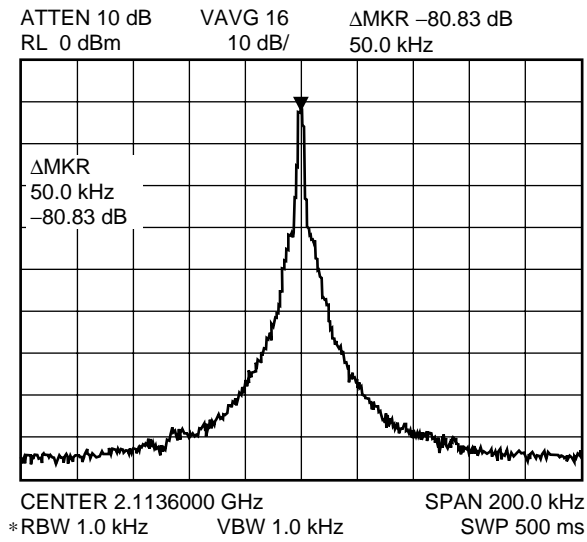
(for Lock-up Time, Phase Noise and Reference Leakage)



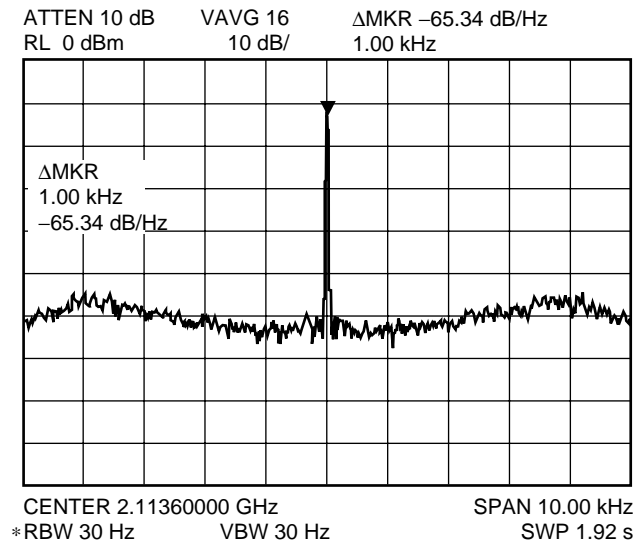
$f_{vco} = 2113.6 \text{ MHz}$ $V_{cc} = 3.0 \text{ V}$
 $K_v = 50 \text{ MHz/V}$ $T_a = +25 \text{ }^\circ\text{C}$
 $f_r = 50 \text{ kHz}$ $CP : 6 \text{ mA mode}$
 $f_{osc} = 19.2 \text{ MHz}$
 LPF



• PLL Reference Leakage



• PLL Phase Noise



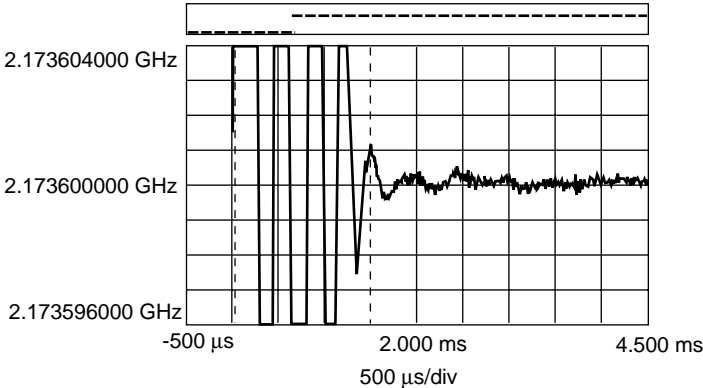
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PLL Lock Up time

2113.6 MHz→2173.6 MHz within ± 1 kHz
L ch→H ch 1.47 ms

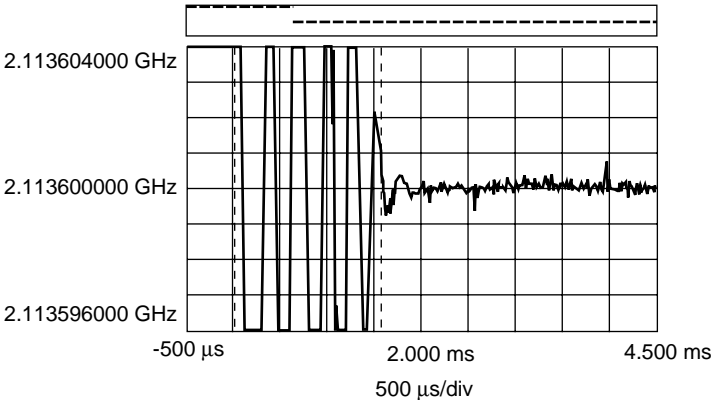
A Mkr x: 439.99764 μs
y: 50.0009 MHz



PLL Lock Up time

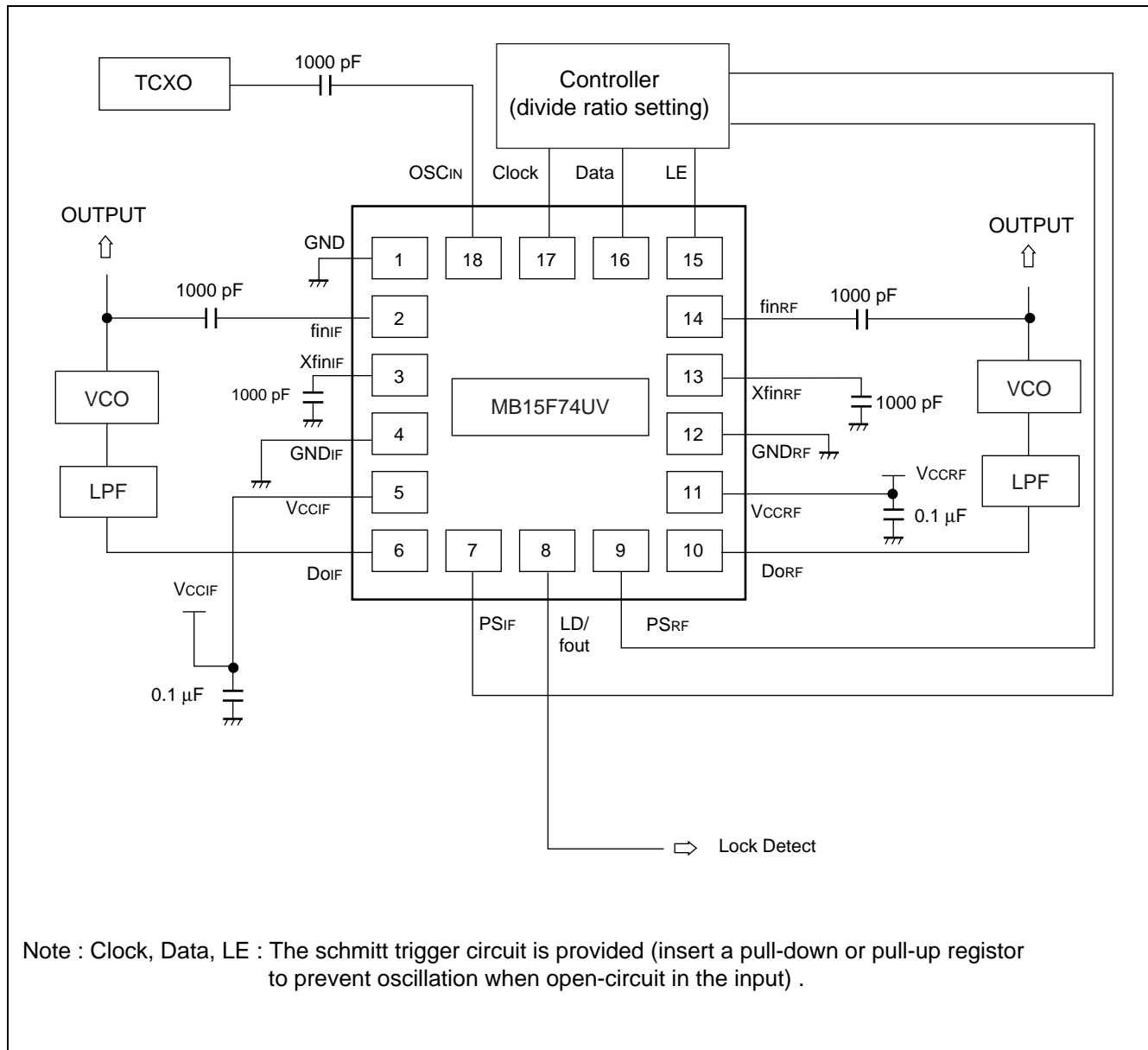
2173.6 MHz→2113.6 MHz within ± 1 kHz
H ch→L ch 1.56 ms

A Mkr x: 400.00146 μs
y: -50.0013 MHz



MB15F74UV

APPLICATION EXAMPLE



■ USAGE PRECAUTIONS

(1) V_{CCRF} and V_{CCIF} must be equal voltage.

Even if either RF-PLL or IF-PLL is not used, power must be supplied to V_{CCRF} and V_{CCIF} to keep them equal. It is recommended that the non-use PLL is controlled by power saving function.

(2) To protect against damage by electrostatic discharge, note the following handling precautions :

- Store and transport devices in conductive containers.
- Use properly grounded workstations, tools, and equipment.
- Turn off power before inserting or removing this device into or from a socket.
- Protect leads with conductive sheet, when transporting a board mounted device

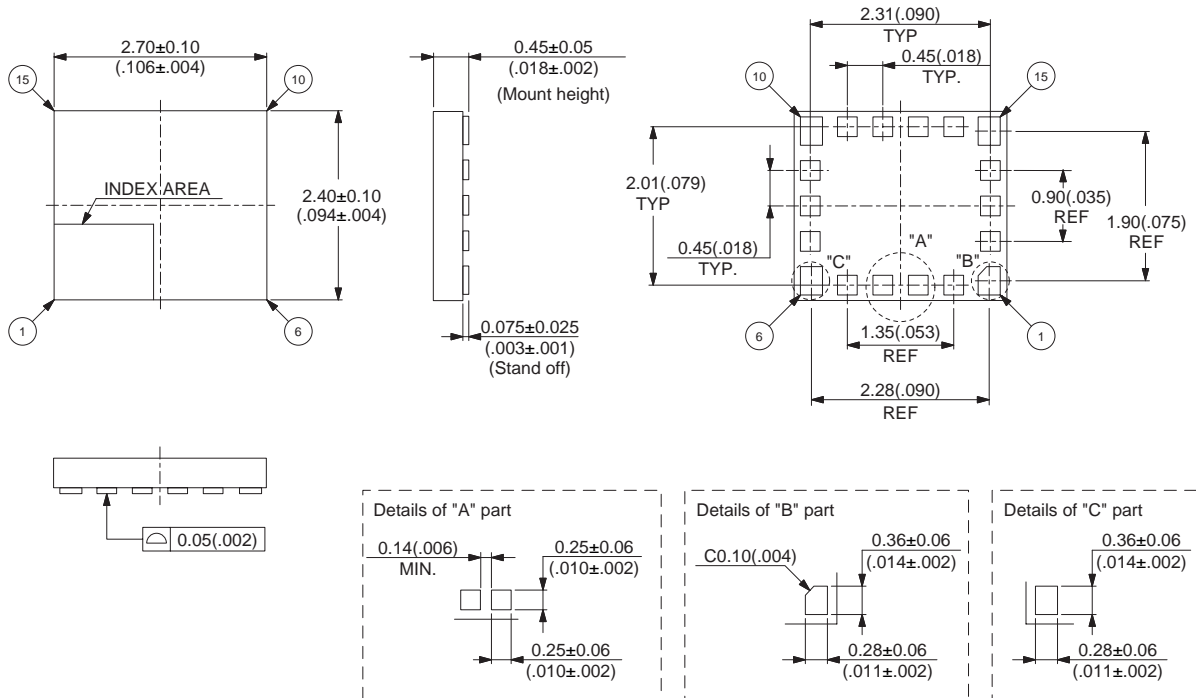
■ ORDERING INFORMATION

Part number	Package	Remarks
MB15F74UVPVB	18-pin plastic BCC (LCC-18P-M05)	

MB15F74UV

■ PACKAGE DIMENSION

18-pin plastic BCC
(LCC-18P-M05)



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Dimensions in mm (inches)

Note : The values in parentheses are reference values.

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