SPECIFICATION

TCC76x

32-bit RISC
Microprocessor
For
Digital Media Player

Rev. 0.07

February 23, 2005

Telechips

Preliminary

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Revision History

Date	Revision	Description
2004-05-10	0.00	Initial release
2004-06-07	0.01	Temporary release for review.
2004-07-27	0.02	• TCC766/TCC767 descriptions added. • TCC763/TCC764 pin description updated. • Added and modified some descriptions for clarification. • Corrected typographical errors.
2004-08-19	0.03	• Operating temperature range increased.
2004-09-10	0.04	• Electrical specification for the NOR Flash and audio CODEC.
2004-09-29	0.05	• Audio CODEC specification updated. • Corrected PW bits of CSCFGx register. • Corrected Block Diagrams for the TCC763/4/6/7
2005-02-03	0.06	• TCC768 added. • Register level descriptions removed from Section 3. (CPU) • Corrected errors in SDCFG/MCFG register descriptions.
2005-02-23	0.07	• TCC761 pin description corrected (PD[15:0]). • TCC763/4/6/7 pin description - Voltage range for VDDIO corrected. • GPIO – Block diagram and description for pull-up resistor. • Interrupt Controller – Block diagram and wakeup event register description. • Clock Generator – Power Down, IDLE mode and register description modified.

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1 INTRODUCTION

The TCC76x is a system LSI for digital media player based on the ARM940T, ARM's proprietary 32-bit RISC CPU core. It can decode and encode MP3 or other types of audio/voice compression/decompression standards by software based architecture. The on-chip USB controller enables the data transmission between a personal computer and storage device such as NAND flash, HDD, CD etc.

Table 1.1 TCC76x Derivatives

Name	Package	Description
TCC760	128-TQFP-1414	Minimal feature set for digital media player
TCC761	208-LQFP-2828	TCC760 + LCD Interface + 32bit External Bus
	208-TBGA-1515	
TCC763	144-FPBGA-1010	TCC760 + 512KB NOR Flash + High performance Audio CODEC
TCC764	144-FPBGA-1010	TCC760 + 1MB NOR Flash + High performance Audio CODEC
TCC766	232-FPBGA-1414	TCC760 + 1MB NOR Flash + High performance Audio CODEC + USB2.0
TCC767	225-FPBGA-1313	TCC760 + 1MB NOR Flash + USB2.0
TCC768	144-FPBGA-1010	TCC760 + 512KB NOR Flash + High performance Audio CODEC + 2MB SDRAM

1.1 Features

- ARM940T CPU core
  - 4KB instruction, 4KB data cache
  - Operating up to 140MHz

- 4Kbytes of internal boot ROM with various boot procedure (NAND, UART) and security

- 64K bytes of internal SRAM for general usage

- On-chip peripherals (TCC760 and TCC761 Core Blocks)
  - External Memory controller for various memories including PROM, NOR & NAND Flash, SRAM, SDRAM, DDR SDRAM (optional), etc.
  - IDE Interface for HDD or external USB 2.0 device
  - USB1.1 Host & device (Full speed)
  - LCD controller supporting STN, TFT type LCD as well as NTSC/PAL interface (TCC761 only)
  - Video input port for CMOS sensor module interface (TCC761 / TCC760 only)
  - ECC generator for SLC and MLC NAND Flash
  - I2S interface for external audio CODEC
  - I2S interface for CD-DSP interface
  - UART/IrDA for serial host interface
  - GSIO for supporting various serial interfaces
  - GPIO for various purposes
  - Support 4 external interrupts
  - I2C compatible serial bus
  - 2-Channel DMA for transferring a bulk of data
  - Four 16bit timer/counters with PWM output and two 20bit timers
  - 32-bit 1Hz counter
  - General purpose 10-bit ADC
  - JTAG interface for code debugging

- 4 or 8Mbits of NOR Flash (TCC763 ~ TCC768)

- High performance Audio CODEC (TCC763, TCC764, TCC766 and TCC768)
  - Highly Efficient Headphone Driver
  - Microphone Input

  - Volume Control and Mute

- USB 2.0 Interface (TCC766/TCC767 only)

- Memory Card Interfaces Cores (TCC766/TCC767 only)
  - Memory Stick (MS)
  - Memory Stick PRO(MSPRO)
  - SecureDigital Card (SD)
  - MultiMedia Card (MMC)
  - Build-in NAND Flash Memory Controller

- 16Mbits of SDRAM (TCC768 only)

- 0.18um low power CMOS process

- 1.5V ~ 1.95V for core, 1.8V ~ 3.6V for I/O port (TCC760 / TCC761 signals)

1.2 Applications

- Portable MP3 player (Flash or CD type)
- MP3 Juke Box
- Digital Audio Encoder/Decoder
- Digital Internet Radio Server
- Multimedia Storage Device
- Low cost PDA

1.3 Block Diagram

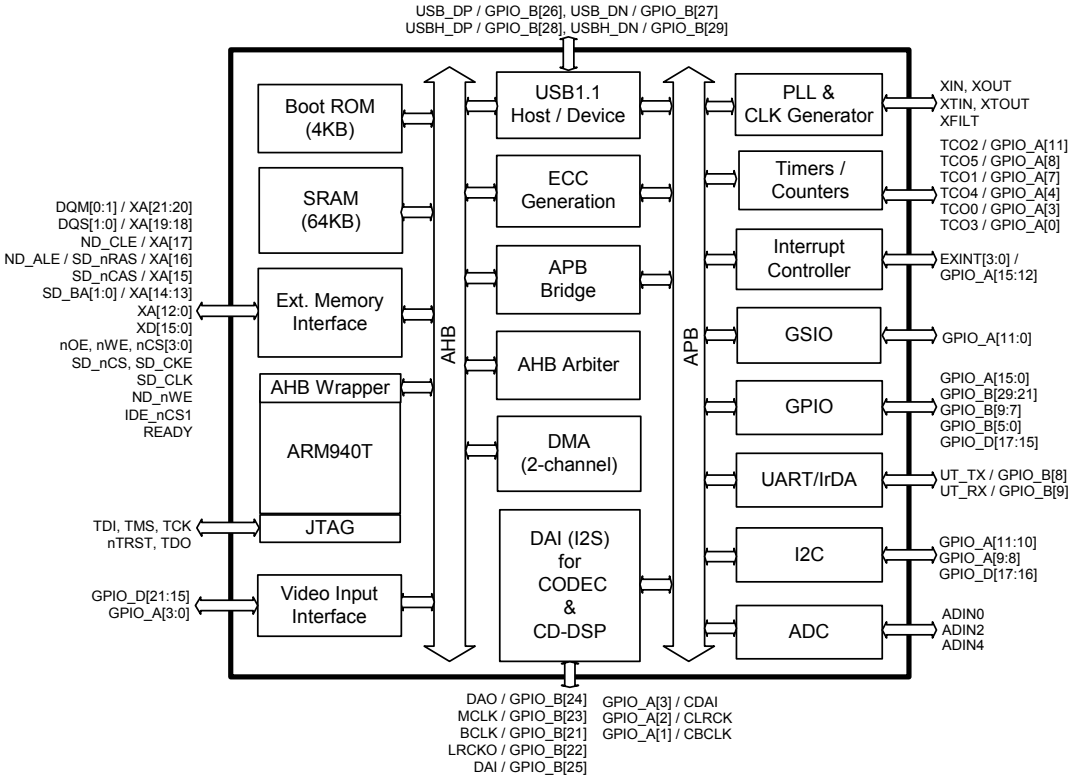


Figure 1.1 TCC760 Functional Block Diagram

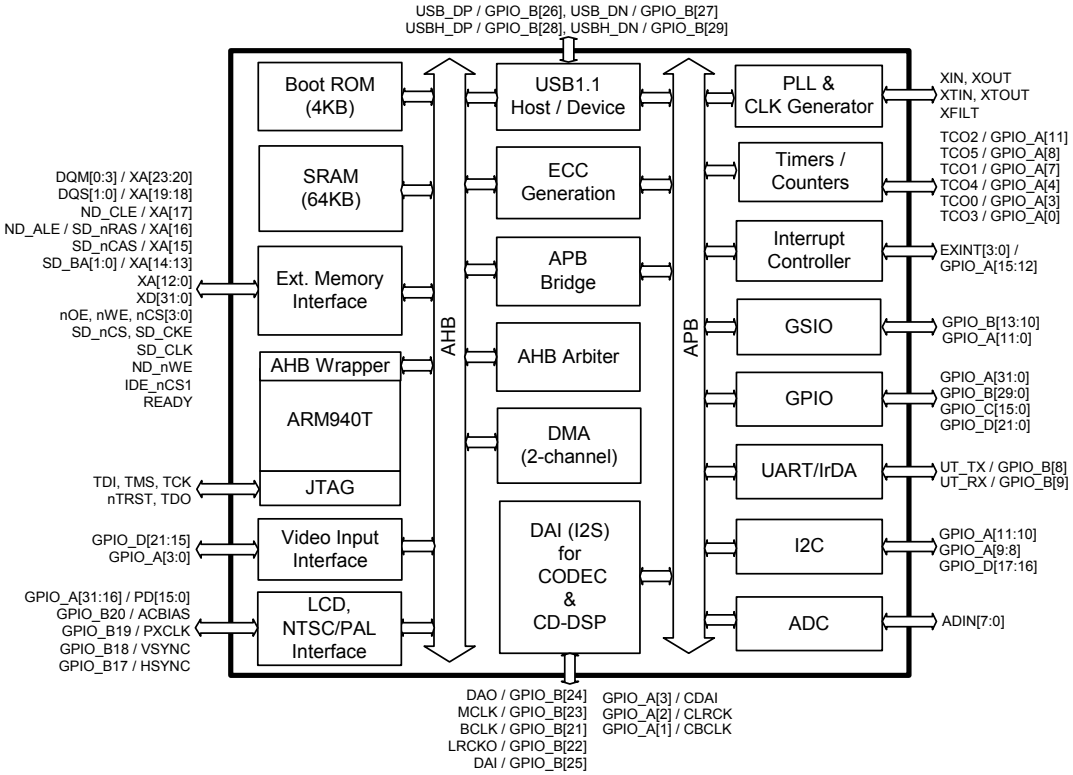


Figure 1.2 TCC761 Functional Block Diagram

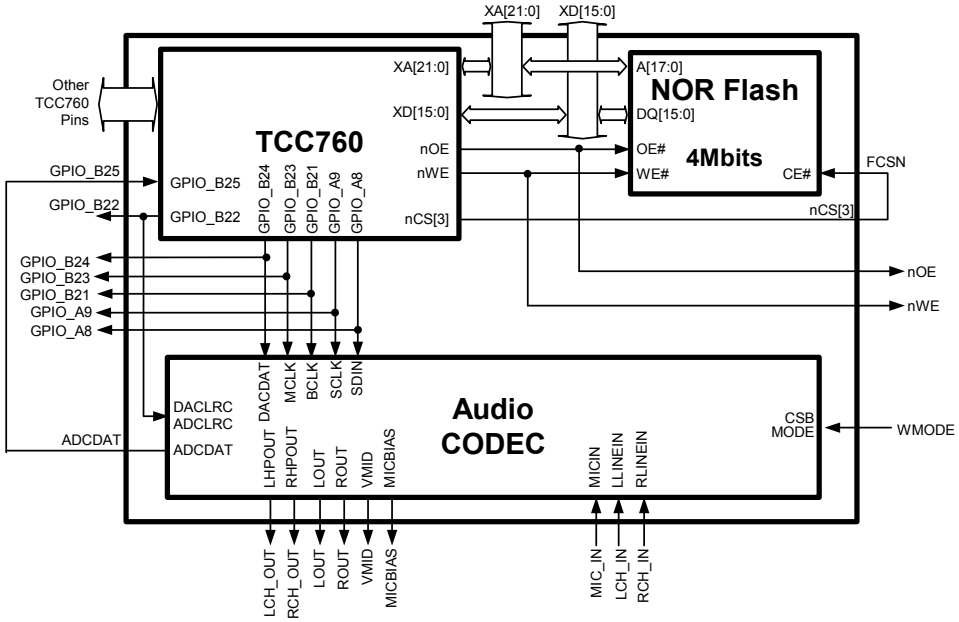


Figure 1.3 TCC763 Functional Block Diagram

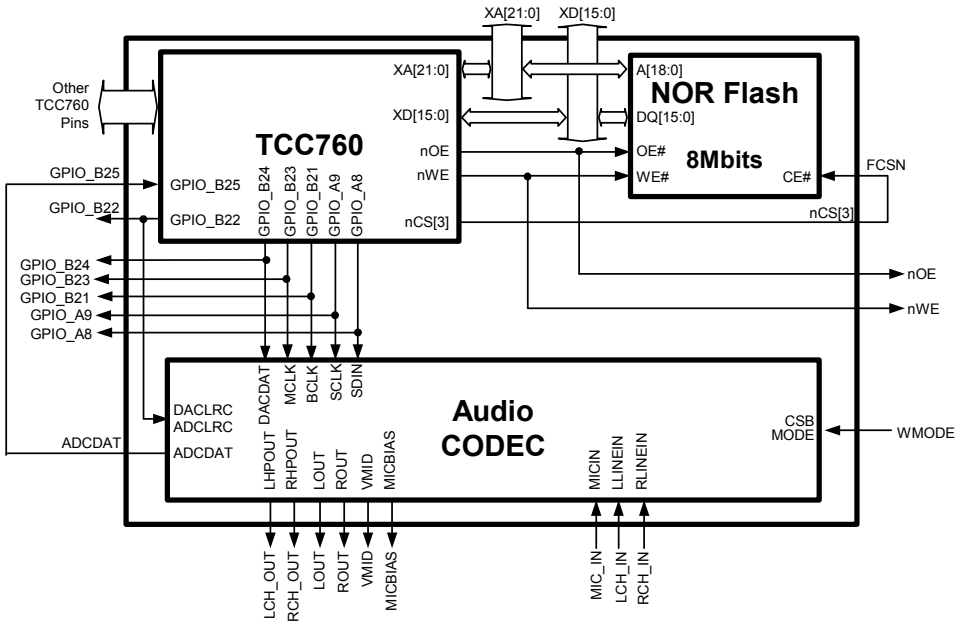


Figure 1.4 TCC764 Functional Block Diagram

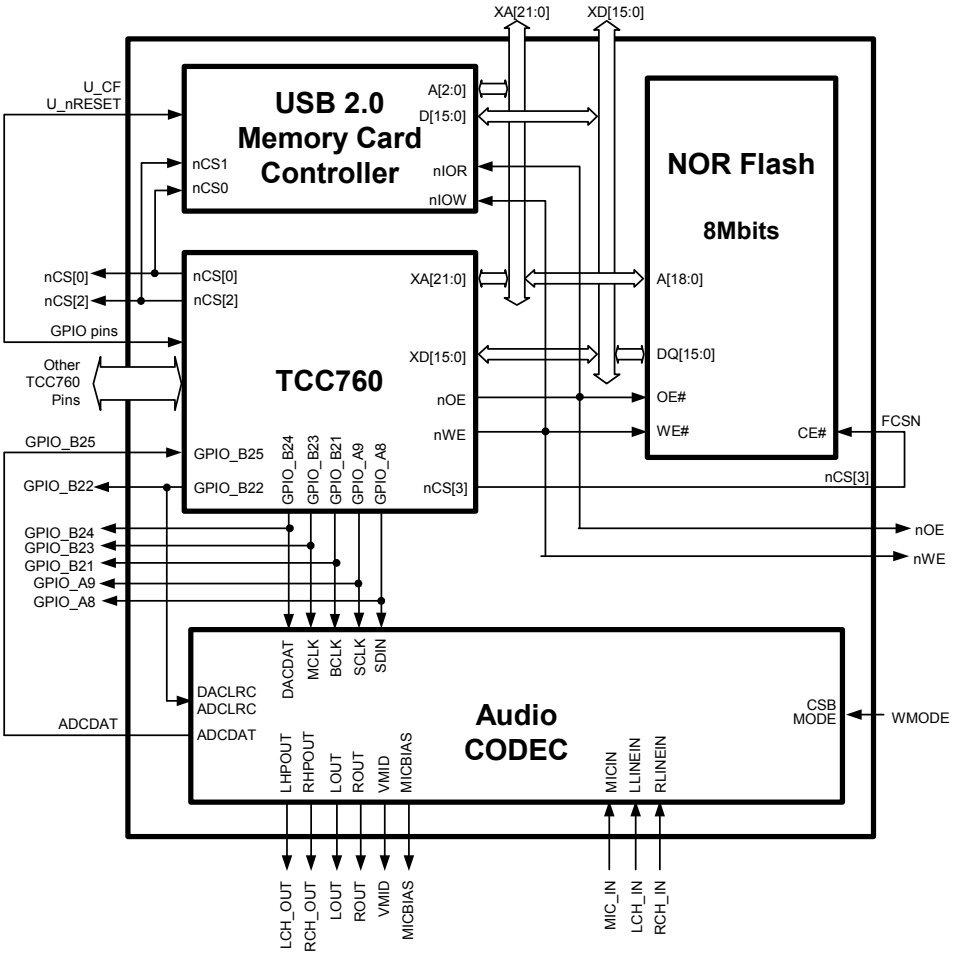


Figure 1.5 TCC766 Functional Block Diagram

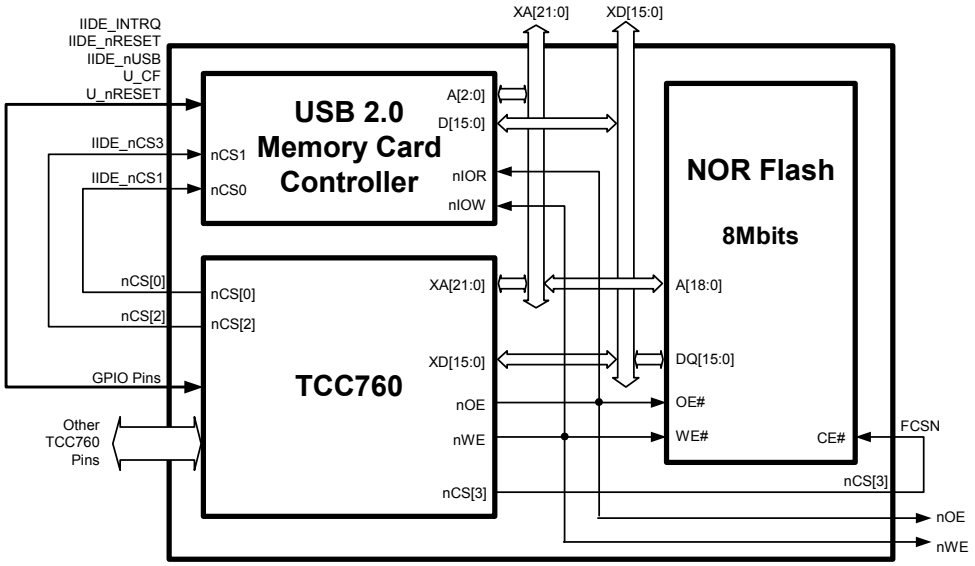


Figure 1.6 TCC767 Functional Block Diagram

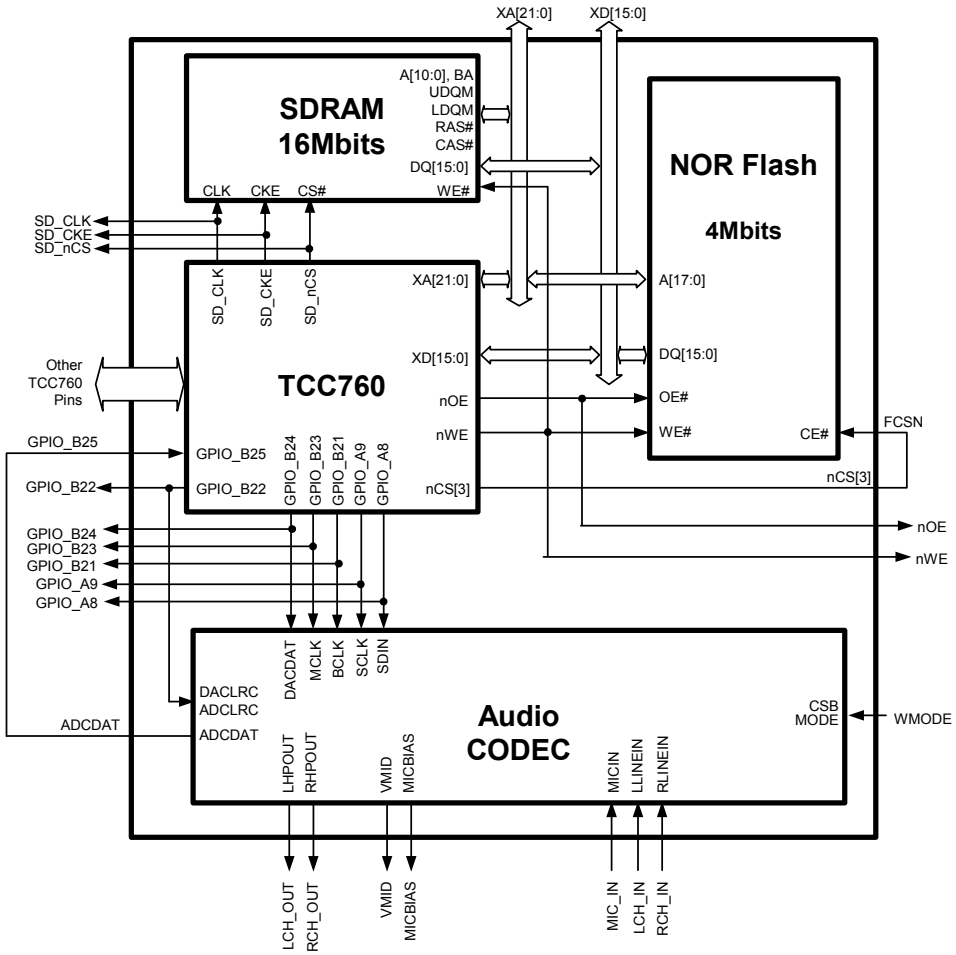


Figure 1.7 TCC768 Functional Block Diagram

1.4 Pin Description

The status of the following GPIO pins are latched at the rising edge of nRESET and used to determine the system bus width and boot mode. External devices must not drive output levels onto these pins during reset period.

Pin Name	State during reset	State after reset	During normal function with DAI enabled
GPIO_A[9] / BW[1] GPIO_A[8] / BW[0]	Bus Width Configuration Input	Normal GPIO Input Mode	GPIO Output Mode for 2-Wire Interface Clock and Data
GPIO_B[24] / BM[2] GPIO_B[22] / BM[1] GPIO_B[21] / BM[0]	Boot Mode Configuration Input	Normal GPIO Input Mode	DAO (I2S Digital Audio Output) LRCK (I2S Word Clock Output) BCLK (I2S Bit Clock Output)

Refer to sections "BOOTING PROCEDURE" and "MEMORY CONTROLLER" for detailed description of BW[1:0] and BM[2:0].

In case of the TCC763, TCC764, TCC766 and TCC768, GPIO_B[22:21]/BM[1:0] signals are connected to internal audio CODEC pins which have on-chip pull-down resistor. If external pull-up resistors are required for these pins, 4.7kΩ is recommended.

The TCC76x is a CMOS device. Floating level on input signals cause unstable device operation and abnormal current consumption. Pull-up or pull-down resistors should be used appropriately for input or bidirectional pins.

Notation

I : Input
O: Output
I/O: Bidirectional
AI: Analog Input
AO: Analog Output
PWR: Power
GND: Ground

1.4.1 TCC760 Pin Description

Table 1.2 TCC760 Pin Description

Signal Name	Shared Signal	Pin #	Type	Description – TCC760
				External Memory Interface Pins
SD_CKE	GPIO_B[0]	56	I/O	SDRAM Clock Enable signal. Active high. / GPIO_B[0]
SD_CLK	GPO	44	I/O	SDRAM Clock / GPO. SD_CLK can be used as a general purpose output. Refer to section "MEMORY CONTROLLER". (MCFG register Bit[3] and Bit[1])
SD_nCS	SD_nCLK / GPIO_B[1]	46	I/O	Chip select signal for SDRAM, Active low / Inverted SD_CLK for DDR SDRAM / GPIO_B[1]
XA[21:20]	DQM[0:1]	43:42	I/O	External Bus Address Bit [21:20] / Data I/O Mask 0, 1
XA[19:18]	DQS[1:0]	40:39	I/O	External Bus Address Bit [19:18] / DDR SDRAM Data Strobe [1:0]
XA[17]	ND_CLE	38	I/O	External Bus Address Bit [17] / CLE for NAND Flash
XA[16]	SD_nRAS / ND_ALE	37	I/O	External Bus Address Bit [16] / SDRAM RAS signal / ALE for NAND Flash
XA[15]	SD_nCAS	36	I/O	External Bus Address Bit [15] / SDRAM CAS signal
XA[14]	SD_BA[1]	35	I/O	External Bus Address Bit [14] / SDRAM Bank Address 1
XA[13]	SD_BA[0]	34	I/O	External Bus Address Bit [13] / SDRAM Bank Address 0.
XA[12:7]		31:26	I/O	External Bus Address Bits [12:0]
XA[6:0]		23:17		
XD[15:9]		15:9	I/O	External Bus Data Bit [15:0]
XD[8:4]		6:2		

Signal Name	Shared Signal	Pin #	Type	Description – TCC760
XD[3:0]		128:125		
NCS[3:0]	ND_nOE[3:0] / GPIO_B[5:2]	50:47	I/O	External Bus Chip Select [3:0] / NAND Flash Output Enable [3:0] / GPIO_B[5:2]
ND_nWE	GPIO_B[7]	57	I/O	NAND flash WE. Active low. / GPIO_B[7]
nWE		58	I/O	Static Memory Write Enable signal. Active low.
nOE		59	I/O	Static Memory Output Enable signal. Active low.
READY		73	I	Ready information from external device.
				USB/UART/IrDA Interface Pins
USB_DP	GPIO_B[26]	51	I/O	USB Function D+ signal / GPIO_B[26]
USB_DN	GPIO_B[27]	52	I/O	USB Function D- signal / GPIO_B[27]
USBH_DP	GPIO_B[28]	53	I/O	USB Host D+ signal / GPIO_B[28]
USBH_DN	GPIO_B[29]	54	I/O	USB Host D- signal / GPIO_B[29]
UT_TX	GPIO_B[8] / SD_nCS	60	I/O	UART or IrDA TX data / GPIO_B[8] / DDR SDRAM Chip Select
UT_RX	GPIO_B[9] / IDE_nCS1	61	I/O	UART or IrDA RX data / GPIO_B[9] / IDE Chip Select 1
				Audio Interface Pins
BCLK	GPIO_B[21] / BM[0]	62	I/O	I2S Bit Clock / GPIO_B[21] / Boot Mode Bit 0
LRCK	GPIO_B[22] / BM[1]	63	I/O	I2S Word Clock / GPIO_B[22] / Boot Mode Bit 1
MCLK	GPIO_B[23]	66	I/O	I2S System Clock / GPIO_B[23]
DAO	GPIO_B[24] / BM[2]	67	I/O	I2S Digital Audio data Output / GPIO_B[24] / Boot Mode Bit 2
DAI	GPIO_B[25]	68	I/O	I2S Digital Audio data Input / GPIO_B[25]
				CD DSP Interface Pins
CBCLK	GPIO_A[1]	105	I/O	CD Data Bit Clock Input / GPIO_A[1]
CLRCK	GPIO_A[2]	106	I/O	CD Data Word Clock Input / GPIO_A[2]
CDAI	GPIO_A[3]	107	I/O	CD Data Input / GPIO_A[3]
				External Interrupt Pins
EXINT[3]	GPIO_A[15]	124	I/O	External Interrupt Request [3] / GPIO_A[15]
EXINT[2:0]	GPIO_A[14:12] / FGPIO[14:12]	123:121	I/O	External Interrupt Request [2:0] / GPIO_A[14:12] / FGPIO[14:12]
				Camera Interface Pins
CISHS	GPIO_D[17]	92	I/O	Horizontal Sync. Input / GPIO_D[17]
CISVS	GPIO_D[16]	91	I/O	Vertical Sync. Input / GPIO_D[16]
CISCLK	GPIO_D[15]	90	I/O	Clock Input / GPIO_D[15]
CISD[7:4] **CISD[3:0]**	GPIO_D[21:18] GPIO_A[3:0]	96:93 107:104	I/O	Data Input[7:0] / GPIO_D[21:18], GPIO_A[3:0]
				General Purpose I/O Pins
GPIO_A[15]	EXINT[3]	124	I/O	GPIO_A[15] / External Interrupt 3
GPIO_A[14:12]	EXINT[2:0] / FGPIO[14:12]	123:121	I/O	GPIO_A[15:12] / External Interrupt 3 ~ 0 / Fast GPIO bits 14 ~ 12
GPIO_A[11] **GPIO_A[10]** **GPIO_A[9] / BW[1]** **GPIO_A[8] / BW[0]**	SDI2 / FGPIO[11] / SCL FRM2 / FGPIO[10] / SDA SCK2 / FGPIO[9] / SCL SDO2 / FGPIO[8] / SDA	118:115	I/O	GPIO_A[11:8] / Bus Width bits 1 ~ 0 / General Purpose Serial I/O 2 Fast GPIO bits 11 ~ 8 / I2C signals. The status of BW[1:0] is latched at the rising edge of nRESET and used to determine external bus width. Refer to section "MEMORY CONTROLLER" for BW[1:0] description.
GPIO_A[7:4]	SDI1 / FGPIO[7] FRM1 / FGPIO[6] SCK1 / FGPIO[5] SDO1 / FGPIO[4]	114 113 111 108	I/O	GPIO_A[7:4] / General Purpose Serial I/O 1 / Fast GPIO bits 7 ~ 4
GPIO_A[3:1]	SDI0 / CDAI / FGPIO[3] FRM0 / CLRCK / FGPIO[2] SCK0 / CBCLK / FGPIO[1]	107:105	I/O	GPIO_A[3:1] / General Purpose Serial I/O 0 / CD Interface Signals / Fast GPIO bits 3 ~ 1

Signal Name	Shared Signal	Pin #	Type	Description – TCC760
GPIO_A[0]	SDO0 / FGPIO[0]	104	I/O	GPIO_A[0] / General purpose serial I/O 0 Serial Data Output FGPIO[0]
GPIO_B[29:28]	USBH_DN, USBH_DP	54:53	I/O	GPIO_B[29:28] / USBH_DN, USBH_DP
GPIO_B[27:26]	USB_DN, USB_DP	52:51	I/O	GPIO_B[27:26] / USB_DN, USB_DP
GPIO_B[25] **GPIO_B[24] / BM[2]** **GPIO_B[23]** **GPIO_B[22] / BM[1]** **GPIO_B[21] / BM[0]**	DAI DAO MCLK LRCK BCLK	68 67 66 63 62	I/O	GPIO_B[25:21] / Boot Mode bits 2 ~ 0 / I2S Interface Signals. The status of BM[2:0] is latched at the rising edge of nRESET and used to determine the system boot mode. Refer to sections "BOOTING PROCEDURE" and "MEMORY CONTROLLER" for detailed description on BM[2:0].
GPIO_B[9]	UT_RX	61	I/O	GPIO_B[9] / UART RX Signal
GPIO_B[8]	UT_TX / SD_nCS	60	I/O	GPIO_B[8] / UART TX Signal / DDR SDRAM Chip Select
GPIO_B[7]	ND_nWE	57	I/O	GPIO_B[7] / Write Enable for NAND Flash
GPIO_B[5:2]	nCS[3:0]	50:47	I/O	GPIO_B[5:2] / External Chip Select 3 ~ 0
GPIO_B[1]	SD_nCS / SD_nCLK	46	I/O	GPIO_B[1] / Chip select for SDRAM / Inverted Clock for DDR SDRAM.
GPIO_B[0]	SD_CKE	56	I/O	GPIO_B[0] / SDRAM clock control
GPIO_D[21:18]	FGPIO[14:11] / CISD[7:4]	96:93	I/O	GPIO_D[21:18] / Fast GPIO bits 14 ~11 / Camera Interface Data Inputs 3 ~ 0. Internal pull-up resistors are enabled at reset.
GPIO_D[17]	FGPIO[10] / SCL / CISHS	92	I/O	GPIO_D[17] / Fast GPIO bit 10/ I2C SCL / Camera Interface Hsync.
GPIO_D[16]	FGPIO[9] / SDA / CISVS	91	I/O	GPIO_D[16] / Fast GPIO bit 9 / I2C SDA / Camera Interface Vsync.
GPIO_D[15]	FGPIO[9] / CISCLK	90	I/O	GPIO_D[15] / Fast GPIO bit 8 / Camera Interface Clock
				ADC Input Pins
ADIN_0	-	82	AI	General purpose multi-channel ADC input 0
ADIN_2	-	83	AI	General purpose multi-channel ADC input 2
ADIN_4	-	84	AI	General purpose multi-channel ADC input 4
				Clock Pins
XIN	-	74	I	Main Crystal Oscillator Input for PLL. 12MHz Crystal must be used if USB Boot Mode is required. Input voltage must not exceed VDD_OSC (1.95V max).
XOUT	-	75	O	Main Crystal Oscillator Output for PLL
XFILT	-	78	AO	PLL filter output
XTIN	-	69	I	Sub Crystal Oscillator Input. 32.768kHz is recommended. Input voltage must not exceed VDD_OSC (1.95V max).
XTOUT	-	70	O	Sub Crystal Oscillator Output
				Mode Control Pins
MODE1	-	98	I	Mode Setting Input 1. Pull-down for normal operation.
PKG1	-	89	I	Package ID1, Pull-up for normal operation.
nRESET	-	72	I	System Reset. Active low.
				JTAG Interface Pins
TDI	-	99	I	JTAG serial data input for ARM940T
TMS	-	100	I	JTAG test mode select for ARM940T
TCK	-	101	I	JTAG test clock for ARM940T
TDO	-	102	I/O	JTAG serial data output for ARM940T. External pull-up resistor is required to prevent floating during normal operation.
nTRST	-	103	I	JTAG reset signal for ARM940T. Active low.
				Power Pins
VDDIO	-	112 76 33 16	PWR	Digital Power for I/O (1.8V ~ 3.3V)

Signal Name	Shared Signal	Pin #	Type	Description – TCC760
VDD_USB	-	64	PWR	Power for USB I/O (3.3V)
VDD_OSC	-	71	PWR	Digital Power for Oscillators (1.8V)
VDDI	-	119 109 41 24 7	PWR	Digital Power for Internal Core (1.8V)
VDDI_ADC	-	87	PWR	Digital Power for ADC (1.8V)
VDDA_ADC	-	81	PWR	Analog Power for ADC (3.3V)
VDDA_PLL	-	77	PWR	Analog & Digital Power for PLL (1.8V)
VSSIO	-	97 65 45 32 1	GND	Digital Ground for I/O
VSSI	-	120 110 55 25 8	GND	Digital Ground for Internal
VSSI_ADC	-	88	GND	Digital Ground for ADC
VBBA_ADC	-	86	GND	Analog Ground for ADC
VSSA_ADC	-	85	GND	Analog Ground for ADC
VBBA_PLL	-	80	GND	Analog Ground for PLL
VSSA_PLL	-	79	GND	Analog Ground for PLL

1.4.2 TCC761 Pin Description

Table 1.3 TCC761 Pin Description

Signal Name	Shared Signal	Pin #	Type	Description – TCC761
				External Memory Interface Pins
SD_CKE	GPIO_B[0]	95	I/O	SDRAM Clock Enable signal. Active high. / GPIO_B[0]
SD_CLK	GPO	77	I/O	SDRAM Clock / GPO. SD_CLK can be used as a general purpose output. Refer to section "MEMORY CONTROLLER". (MCFG register Bit[3] and Bit[1])
SD_nCS	SD_nCLK / GPIO_B[1]	80	I/O	Chip select signal for SDRAM, Active low / Inverted SD_CLK for DDR SDRAM / GPIO_B[1]
XA[23:22]	DQM[0:1]	68:67	I/O	External Bus Address Bits [23:22] / Data I/O Mask [0:1]
XA[21:20]	DQM[2:3]	66:65	I/O	External Bus Address Bits [21:20] / Data I/O Mask [2:3]
XA[19:18]	DQS[1:0]	61:60	I/O	External Bus Address Bit [19:18] / DDR SDRAM Data Strobe [1:0]
XA[17]	ND_CLE	59	I/O	External Bus Address Bit [17] / CLE for NAND Flash
XA[16]	SD_nRAS / ND_ALE	58	I/O	External Bus Address Bit [16] / SDRAM RAS signal / ALE for NAND Flash
XA[15]	SD_nCAS	57	I/O	External Bus Address Bit [15] / SDRAM CAS signal
XA[14]	SD_BA[1]	56	I/O	External Bus Address Bit [14] / SDRAM Bank Address 1
XA[13]	SD_BA[0]	55	I/O	External Bus Address Bit [13] / SDRAM Bank Address 0.
XA[12:7]		50:45	I/O	External Bus Address Bits [12:0]
XA[6:0]		38:32		
XD[15:9]		20:14,	I/O	External Bus Data Bit [15:0]
XD[8:4]		7:3,		
XD[3:0]		208:205		
XD[31:24]	GPIO_C[15:8]	76:69	I/O	External Bus Data Bits [31:16] / GPIO_C[15:0]
XD[23:16]	GPIO_C[7:0],	31:24		
NCS[3:0]	ND_nOE[3:0] / GPIO_B[5:2]	84:81	I/O	External Bus Chip Select [3:0] / NAND Flash Output Enable [3:0] / GPIO_B[5:2]
IDE_nCS1	GPIO_B[6]	94	I/O	IDE chip select 1. Active low. / GPIO_B[6]
ND_nWE	GPIO_B[7]	96	I/O	NAND flash WE. Active low. / GPIO_B[7]
nWE		97	I/O	Static Memory Write Enable signal. Active low.
nOE		98	I/O	Static Memory Output Enable signal. Active low.
READY		118	I	Ready information from external device.
				USB/UART/IrDA Interface Pins
USB_DP	GPIO_B[26]	88	I/O	USB Function D+ signal / GPIO_B[26]
USB_DN	GPIO_B[27]	89	I/O	USB Function D- signal / GPIO_B[27]
USBH_DP	GPIO_B[28]	90	I/O	USB Host D+ signal / GPIO_B[28]
USBH_DN	GPIO_B[29]	91	I/O	USB Host D- signal / GPIO_B[29]
UT_TX	GPIO_B[8] / SD_nCS	99	I/O	UART or IrDA TX data / GPIO_B[8] / DDR SDRAM Chip Select
UT_RX	GPIO_B[9] / IDE_nCS1	100	I/O	UART or IrDA RX data / GPIO_B[9] / IDE Chip Select 1
				Audio Interface Pins
BCLK	GPIO_B[21]	101	I/O	I2S Bit Clock / GPIO_B[21] / Boot Mode Bit 0
LRCK	GPIO_B[22]	102	I/O	I2S Word Clock / GPIO_B[22] / Boot Mode Bit 1
MCLK	GPIO_B[23]	107	I/O	I2S System Clock / GPIO_B[23]
DAO	GPIO_B[24]	108	I/O	I2S Digital Audio data Output / GPIO_B[24] / Boot Mode Bit 2
DAI	GPIO_B[25]	109	I/O	I2S Digital Audio data Input / GPIO_B[25]
				CD DSP Interface Pins
CBCLK	GPIO_B[14]	85	I/O	CD Data Bit Clock Input / GPIO_B[14]

Signal Name	Shared Signal	Pin #	Type	Description – TCC761
CLRCK	GPIO_B[15]	86	I/O	CD Data Word Clock Input / GPIO_B[15]
CDAI	GPIO_B[16]	87	I/O	CD Data input / GPIO_B[16]
				External Interrupt Pins
EXINT[3]	GPIO_A[15]	204	I/O	External Interrupt Request [3] / GPIO_A[15]
EXINT[2:0]	GPIO_A[14:12]/FGPIO[14:12]	203:201	I/O	External Interrupt Request [2:0] / GPIO_A[14:12] / FGPIO[14:12]
				LCD, NTSC/PAL Interface Pins
HSYNC	GPIO_B[17]	165	I/O	Line sync / GPIO_B[17]
VSYNC	GPIO_B[18]	166	I/O	Frame sync / GPIO_B[18]
PXCLK	GPIO_B[19]	167	I/O	Pixel clock / GPIO_B[19]
AC_BIAS	GPIO_B[20]	168	I/O	AC bias control signal / GPIO_B[20]
PD[15:12] **PD[11:6]** **PD[5:4]** **PD[3:0]**	GPIO_A[31:28] GPIO_A[27:22] GPIO_A[21:20] GPIO_A[19:16]	177:174 130:125 122:121 115:112	I/O	Pixel data bus [15:0] / GPIO_A[31:16]
				Camera Interface Pins
CISHS	GPIO_D[17]	152	I/O	Horizontal Sync. Input / GPIO_D[17]
CISVS	GPIO_D[16]	151	I/O	Vertical Sync. Input / GPIO_D[16]
CISCLK	GPIO_D[15]	150	I/O	Clock Input / GPIO_D[15]
CISD[7:4] **CISD[3:0]**	GPIO_D[21:18] GPIO_A[3:0]	156:153 172:169	I/O	Data Input[7:0] / GPIO_D[21:18], GPIO_A[3:0]
				General Purpose I/O Pins
GPIO_A[31:28] **GPIO_A[27:22]** **GPIO_A[21:20]** **GPIO_A[19:16]**	PD[15:12] PD[11:6] PD[5:4] PD[3:0]	177:174, 130:125 122:121 115:112	I/O	GPIO_A[31:16] / Pixel Data Bus [15:0]
GPIO_A[15]	EXINT[3]	204	I/O	GPIO_A[15] / External Interrupt Request 3
GPIO_A[14:12]	EXINT[2:0] / FGPIO[14:12]	203:201	I/O	GPIO_A[15:12] / External Interrupt Request 3 ~ 0 / Fast GPIO bits 14 ~ 12
GPIO_A[11] **GPIO_A[10]** **GPIO_A[9] / BW[1]** **GPIO_A[8] / BW[0]**	SDI2 / FGPIO[11] / SCL FRM2 / FGPIO[10] / SDA SCK2 / FGPIO[9] / SCL SDO2 / FGPIO[8] / SDA	192:189	I/O	GPIO_A[11:8] / Bus Width bits 1 ~ 0 / General Purpose Serial I/O 2 Fast GPIO bits 11 ~ 8 / I2C signals. The status of BW[1:0] is latched at the rising edge of nRESET and used to determine external bus width. Refer to section "MEMORY CONTROLLER" for BW[1:0] description.
GPIO_A[7:4]	SDI1 / FGPIO[7] FRM1 / FGPIO[6] SCK1 / FGPIO[5] SDO1 / FGPIO[4]	186:185 182 178	I/O	GPIO_A[7:4] / General Purpose Serial I/O 1 / Fast GPIO bits 7 ~ 4
GPIO_A[3:0]	SDI0 / FGPIO[3] / CISD[3] FRM0 / FGPIO[2] / CISD[2] SCK0 / FGPIO[1] / CISD[1] SDO0 / FGPIO[0] / CISD[0]	172:169	I/O	GPIO_A[3:0] / General purpose serial I/O 0 / Fast GPIO bits 3 ~ 0 / Camera Interface Data Inputs 3 ~ 0
GPIO_B[29:28]	USBH_DN, USBH_DP	91:90	I/O	GPIO_B[29:28] / USBH_DN, USBH_DP
GPIO_B[27:26]	USB_DN, USB_DP	89:88	I/O	GPIO_B[27:26] / USB_DN, USB_DP
GPIO_B[25] **GPIO_B[24] / BM[2]** **GPIO_B[23]** **GPIO_B[22] / BM[1]** **GPIO_B[21] / BM[0]**	DAI DAO MCLK LRCK BCLK	109 108 107 102 101	I/O	GPIO_B[25:21] / Boot Mode bits 2 ~ 0 / I2S Interface Signals. The status of BM[2:0] is latched at the rising edge of nRESET and used to determine the system boot mode. Refer to sections "BOOTING PROCEDURE" and "MEMORY CONTROLLER" for detailed description on BM[2:0].

Signal Name	Shared Signal	Pin #	Type	Description – TCC761
GPIO_B[20:17]	ACBIAS PXCLK VSYNC HSYNC	168 167 166 165	I/O	GPIO_B[20:17] / LCD Interface Signals
GPIO_B[16:14]	CDAI CLRCK CBCLK	87 86 85	I/O	GPIO_B[16:14] / CD Interface Signals
GPIO_B[13:10]	SDI13 FRM3 SCK3 SDO3	11:8	I/O	GPIO_B[13:10] / General Purpose Serial I/O 3
GPIO_B[9]	UT_RX	100	I/O	GPIO_B[9] / UART RX Signal
GPIO_B[8]	UT_TX / SD_nCS	99	I/O	GPIO_B[8] / UART TX Signal / DDR SDRAM Chip Select.
GPIO_B[7]	ND_nWE	96	I/O	GPIO_B[7] / Write enable for NAND flash
GPIO_B[6]	IDE_nCS1	94	I/O	GPIO_B[6] / Chip select 1 for IDE Interface
GPIO_B[5:2]	nCS[3:0]	84:81	I/O	GPIO_B[5:2] / External Chip Select 3 ~ 0
GPIO_B[1]	SD_nCS / SD_nCLK	80	I/O	GPIO_B[1] / Chip select for SDRAM / Inverted Clock for DDR SDRAM.
GPIO_B[0]	SD_CKE	95	I/O	GPIO_B[0] / SDRAM clock control
GPIO_C[15:0]	XD[31:24] XD[23:16]	76:69 31:24	I/O	GPIO_C[15:0] / External Data Bus [31:16]
GPIO_D[14] **GPIO_D[13:10]** **GPIO_D[9:8]** **GPIO_D[7:6]** **GPIO_D[5:4]** **GPIO_D[3:1]** **GPIO_D[0]**		200 196:193 188:187 173, 93 64, 62 44:42 21	I/O	GPIO_D[14:0]
GPIO_D[21:18]	FGPIO[14:11] / CISD[7:4]	156:153	I/O	GPIO_D[21:18] / Fast GPIO bits 14 ~11 / Camera Interface Data Inputs 3 ~ 0. Internal pull-up resistors are enabled at reset.
GPIO_D[17]	FGPIO[10] / SCL / CISHS	152	I/O	GPIO_D[17] / Fast GPIO bit 10/ I2C SCL / Camera Interface Hsync.
GPIO_D[16]	FGPIO[9] / SDA / CISVS	151	I/O	GPIO_D[16] / Fast GPIO bit 9 / I2C SDA / Camera Interface Vsync.
GPIO_D[15]	FGPIO[8] / CISCLK	150	I/O	GPIO_D[15] / Fast GPIO bit 8 / Camera Interface Clock
				ADC Input Pins
ADIN[7:0]		143:136	AI	General purpose multi-channel ADC inputs 7 ~ 0
				Clock Pins
XIN		119	I	Main Crystal Oscillator Input for PLL. 12MHz Crystal must be used if USB Boot Mode is required. Input voltage must not exceed VDD_OSC (1.95V max).
XOUT		120	O	Main Crystal Oscillator Output for PLL
XFILT		132	AO	PLL filter output
XTIN		110	I	Sub Crystal Oscillator Input. 32.768kHz is recommended. Input voltage must not exceed VDD_OSC (1.95V max).
XTOUT		111	O	Sub Crystal Oscillator Output
				Mode Control Pins
MODE1		159	I	Mode Setting Input 1. Pull-down for normal operation
PKG1		149	I	Package ID1. Pull-up for normal operation
PKG0		148	I	Package ID0. Pull-down for normal operation
nRESET		117	I	System Reset. Active low.
				JTAG Interface Pins
TDI		160	I	JTAG serial data input for ARM940T
TMS		161	I	JTAG test mode select for ARM940T

Signal Name	Shared Signal	Pin #	Type	Description – TCC761
TCK		162	I	JTAG test clock for ARM940T
TDO		163	I/O	JTAG serial data output for ARM940T. External pull-up resistor is required to prevent floating during normal operation.
nTRST		164	I	JTAG reset signal for ARM940T. Active low.
				Power Pins
VDDIO		184 183 124 123 54 53 23 22	PWR	Digital Power for I/O (1.8V ~ 3.3V)
VDD_USB		104 103	PWR	Power for USB I/O (3.3V)
VDD_OSC		116	PWR	Digital Power for Oscillators (1.8V)
VDDI		198 197 179 63 39 12	PWR	Digital Power for Internal Core (1.8V)
VDDI_ADC		146	PWR	Digital Power for ADC (1.8V)
VDDA_ADC		135	PWR	Analog Power for ADC (3.3V)
VDDA_PLL		131	PWR	Analog & Digital Power for PLL (1.8V)
VSSIO		158 157 106 105 79 78 52 51 2 1	GND	Digital Ground for I/O
VSSI		199 181 180 92 41 40 13	GND	Digital Ground for Internal
VSSI_ADC		147	GND	Digital ground for ADC
VBBA_ADC		145	GND	Analog Ground for ADC
VSSA_ADC		144	GND	Analog Ground for ADC
VBBA_PLL		134	GND	Analog Ground for PLL
VSSA_PLL		133	GND	Analog Ground for PLL

Table 1.4 Mapping between TCC761-E and TCC761-Y

LQFP	TBGA	Name	LQFP	TBGA	Name	LQFP	TBGA	Name	LQFP	TBGA	Name
1	A1	VSSIO	53	U1	VDDIO	105	U17	VSSIO	157	A17	VSSIO
2	C2	VSSIO	54	T3	VDDIO	106	R16	VSSIO	158	B15	VSSIO
3	D4	XD4	55	P4	XA13	107	P14	GPIO_B23	159	D14	MODE1
4	B1	XD5	56	U2	XA14	108	T17	GPIO_B24	160	A16	TDI
5	C1	XD6	57	U3	XA15	109	R17	GPIO_B25	161	A15	TMS
6	D2	XD7	58	T4	XA16	110	P16	XTIN	162	B14	TCK
7	D3	XD8	59	R4	XA17	111	P15	XTOUT	163	C14	TDO
8	E4	GPIO_B10	60	P5	XA18	112	N14	GPIO_A16	164	D13	nTRST
9	D1	GPIO_B11	61	U4	XA19	113	P17	GPIO_A17	165	A14	GPIO_B17
10	E2	GPIO_B12	62	T5	GPIO_D4	114	N16	GPIO_A18	166	B13	GPIO_B18
11	E3	GPIO_B13	63	R5	VDDI	115	N15	GPIO_A19	167	C13	GPIO_B19
12	F4	VDDI	64	P6	GPIO_D5	116	M14	VDDI	168	D12	GPIO_B20
13	E1	VSSI	65	U5	XA20	117	N17	nRESET	169	A13	GPIO_A0
14	F2	XD9	66	T6	XA21	118	M16	MODE0	170	B12	GPIO_A1
15	F3	XD10	67	R6	XA22	119	M15	XIN	171	C12	GPIO_A2
16	G4	XD11	68	P7	XA23	120	L14	XOUT	172	D11	GPIO_A3
17	F1	XD12	69	U6	XD24	121	M17	GPIO_A20	173	A12	GPIO_D7
18	G2	XD13	70	T7	XD25	122	L16	GPIO_A21	174	B11	GPIO_A28
19	G3	XD14	71	R7	XD26	123	L15	VDDIO	175	C11	GPIO_A29
20	H4	XD15	72	P8	XD27	124	K14	VDDIO	176	D10	GPIO_A30
21	G1	GPIO_D0	73	U7	XD28	125	L17	GPIO_A22	177	A11	GPIO_A31
22	H2	VDDIO	74	T8	XD29	126	K16	GPIO_A23	178	B10	GPIO_A4
23	H3	VDDIO	75	R8	XD30	127	K15	GPIO_A24	179	C10	VDDI
24	J4	XD16	76	P9	XD31	128	J14	GPIO_A25	180	D9	VSSI
25	H1	XD17	77	U8	SD_CLK	129	K17	GPIO_A26	181	A10	VSSI
26	J2	XD18	78	T9	VSSIO	130	J16	GPIO_A27	182	B9	GPIO_A5
27	J3	XD19	79	R9	VSSIO	131	J15	VDDA_PLL	183	C9	VDDIO
28	K4	XD20	80	P10	GPIO_B1	132	H14	XFILT	184	D8	VDDIO
29	J1	XD21	81	U9	GPIO_B2	133	J17	VSSA_PLL	185	A9	GPIO_A6
30	K2	XD22	82	T10	GPIO_B3	134	H16	VBBA_PLL	186	B8	GPIO_A7
31	K3	XD23	83	R10	GPIO_B4	135	H15	VDDA_ADC	187	C8	GPIO_D8
32	L4	XA0	84	P11	GPIO_B5	136	G14	ADIN_0	188	D7	GPIO_D9
33	K1	XA1	85	U10	GPIO_B14	137	H17	ADIN_1	189	A8	GPIO_A8
34	L2	XA2	86	T11	GPIO_B15	138	G16	ADIN_2	190	B7	GPIO_A9
35	L3	XA3	87	R11	GPIO_B16	139	G15	ADIN_3	191	C7	GPIO_A10
36	M4	XA4	88	P12	USB_DP	140	F14	ADIN_4	192	D6	GPIO_A11
37	L1	XA5	89	U11	USB_DN	141	G17	ADIN_5	193	A7	GPIO_D10
38	M2	XA6	90	T12	USBH_DP	142	F16	ADIN_6	194	B6	GPIO_D11
39	M3	VDDI	91	R12	USBH_DN	143	F15	ADIN_7	195	C6	GPIO_D12
40	N4	VSSI	92	P13	VSSI	144	E14	VSSA_ADC	196	D5	GPIO_D13
41	M1	VSSI	93	U12	GPIO_D6	145	F17	VBBA_ADC	197	A6	VDDI
42	N2	GPIO_D1	94	T13	GPIO_B6	146	E16	VDDI_ADC	198	B5	VDDI
43	N3	GPIO_D2	95	R13	GPIO_B0	147	E15	VSSI_ADC	199	C5	VSSI
44	N1	GPIO_D3	96	U13	GPIO_B7	148	E17	PKG0	200	A5	GPIO_D14
45	P1	XA7	97	U14	nWE	149	D17	PKG1	201	A4	GPIO_A12
46	P2	XA8	98	T14	nOE	150	D16	GPIO_D15	202	B4	GPIO_A13
47	P3	XA9	99	R14	GPIO_B8	151	D15	GPIO_D16	203	C4	GPIO_A14
48	R1	XA10	100	U15	GPIO_B9	152	C17	GPIO_D17	204	A3	GPIO_A15
49	T1	XA11	101	U16	GPIO_B21	153	B17	GPIO_D18	205	A2	XD0
50	R2	XA12	102	T15	GPIO_B22	154	C16	GPIO_D19	206	B3	XD1
51	R3	VSSIO	103	R15	VDD_USB	155	C15	GPIO_D20	207	C3	XD2
52	T2	VSSIO	104	T16	VDD_USB	156	B16	GPIO_D21	208	B2	XD3

1.4.3 TCC763 / TCC764 Pin Description

Table 1.5 TCC763 / TCC764 Pin Description

Signal Name	Shared Signal	Ball	Type	Description – TCC763/ TCC764
				External Memory Interface Pins
SD_CKE	GPIO_B[0]	J8	I/O	SDRAM Clock Enable signal. Active high. / GPIO_B[0]
SD_CLK	GPO	L5	I/O	SDRAM Clock / GPO. SD_CLK can be used as a general purpose output. Refer to section "MEMORY CONTROLLER". (MCFG register Bit[3] and Bit[1])
SD_nCS	SD_nCLK / GPIO_B[1]	L6	I/O	Chip select signal for SDRAM, Active low / Inverted SD_CLK for DDR SDRAM / GPIO_B[1]
XA[21:20]	DQM[0:1]	L4,K4	I/O	External Bus Address Bit [21:20] / Data I/O Mask 0, 1
XA[19:18]	DQS[1:0]	K3,L2	I/O	External Bus Address Bit [19:18] / DDR SDRAM Data Strobe [1:0]
XA[17]	ND_CLE	L3	I/O	External Bus Address Bit [17] / CLE for NAND Flash
XA[16]	SD_nRAS / ND_ALE	G3	I/O	External Bus Address Bit [16] / SDRAM RAS signal / ALE for NAND Flash
XA[15]	SD_nCAS	M3	I/O	External Bus Address Bit [15] / SDRAM CAS signal
XA[14]	SD_BA[1]	M2	I/O	External Bus Address Bit [14] / SDRAM Bank Address 1
XA[13]	SD_BA[0]	M1	I/O	External Bus Address Bit [13] / SDRAM Bank Address 0.
XA[12:0]		J4, K2 M4, J1 H4, H5 H1, G6 H2, G5 G4, G7 G8	I/O	External Bus Address Bits [12:0]
XD[15:0],		A3, F4 E2, E5 D8, F7 E1, F6 E3, D4 C2, B1 A7, B2 A10, F8	I/O	External Bus Data Bit [15:0]
NCS[3]	ND_nOE[3] / GPIO_B[5]	H6	I/O	External Bus Chip Select [3:0] / NAND Flash Output Enable [3:0] / GPIO_B[5:2]
NCS[2]	ND_nOE[2] / GPIO_B[4]	J6	I/O	
NCS[1]	ND_nOE[1] / GPIO_B[3]	K6	I/O	
NCS[0]	ND_nOE[0] / GPIO_B[2]	J5	I/O	
ND_nWE	GPIO_B[7]	L10	I/O	NAND flash WE. Active low. / GPIO_B[7]
nWE		M5	I/O	Static Memory Write Enable signal. Active low.
nOE		H7	I/O	Static Memory Output Enable signal. Active low.
READY		J11	I	Ready information from external device.
FCSN		A12	I	NOR Flash Chip Select. Should be connected to nCS[3].
				USB/UART/IrDA Interface Pins
USB_DP	GPIO_B[26]	L7	I/O	USB Function D+ signal / GPIO_B[26]
USB_DN	GPIO_B[27]	K8	I/O	USB Function D- signal / GPIO_B[27]
USBH_DP	GPIO_B[28]	L8	I/O	USB Host D+ signal / GPIO_B[28]
USBH_DN	GPIO_B[29]	M9	I/O	USB Host D- signal / GPIO_B[29]
UT_TX	GPIO_B[8] / SD_nCS	M10	I/O	UART or IrDA TX data / GPIO_B[8] / DDR SDRAM Chip Select
UT_RX	GPIO_B[9] / IDE_nCS1	L9	I/O	UART or IrDA RX data / GPIO_B[9] / IDE Chip Select 1
				Audio Interface Pins

Signal Name	Shared Signal	Ball	Type	Description – TCC763/ TCC764
BCLK	GPIO_B[21] / BM[0]	J9	I/O	I2S Bit Clock / GPIO_B[21] / Boot Mode Bit 0. Internal pull-down resistor is active at power up.
LRCK	GPIO_B[22] / BM[1]	L11	I/O	I2S Word Clock / GPIO_B[22] / Boot Mode Bit 1 Internal pull-down resistor is active at power up.
MCLK	GPIO_B[23]	K12	I/O	I2S System Clock / GPIO_B[23]
DAO	GPIO_B[24] / BM[2]	K11	I/O	I2S Digital Audio data Output / GPIO_B[24] / Boot Mode Bit 2
DAI	GPIO_B[25]	K10	I/O	I2S Digital Audio data Input / GPIO_B[25]
ADCDAT		H10	O	I2S Digital Audio data Output of audio CODEC(ADC). Must be connected externally to GPIO_B25 (DAI)
LCH_OUT		E11	AO	DAC Left Channel Output of audio CODEC
RCH_OUT		E12	AO	DAC Right Channel Output of audio CODEC
LOUT		B9	AO	DAC Left Channel Line Output of audio CODEC
ROUT		A8	AO	DAC Right Channel Line Output of audio CODEC
RCH_IN		F1	AI	ADC Right Channel Input of audio CODEC
MIC_IN		A4	AI	Microphone Input of audio CODEC
LCH_IN		F2	AI	ADC Left Channel Input of internal audio CODEC
VMID		B5	AO	Mid-rail reference decoupling point
MICBIAS		D5	AO	Microphone Bias
WMODE	CSB	F3	I	CODEC I/F Control. Pull-down for normal operation. Internal pull-up resistor is active at power up.
SDIN	GPIO_A[8] / BW[0]	D6	I/O	2-Wire MCU Data Input for CODEC
SCLK	GPIO_A[9] / BW[1]	E7	I/O	2-Wire MCU Clock Input for CODEC
				CD DSP Interface Pins
CBCLK	GPIO_A[1]	D9	I/O	CD Data Bit Clock Input / GPIO_A[1]
CLRCK	GPIO_A[2]	E9	I/O	CD Data Word Clock Input / GPIO_A[2]
CDAI	GPIO_A[3]	E8	I/O	CD Data Input / GPIO_A[3]
				External Interrupt Pins
EXINT[3]	GPIO_A15	A2	I/O	External Interrupt Request [3] / GPIO_A[15]
EXINT[2:0]	GPIO_A14 / FGPIO[14] GPIO_A13 / FGPIO[13] GPIO_A12 / FGPIO[12]	D3 B3 C3	I/O	External Interrupt Request [2:0] / GPIO_A[14:12] / FGPIO[14:12]
				General Purpose I/O Pins
GPIO_A[15]	EXINT[3]	A2	I/O	GPIO_A[15] / External Interrupt Request 3
GPIO_A[14:12]	EXINT[2:0] / FGPIO[14:12]	D3 B3 C3	I/O	GPIO_A[15:12] / External Interrupt 3 ~ 0 / Fast GPIO bits 14 ~ 12
GPIO_A[11] **GPIO_A[10]** **GPIO_A[9] / BW[1]** **GPIO_A[8] / BW[0]**	SDI2 / FGPIO[11] / SCL FRM2 / FGPIO[10] / SDA SCK2 / FGPIO[9] / SCL SDO2 / FGPIO[8] / SDA	E4 E6 E7 D6	I/O	GPIO_A[11:8] / Bus Width bits 1 ~ 0 / General Purpose Serial I/O 2 Fast GPIO bits 11 ~ 8 / I2C signals. The status of BW[1:0] is latched at the rising edge of nRESET and used to determine external bus width. Refer to section "MEMORY CONTROLLER" for BW[1:0] description. GPIO_A[9:8] is internally connected with audio CODEC signals. Refer to Figure 1.3 for more information.
GPIO_A[7:4]	SDI1 / FGPIO[7] FRM1 / FGPIO[6] SCK1 / FGPIO[5] SDO1 / FGPIO[4]	B6 C6 B7 B8	I/O	GPIO_A[7:4] / General Purpose Serial I/O 1 / Fast GPIO bits 7 ~ 4
GPIO_A[3:1]	SDI0 / CDAI / FGPIO[3] FRM0 / CLRCK / FGPIO[2] SCK0 / CBCLK / FGPIO[1]	E8 E9 D9	I/O	GPIO_A[3:1] / General Purpose Serial I/O 0 / CD Interface Signals / Fast GPIO bits 3 ~ 1

Signal Name	Shared Signal	Ball	Type	Description – TCC763/ TCC764
GPIO_A[0]	SDO0 / FGPIO[0]	C9	I/O	GPIO_A[0] / General purpose serial I/O 0 Serial Data Output FGPIO[0]
GPIO_B[29:28]	USBH_DN, USBH_DP	M9,L8	I/O	GPIO_B[29:28] / USBH_DN, USBH_DP
GPIO_B[27:26]	USB_DN, USB_DP	K8,L7	I/O	GPIO_B[27:26] / USB_DN, USB_DP
GPIO_B[25] **GPIO_B[24] / BM[2]** **GPIO_B[23]** **GPIO_B[22] / BM[1]** **GPIO_B[21] / BM[0]**	DAI DAO MCLK LRCK BCLK	K10 K11 K12 L11 J9	I/O	GPIO_B[25:21] / Boot Mode bits 2 ~ 0 / I2S Interface Signals. The status of BM[2:0] is latched at the rising edge of nRESET and used to determine the system boot mode. Refer to sections "BOOTING PROCEDURE" and "MEMORY CONTROLLER" for detailed description on BM[2:0]. GPIO_A[24:21] is internally connected with audio CODEC signals. Refer to Figure 1.3 for more information. GPIO_B[22:21] have internal pull-down resistor which is active at power up.
GPIO_B[9]	UT_RX	L9	I/O	GPIO_B[9] / UART RX Signal
GPIO_B[8]	UT_TX / SD_nCS	M10	I/O	GPIO_B[8] / UART TX Signal / DDR SDRAM Chip Select
GPIO_B[7]	ND_nWE	L10	I/O	GPIO_B[7] / Write Enable for NAND Flash
GPIO_B[5:2]	nCS[3:0]	H6, J6 K6, J5	I/O	GPIO_B[5:2] / External Chip Select 3 ~ 0
GPIO_B[1]	SD_nCS / SD_nCLK	L6	I/O	GPIO_B[1] / Chip select for SDRAM / Inverted Clock for DDR SDRAM.
GPIO_B[0]	SD_CKE	J8	I/O	GPIO_B[0] / SDRAM clock control
GPIO_D[19]	FGPIO[12]	H12	I/O	GPIO_D[19] / Fast GPIO bit 12. Internal pull-up resistor is enabled at reset.
GPIO_D[18]	FGPIO[11]	D2	I/O	GPIO_D[18] / Fast GPIO bit 11. Internal pull-up resistor is enabled at reset.
GPIO_D[17]	FGPIO[10] / SCL	G2	I/O	GPIO_D[17] / Fast GPIO bit 10 / I2C SCL
GPIO_D[16]	FGPIO[9] / SDA	A9	I/O	GPIO_D[16] / Fast GPIO bit 9 / I2C SDA
GPIO_D[15]	FGPIO[8]	G1	I/O	GPIO_D[15] / Fast GPIO bit 8
				ADC Input Pins
ADIN_0		G10	AI	General purpose multi-channel ADC input 0
ADIN_2		F10	AI	General purpose multi-channel ADC input 2
ADIN_4		E10	AI	General purpose multi-channel ADC input 4
				Clock Pins
XIN		H8	I	Main Crystal Oscillator Input for PLL. 12MHz Crystal must be used if USB Boot Mode is required. Input voltage must not exceed VDD_OSC (1.95V max).
XOUT		G9	O	Main Crystal Oscillator Output for PLL
XFILT		G12	AO	PLL filter output
XTIN		K9	I	Sub Crystal Oscillator Input. 32.768kHz is recommended. Input voltage must not exceed VDD_OSC (1.95V max).
XTOUT		J10	O	Sub Crystal Oscillator Output
				JTAG Interface Pins
TDI		C11	I	JTAG serial data input for ARM940T
TMS		D11	I	JTAG test mode select for ARM940T
TCK		C10	I	JTAG test clock for ARM940T
TDO		D10	I/O	JTAG serial data output for ARM940T. External pull-up resistor is required to prevent floating during normal operation.
nTRST		B10	I	JTAG reset signal for ARM940T. Active low.
				Mode Control Pins
MODE1		B11	I	Mode Setting Input 1. Pull-down for normal operation.
PKG1		J7	I	Package ID1. Pull-up for normal operation.

Signal Name	Shared Signal	Ball	Type	Description – TCC763/ TCC764
nRESET		J12	I	System Reset. Active low.
				Power Pins
VDDIO		F5 L1 H9 D7	PWR	Digital Power for I/O (3.3V)
VDDIO_USB		M12	PWR	Power for USB I/O (3.3V)
VDD_NOR		A6	PWR	Digital Power for NOR Flash
VDD_OSC		M11	PWR	Digital Power for Oscillators (1.8V)
VDDI		C1 H3 J3 C8 C4	PWR	Digital Power for Internal Core (1.8V)
VDDI_ADC		D12	PWR	Digital Power for ADC (1.8V)
VDDA_ADC		F11	PWR	Analog Power for ADC (3.3V)
VDDA_PLL		H11	PWR	Analog & Digital Power for PLL (1.8V)
HPVDD		F12	PWR	Analog Power for Headphone Amp
VDDB_WF		M8	PWR	Digital Buffer Power for CODEC
VDDC_WF		M6	PWR	Core Power for CODEC
AVDD		A5	PWR	Analog Power for CODEC
VSSIO		A1 K1 K5 L12 B12	GND	Digital Ground for I/O
VSS_NOR		A11	GND	Digital Ground for NOR Flash
VSS_WF		M7	GND	Digital Ground for CODEC
VSSI		D1 J2 K7 C7 B4	GND	Digital Ground for Internal
VSSI_ADC		F9	GND	Digital ground for ADC
VSSA_ADC		C12	GND	Analog Ground for ADC
VSSA_PLL		G11	GND	Analog Ground for PLL
AGND		C5	GND	Analog Ground for CODEC

1.4.4 TCC766 Pin Description

Table 1.6 TCC766 Pin Description

Signal Name	Shared Signal	Ball	Type	Description – TCC766
				External Memory Interface Pins
SD_CKE	GPIO_B[0]	L9	I/O	SDRAM Clock Enable signal. Active high. / GPIO_B[0]
SD_CLK	GPO	P8	I/O	SDRAM Clock / GPO. SD_CLK can be used as a general purpose output. Refer to section "MEMORY CONTROLLER". (MCFG register Bit[3] and Bit[1])
SD_nCS	SD_nCLK / GPIO_B[1]	M8	I/O	Chip select signal for SDRAM, Active low / Inverted SD_CLK for DDR SDRAM / GPIO_B[1]
XA[21]	DQM[0]	L7	I/O	External Bus Address Bit [21] / Data I/O Mask 0
XA[20]	DQM[1]	N7	I/O	External Bus Address Bit [20] / Data I/O Mask 1
XA[19]	DQS[1]	L6	I/O	External Bus Address Bit [19] / DDR SDRAM Data Strobe [1]
XA[18]	DQS[0]	L5	I/O	External Bus Address Bit [18] / DDR SDRAM Data Strobe [0]
XA[17]		P7	I/O	External Bus Address Bit [17]
XA[16]	SD_nRAS	D5	I/O	External Bus Address Bit [16] / SDRAM RAS signal
XA[15]	SD_nCAS	N4	I/O	External Bus Address Bit [15] / SDRAM CAS signal
XA[14]	SD_BA[1]	N2	I/O	External Bus Address Bit [14] / SDRAM Bank Address 1
XA[13]	SD_BA[0]	N3	I/O	External Bus Address Bit [13] / SDRAM Bank Address 0.
XA[12]		N5	I/O	External Bus Address Bit [12]
XA[11]		M1	I/O	External Bus Address Bit [11]
XA[10]		M5	I/O	External Bus Address Bit [10]
XA[9]		M3	I/O	External Bus Address Bit [9]
XA[8]		L2	I/O	External Bus Address Bit [8]
XA[7]		L4	I/O	External Bus Address Bit [7]
XA[6]		K3	I/O	External Bus Address Bit [6]
XA[5]		J4	I/O	External Bus Address Bit [5]
XA[4]		P14	I/O	External Bus Address Bit [4]
XA[3]		J2	I/O	External Bus Address Bit [3]
XA[2]		J3	I/O	External Bus Address Bit [2]
XA[1]		J5	I/O	External Bus Address Bit [1]
XA[0]		H4	I/O	External Bus Address Bit [0]
XD[15]		H5	I/O	External Bus Data Bit [15]
XD[14]		L3	I/O	External Bus Data Bit [14]
XD[13]		F2	I/O	External Bus Data Bit [13]
XD[12]		E1	I/O	External Bus Data Bit [12]
XD[11]		E9	I/O	External Bus Data Bit [11]
XD[10]		F3	I/O	External Bus Data Bit [10]
XD[9]		D1	I/O	External Bus Data Bit [9]
XD[8]		A2	I/O	External Bus Data Bit [8]
XD[7]		B1	I/O	External Bus Data Bit [7]
XD[6]		F5	I/O	External Bus Data Bit [6]
XD[5]		C2	I/O	External Bus Data Bit [5]
XD[4]		D3	I/O	External Bus Data Bit [4]
XD[3]		G5	I/O	External Bus Data Bit [3]
XD[2]		F10	I/O	External Bus Data Bit [2]
XD[1]		H16	I/O	External Bus Data Bit [1]
XD[0]		F11	I/O	External Bus Data Bit [0]
nCS[3]	GPIO_B[5]	M9	I/O	External Bus Chip Select 3 / GPIO_B[5]. This pin should be connected to FCSN.
nCS[2]	GPIO_B[4] / TESTCS2	R7	I/O	External Bus Chip Select 2 / GPIO_B[4]. This pin has an internal connection to the USB2.0 module. Do not use for external components.
nCS[1]	GPIO_B[3]	R8	I/O	External Bus Chip Select 1 / GPIO_B[3]
nCS[0]	GPIO_B[2] / TESTCS0	P6	I/O	External Bus Chip Select 0 / GPIO_B[2]. This pin has an internal connection to the USB2.0 module. Do not use for external components.
nWE		N8	I/O	Static Memory Write Enable signal. Active low.
nOE		D12	I/O	Static Memory Output Enable signal. Active low.
READY		K13	I	Ready information from external device.
FCSN		C14	I	NOR Flash Chip Select. Should be connected to nCS[3].

Signal Name	Shared Signal	Ball	Type	Description – TCC766
				USB/UART/IrDA Interface Pins
USB_DP	GPIO_B[26]	P9	I/O	USB Function D+ signal / GPIO_B[26]
USB_DN	GPIO_B[27]	T8	I/O	USB Function D- signal / GPIO_B[27]
USBH_DP	GPIO_B[28]	R10	I/O	USB Host D+ signal / GPIO_B[28]
USBH_DN	GPIO_B[29]	N10	I/O	USB Host D- signal / GPIO_B[29]
UT_TX	GPIO_B[8] / SD_nCS	M11	I/O	UART or IrDA TX data / GPIO_B[8] / DDR SDRAM Chip Select
UT_RX	GPIO_B[9]	N11	I/O	UART or IrDA RX data / GPIO_B[9]
				Audio Interface Pins
BCLK	GPIO_B[21] / BM[0]	N12	I/O	I2S Bit Clock / GPIO_B[21] Internal pull-down resistor is active at power up.
LRCK	GPIO_B[22] / BM[1]	L14	I/O	I2S Word Clock / GPIO_B[22] Internal pull-down resistor is active at power up.
MCLK	GPIO_B[23]	N6	I/O	I2S System Clock
DAO	GPIO_B[24] / BM[2]	M14	I/O	I2S Digital Audio data Output
DAI	GPIO_B[25]	M13	I/O	I2S Digital Audio data Input / GPIO_B[25] must be connected externally to ADCDAT
ADCDAT		K14	O	I2S digital audio data output of audio CODEC(ADC) must be connected externally to GPIO_B[25] (DAI)
LCH_OUT		H15	AO	DAC Left Channel Output of audio CODEC
RCH_OUT		G15	AO	DAC Right Channel Output of audio CODEC
LOUT		C10	AO	DAC Left Channel Line Output of audio CODEC
ROUT		C8	AO	DAC Right Channel Line Output of audio CODEC
RCH_IN		F1	AI	ADC Right Channel Input of audio CODEC
MIC_IN		A3	AI	Microphone Input of audio CODEC
LCH_IN		G4	AI	ADC Left Channel Input of internal audio CODEC
VMID		A4	AO	Mid-rail reference decoupling point
MICBIAS		C6	AO	Microphone Bias
WMODE	CSB	H1	I	CODEC I/F Control. To enable 2-wire serial interface ot the internal CODEC, low level must be maintained. This pin has an internal pull-up resistor.
SDIN	GPIO_A[8] / BW[0]	E7	I	2-Wire MCU Data Input for CODEC
SCLK	GPIO_A[9] / BW[1]	B4	I	2-Wire MCU Clock Input for CODEC
				CD DSP Interface Pins
CBCLK	GPIO_A[1]	E11	I/O	CD Data Bit Clock Input / GPIO_A[1]
CLRCK	GPIO_A[2]	E10	I/O	CD Data Word Clock Input / GPIO_A[2]
CDAI	GPIO_A[3]	D9	I/O	CD Data Input / GPIO_A[3]
				External Interrupt Pins
EXINT[3]	GPIO_A[15]	D4	I/O	External Interrupt Request [3] / GPIO_A[15]
EXINT[2]	GPIO_A[14] / FGPIO[14]	A1	I/O	External Interrupt Request [2] / GPIO_A[14] / FGPIO[14]
EXINT[1]	GPIO_A[13] / FGPIO[13]	B2	I/O	External Interrupt Request [1] / GPIO_A[13] / FGPIO[13]
EXINT[0]	GPIO_A[12] / FGPIO[12]	E6	I/O	External Interrupt Request [0] / GPIO_A[12] / FGPIO[12]. This pin is internally connected to the USB2.0 module. Do not use for external component.
				General Purpose I/O Pins
GPIO_A[15]	EXINT[3]	D4	I/O	GPIO_A[15] / External Interrupt Request 3
GPIO_A[14]	EXINT[2] / FGPIO[14]	A1	I/O	GPIO_A[14] / External Interrupt Request 2 / Fast GPIO bit 14
GPIO_A[13]	EXINT[1] / FGPIO[13]	B2	I/O	GPIO_A[13] / External Interrupt Request 1 / Fast GPIO bit 13
GPIO_A[12]	TESTIRQ	E6	I/O	GPIO_A[12] / External Interrupt Request 0 / Fast GPIO bit 12. This pin is internally connected to the USB2.0 module. Do not use for external component.
GPIO_A[11]	SDI2 / FGPIO[11] / SCL	C7	I/O	GPIO_A[11] / GSIO2 Data In / Fast GPIO bit 11 / I2C Clock.
GPIO_A[10]	FRM2 / FGPIO[10] / SDA	F8	I/O	GPIO_A[10] / GSIO2 FRM / Fast GPIO bit 10 / I2C Data Line.
GPIO_A[9] / BW[1]	SCLK	B4	I/O	GPIO_A[9] / Bus Width bit 1. The status of BW[1:0] is latched at the rising edge of nRESET and used to determine external bus width. Refer to section "MEMORY CONTROLLER" for BW[1:0] description.

Signal Name	Shared Signal	Ball	Type	Description – TCC766
GPIO_A[8] / BW[0]	SDIN	E7	I/O	GPIO_A[8] / Bus Width bit 0. The status of BW[1:0] is latched at the rising edge of nRESET and used to determine external bus width. Refer to section "MEMORY CONTROLLER" for BW[1:0] description.
GPIO_A[7]	SDI1 / FGPIO[7]	B7	I/O	GPIO_A[7] / GSIO1 Data In / Fast GPIO bit 7
GPIO_A[6]	TESTRST	A7	I/O	GPIO_A[6] / Reset for the internal USB2.0 module. Pull-down for normal operation.
GPIO_A[5]	TESTUSB	F9	I/O	GPIO_A[5] / Mode Selection for the internal USB2.0 module. Pull-up for normal operation.
GPIO_A[4]	SDO1 / FGPIO[4]	B10	I/O	GPIO_A[4] / GSIO1 Data Output / Fast GPIO bit 4
GPIO_A[3]	SDI0 / CDAI / FGPIO[3]	D9	I/O	GPIO_A[3] / GSIO0 Data In / CD Interface Data / Fast GPIO bit 3. This pin has an internal pull-up resistor.
GPIO_A[2]	FRM0 / CLRCK / FGPIO[2]	E10	I/O	GPIO_A[2] / GSIO0 FRM / CD Interface LRCK / Fast GPIO bit 2 This pin has an internal pull-up resistor.
GPIO_A[1]	SCK0 / CBCLK / FGPIO[1]	E11	I/O	GPIO_A[1] / GSIO0 Clock / CD Interface BCLK / Fast GPIO bit 1 This pin has an internal pull-up resistor.
GPIO_A[0]	SDO0 / FGPIO[0]	M4	I/O	GPIO_A[0] / GSIO0 Data Out / FGPIO[0] This pin has an internal pull-up resistor.
GPIO_B[29]	USBH_DN	N10	I/O	GPIO_B[29] / USBH_DN
GPIO_B[28]	USBH_DP	R10	I/O	GPIO_B[28] / USBH_DP
GPIO_B[27]	USB_DN	T8	I/O	GPIO_B[27] / USB_DN
GPIO_B[26]	USB_DP	P9	I/O	GPIO_B[26] / USB_DP
GPIO_B[25]	DAI	M13	I/O	GPIO_B[25] / I2S Interface Data In. Should be connected externally to ADCDAT pin.
GPIO_B[24] / BM[2]	DAO	M14	I/O	GPIO_B[24] / Boot Mode bit 2 / I2S Interface Data Out. The status of BM[2:0] is latched at the rising edge of nRESET and used to determine the system boot mode. Refer to sections "BOOTING PROCEDURE" and "MEMORY CONTROLLER" for detailed description on BM[2:0]. Refer to "Functional Block Diagram" for more information about internal connectivity.
GPIO_B[23]	MCLK	N6	I/O	GPIO_B[23] / I2S Interface Master Clock. Refer to "Functional Block Diagram" for more information about internal connectivity.
GPIO_B[22] / BM[1]	LRCK	L14	I/O	GPIO_B[22] / Boot Mode bit 1 / I2S Interface LRCK. The status of BM[2:0] is latched at the rising edge of nRESET and used to determine the system boot mode. Refer to sections "BOOTING PROCEDURE" and "MEMORY CONTROLLER" for detailed description on BM[2:0]. Internal pull-down resistor is active at power up.
GPIO_B[21] / BM[0]	BCLK	N12	I/O	GPIO_B[21] / Boot Mode bit 0 / I2S Interface BCLK. The status of BM[2:0] is latched at the rising edge of nRESET and used to determine the system boot mode. Refer to sections "BOOTING PROCEDURE" and "MEMORY CONTROLLER" for detailed description on BM[2:0]. Internal pull-down resistor is active at power up.
GPIO_B[9]	UT_RX	N11	I/O	GPIO_B[9] / UART RX Signal
GPIO_B[8]	UT_TX / SD_nCS	M11	I/O	GPIO_B[8] / UART TX Signal / DDR SDRAM Chip Select
GPIO_B[7]		L10	I/O	GPIO_B[7]
GPIO_B[5]	nCS[3]	M9	I/O	GPIO_B[5] / External Chip Select 3. Should be connected externally to FCSN.
GPIO_B[4]	nCS[2] / TESTCS2	R7	I/O	GPIO_B[4] / External Chip Select 2. This pin has an internal connection to the USB2.0 module. Do not connect to external components.
GPIO_B[3]	nCS[1]	R8	I/O	GPIO_B[3] / External Chip Select 1
GPIO_B[2]	nCS[0] / TESTCS0	P6	I/O	GPIO_B[2] / External Chip Select 0. This pin has an internal connection to the USB2.0 module. Do not connect external components.
GPIO_B[1]	SD_nCS / SD_nCLK	M8	I/O	GPIO_B[1] / Chip select for SDRAM / Inverted Clock for DDR SDRAM.
GPIO_B[0]	SD_CKE	L9	I/O	GPIO_B[0] / SDRAM clock control
GPIO_D[17]	FGPIO[10] / SCL	B16	I/O	GPIO_D[17] / Fast GPIO bit 10 / I2C SCL

Signal Name	Shared Signal	Ball	Type	Description – TCC766
GPIO_D[16]	FGPIO[9] / SDA	C15	I/O	GPIO_D[16] / Fast GPIO bit 9 / I2C SDA
GPIO_D[15]	FGPIO[8]	D14	I/O	GPIO_D[15] / Fast GPIO bit 8
				ADC Input Pins
ADIN0		H12	AI	General purpose multi-channel ADC input 0
ADIN2		G13	AI	General purpose multi-channel ADC input 2
ADIN4		G14	AI	General purpose multi-channel ADC input 4
				Clock Pins
XIN		L16	I	Main Crystal Oscillator Input for PLL. Input voltage must not exceed VDD_OSC (1.95V max).
XOUT		K15	O	Main Crystal Oscillator Output for PLL
XFILT		J13	AO	PLL filter output
XTIN		L11	I	Sub Crystal Oscillator Input. 32.768kHz is recommended. Input voltage must not exceed VDD_OSC (1.95V max).
XTOUT		L12	O	Sub Crystal Oscillator Output
XSCI		A6	I	Crystal Oscillator Input for USB 2.0
XSCO		B5	O	Crystal Oscillator Output for USB 2.0
				JTAG Interface Pins
TDI		F12	I	JTAG serial data input for ARM940T
TMS		B13	I	JTAG test mode select for ARM940T
TCK		C12	I	JTAG test clock for ARM940T
TDO		A13	I/O	JTAG serial data output for ARM940T. External pull-up resistor is required to prevent floating during normal operation.
nTRST		D11	I	JTAG reset signal for ARM940T. Active low.
				Mode Control Pins
MODE1		D13	I	Mode Setting Input 1. Used for programming internal NOR flash. Pull-down for normal operation.
PKG		E13	I	Package ID, Pull-up for normal operation.
nRESET		L8	I	System Reset. Active low.
				USB 2.0 Interface Pins
DMRS		D2	I/O	USB 1.1 D- signal. Connect to external series resistor (39Ω±1%).
DPRS		C1	I/O	USB 1.1 D+ signal. Connect to external series resistor (39Ω±1%).
DM		B3	I/O	USB 2.0 D- signal.
DP		C4	I/O	USB 2.0 D+ signal.
RREF		C5	I	Connect external reference resistor (12.1kΩ±1%) to ground (VSS_U20).
RPU		E3	I	Connect external pull-up resistor(1.5kΩ±1%) to USB 2.0 analog power (VDDA_U20).
				MS & MSPRO Interface Pins
MS_CLK		P2	O	MS/MSPRO Serial protocol Clock signal.
MS_BS		P3	I/O	MS/MSPRO Serial protocol Bus State signal.
MS_D[3]		P1	I/O	MS/MSPRO Data Line [3]
MS_D[2]		P5	I/O	MS/MSPRO Data Line [2]
MS_D[1]		R5	I/O	MS/MSPRO Data Line [1]
MS_D[0]		R6	I/O	MS/MSPRO Data Line [0]
MS_CD		T5	I/O	MS/MSPRO Card Detection Input.
MS_PC		L1	I/O	MS/MSPRO Power Control signal with internal pull-up.
				MMC & SD Interface Pins
MMC_CLK		A16	O	MMC/SD Clock
MMC_CMD		A15	I/O	MMC/SD Command/Respond.
MMC_D[3]		C11	I/O	MMC/SD Data Line [3].
MMC_D[2]		B12	I/O	MMC/SD Data Line [2].
MMC_D[1]		A14	I/O	MMC/SD Data Line [1].
MMC_D[0]		B14	I/O	MMC/SD Data Line [0].
MMC_CD		T2	I/O	MMC/SD Card Detection Input.
MMC_PC		P4	I/O	MMC/SD Power Control signal with internal pull-up.

Signal Name	Shared Signal	Ball	Type	Description – TCC766
MST[2]		P10	I/O	Memory Card Configuration Select Bit 2 MST[2:0] / Configuration 111 – Record in flash memory by AP 001 – Only support MMC/SD card 010 – Only support MS/MS_Pro/New MS card 011 – Support two kinds of card above. And MMC/SD is the first slot in USB mode. 100 – Support two kinds of card above. And MS/MS_Pro/New MS card is the first slot in USB mode.
MST[1]		T9	I/O	Memory Card Configuration Select Bit 1
MST[0]		T10	I/O	Memory Card Configuration Select Bit 0
				Flash Memory Interface Pins
ND_D[15]		C16	I/O	Flash Data Bus Bit 15
ND_D[14]		D15	I/O	Flash Data Bus Bit 14
ND_D[13]		D16	I/O	Flash Data Bus Bit 13
ND_D[12]		E16	I/O	Flash Data Bus Bit 12
ND_D[11]		E15	I/O	Flash Data Bus Bit 11
ND_D[10]		F15	I/O	Flash Data Bus Bit 10
ND_D[9]		F14	I/O	Flash Data Bus Bit 9
ND_D[8]		F16	I/O	Flash Data Bus Bit 8
ND_D[7]		T16	I/O	Flash Data Bus Bit 7
ND_D[6]		P15	I/O	Flash Data Bus Bit 6
ND_D[5]		R15	I/O	Flash Data Bus Bit 5
ND_D[4]		T14	I/O	Flash Data Bus Bit 4
ND_D[3]		R14	I/O	Flash Data Bus Bit 3
ND_D[2]		T15	I/O	Flash Data Bus Bit 2
ND_D[1]		R13	I/O	Flash Data Bus Bit 1
ND_D[0]		P13	I/O	Flash Data Bus Bit 0
ND_nCE[1]		R3	I/O	Flash Chip Enable 1, Low active.
ND_nCE[0]		R2	I/O	Flash Chip Enable 0, Low active.
ND_ALE		R11	O	Flash Address Latch Enable, High active.
ND_CLE		R12	O	Flash Command Latch Enable, High active.
ND_nOE		P11	O	Flash Read Control signal, Low active.
ND_nWE		T11	O	Flash Write Control signal, Low active.
ND_nWP		P12	I/O	Flash Write Protect Control signal, Low active.
ND_RDY		T12	I	Flash Ready/Busy signal. Pull-up resistor required.
ND_WP_CTL		A12	I/O	Flash Write Protect Control Enable Input. ND_nWP signal output is enabled when this signal is high.
PRTST		K1	I/O	NAND Flash low level format control signal with internal pull-up. Pull-up for normal operation (low level format disabled).
AGN_nRESET		M15	I/O	Active low reset signal to AGAND Flash.
				Miscellaneous Pins
ACT_nSPND		M16	I/O	Power Control Status Output. High indicates power on state (Access Mode), low indicates power off state (Suspend Mode).
ACS_IND		N1	I/O	Flash Memory Access Indicator with internal pull-up. This signal will be blinking when Flash Memory is accessed.
U_CF		J16	I	Internal IDE Mode Select Signal. For normal operation, connect this signal to GPIO_A[5].
U_nRESET		B15	I	Reset Signal
U_nEA		L15	I	EAMODE Select for Test. Pull-up for normal operation.
U_nTEST		C13	I	Test Mode. (active low). Pull-up for normal operation.
TESTCS2	GPIO_B[4]	R7	I/O	Chip Select 2 for the internal IDE interface. This signal is internally connected to GPIO_B[4]. Do not connect to external component.
TESTCS0	GPIO_B[2]	P6	I/O	Chip Select 1 for the internal IDE interface. This signal is internally connected to GPIO_B[2]. Do not connect to external component.

Signal Name	Shared Signal	Ball	Type	Description – TCC766
TESTIRQ	GPIO_A[12]	E6	I/O	Active high Interrupt Request. This pin is internally connected to the USB2.0 module. Pull-down for normal operation.
TESTRST	GPIO_A[6]	A7	I/O	Active low hardware reset for the internal USB2.0 module. Pull-down for normal operation.
TESTUSB	GPIO_A[5]	F9	I/O	IDE / USB Mode Selection signal. Pull-up for normal operation. (1: IDE Mode, 0:USB Mode)
TESTIO7	GPIO_A[3]	D9	I/O	Reserved for Chip Test. Internal pull-up active.
TESTIO6	GPIO_A[2]	E10	I/O	Reserved for Chip Test. Internal pull-up active.
TESTIO5	GPIO_A[1]	E11	I/O	Reserved for Chip Test. Internal pull-up active.
TESTIO4	GPIO_A[0]	M4	I/O	Reserved for Chip Test. Internal pull-up active.
TEST_MWP		T7	I/O	Reserved for Chip Test. Pull-up for normal operation.
TEST_AG		A9	I/O	Reserved for Chip Test. Pull-down for normal operation.
TEST_SP		A10	I/O	Reserved for Chip Test. Pull-down for normal operation.
TESTEASL		A11	I	Reserved for Chip Test. Pull-down for normal operation.
TESTHOE		T4	I/O	Reserved for Chip Test. Pull-down for normal operation.
TESTHWE		R9	I/O	R eserved for Chip Test. Pull-up for normal operation.
TESTREG		J12	I/O	R eserved for Chip Test. Pull-up for normal operation.
TESTPACK		B9	I/O	Reserved for Chip Test.
TESTIS16		B11	I/O	Reserved for Chip Test.
TESTCE4		N16	I/O	Reserved for Chip Test.
TESTCE3		T1	I/O	Reserved for Chip Test.
TESTCE2		T3	I/O	Reserved for Chip Test.
TESTFAL		N14	O	Reserved for Chip Test.
TESTFCL		N15	O	Reserved for Chip Test.
TESTFRD		R16	O	Reserved for Chip Test.
TESTFWE		P16	O	Reserved for Chip Test.
				Power Pins
VDDIO		E8	PWR	Digital Power for I/O (3.3V)
VDDIO		H3	PWR	Digital Power for I/O (3.3V)
VDDIO		M6	PWR	Digital Power for I/O (3.3V)
VDDIO		K16	PWR	Digital Power for I/O (3.3V)
VDDIO_USB		M12	PWR	Power for USB I/O (3.3V)
VDD_NOR		F6	PWR	Digital Power for NOR Flash. (3.3V)
VDD_OSC		L13	PWR	Digital Power for Oscillators (1.8V)
VDDI		G12	PWR	Digital Power for Internal Core (1.8V)
VDDI		F7	PWR	Digital Power for Internal Core (1.8V)
VDDI		M7	PWR	Digital Power for Internal Core (1.8V)
VDDI		E4	PWR	Digital Power for Internal Core (1.8V)
VDDI		C9	PWR	Digital Power for Internal Core (1.8V)
VDDI		K2	PWR	Digital Power for Internal Core (1.8V)
VDDA_ADC		H13	PWR	Analog Power for ADC (3.3V)
VDDA_PLL		K12	PWR	Analog & Digital Power for PLL (1.8V)
HPVDD		J15	PWR	Analog Power for Headphone Amp
VDDB_CDC		T6	PWR	Digital Buffer Power for CODEC
VDDC_CDC		R4	PWR	Core Power for CODEC
AVDD		A5	PWR	Analog Power for CODEC
VSSIO		E12	GND	Digital Ground for I/O
VSSIO		N13	GND	Digital Ground for I/O
VSSIO		E5	GND	Digital Ground for I/O
VSSIO		M2	GND	Digital Ground for I/O
VSSIO		K5	GND	Digital Ground for I/O
VSS_NOR		C3	GND	Digital Ground for NOR Flash
VSS_CDC		R1	GND	Digital Ground for CODEC
VSSI		D7	GND	Digital Ground for Internal
VSSI		D8	GND	Digital Ground for Internal
VSSI		F4	GND	Digital Ground for Internal
VSSI		F13	GND	Digital Ground for Internal
VSSI		M10	GND	Digital Ground for Internal
VSSI		K4	GND	Digital Ground for Internal
VSSA_ADC		G16	GND	Analog Ground for ADC
VSSA_PLL		H14	GND	Analog Ground for PLL

Signal Name	Shared Signal	Ball	Type	Description – TCC766
AGND		B8	GND	Analog Ground for CODEC
				Power Pins for USB 2.0
VDDA_U20		G1	PWR	3.3V Analog Power for USB 2.0
VDDA_U20		B6	PWR	3.3V for USB 2.0
VDDA_U20		G3	PWR	3.3V for USB 2.0
VDD_U20		E14	PWR	3.3V for USB 2.0
VDD_U20		N9	PWR	3.3V for USB 2.0
VDDI_U20		A8	PWR	2.5V Power for Internal. Connect to VO25.
VO25		J1	PWRO	2.5V Output. Connect to VDDI_U20.
VSSA_U20		E2	GND	Ground for USB 2.0
VSSA_U20		D6	GND	Ground for USB 2.0
VSSA_U20		G2	GND	Ground for USB 2.0
VSS_U20		J14	GND	Ground for USB 2.0
VSS_U20		D10	GND	Ground for USB 2.0
VSS_U20		H2	GND	Ground for USB 2.0
VSS_U20		T13	GND	Ground for USB 2.0

1.4.5 TCC767 Pin Description

Table 1.7 TCC767 Pin Description

Signal Name	Shared Signal	Ball	Type	Description – TCC767
				External Memory Interface Pins
SD_CKE	GPIO_B[0]	M10	I/O	SDRAM Clock Enable signal. Active high. / GPIO_B[0]
SD_CLK	GPO	N2	I/O	SDRAM Clock / GPO. SD_CLK can be used as a general purpose output. Refer to section "MEMORY CONTROLLER". (MCFG register Bit[3] and Bit[1])
SD_nCS	SD_nCLK / GPIO_B[1]	P2	I/O	Chip select signal for SDRAM, Active low / Inverted SD_CLK for DDR SDRAM / GPIO_B[1]
XA[21]	DQM[0]	L6	I/O	External Bus Address Bit [21] / Data I/O Mask 0
XA[20]	DQM[1]	P3	I/O	External Bus Address Bit [20] / Data I/O Mask 1
XA[19]	DQS[1]	M6	I/O	External Bus Address Bit [19] / DDR SDRAM Data Strobe [1]
XA[18]	DQS[0]	L7	I/O	External Bus Address Bit [18] / DDR SDRAM Data Strobe [0]
XA[17]		P10	I/O	External Bus Address Bit [17]
XA[16]	SD_nRAS	G5	I/O	External Bus Address Bit [16] / SDRAM RAS signal
XA[15]	SD_nCAS	N3	I/O	External Bus Address Bit [15] / SDRAM CAS signal
XA[14]	SD_BA[1]	M5	I/O	External Bus Address Bit [14] / SDRAM Bank Address 1
XA[13]	SD_BA[0]	M4	I/O	External Bus Address Bit [13] / SDRAM Bank Address 0.
XA[12]		K4	I/O	External Bus Address Bit [12]
XA[11]		L1	I/O	External Bus Address Bit [11]
XA[10]		H1	I/O	External Bus Address Bit [10]
XA[9]		K6	I/O	External Bus Address Bit [9]
XA[8]		K7	I/O	External Bus Address Bit [8]
XA[7]		H2	I/O	External Bus Address Bit [7]
XA[6]		G1	I/O	External Bus Address Bit [6]
XA[5]		H4	I/O	External Bus Address Bit [5]
XA[4]		G2	I/O	External Bus Address Bit [4]
XA[3]		J7	I/O	External Bus Address Bit [3]
XA[2]		J9	I/O	External Bus Address Bit [2]
XA[1]		H9	I/O	External Bus Address Bit [1]
XA[0]		G9	I/O	External Bus Address Bit [0]
XD[15]		H6	I/O	External Bus Data Bit [15]
XD[14]		H5	I/O	External Bus Data Bit [14]
XD[13]		J6	I/O	External Bus Data Bit [13]
XD[12]		H7	I/O	External Bus Data Bit [12]
XD[11]		H8	I/O	External Bus Data Bit [11]
XD[10]		G8	I/O	External Bus Data Bit [10]
XD[9]		H10	I/O	External Bus Data Bit [9]
XD[8]		F9	I/O	External Bus Data Bit [8]
XD[7]		E5	I/O	External Bus Data Bit [7]
XD[6]		G6	I/O	External Bus Data Bit [6]
XD[5]		G7	I/O	External Bus Data Bit [5]
XD[4]		F7	I/O	External Bus Data Bit [4]
XD[3]		E6	I/O	External Bus Data Bit [3]
XD[2]		D9	I/O	External Bus Data Bit [2]
XD[1]		E11	I/O	External Bus Data Bit [1]
XD[0]		E10	I/O	External Bus Data Bit [0]
nCS[3]	GPIO_B[5]	M7	I/O	External Bus Chip Select 3 / GPIO_B[5]
nCS[2]	GPIO_B[4]	R2	I/O	External Bus Chip Select 2 / GPIO_B[4]
nCS[1]	GPIO_B[3]	M3	I/O	External Bus Chip Select 1 / GPIO_B[3]
nCS[0]	GPIO_B[2]	N1	I/O	External Bus Chip Select 0 / GPIO_B[2]
nWE		J8	I/O	Static Memory Write Enable signal. Active low.
nOE		K10	I/O	Static Memory Output Enable signal. Active low.
READY		J15	I	Ready information from external device.
FCSN		D12	I	NOR Flash Chip Select. Should be connected to nCS[3].
				USB/UART/IrDA Interface Pins
USB_DP	GPIO_B[26]	P8	I/O	USB Function D+ signal / GPIO_B[26]
USB_DN	GPIO_B[27]	M9	I/O	USB Function D- signal / GPIO_B[27]
USBH_DP	GPIO_B[28]	R8	I/O	USB Host D+ signal / GPIO_B[28]

Signal Name	Shared Signal	Ball	Type	Description – TCC767
USBH_DN	GPIO_B[29]	K9	I/O	USB Host D- signal / GPIO_B[29]
UT_TX	GPIO_B[8] / SD_nCS	L11	I/O	UART or IrDA TX data / GPIO_B[8] / DDR SDRAM Chip Select
UT_RX	GPIO_B[9]	L10	I/O	UART or IrDA RX data / GPIO_B[9]
				Audio Interface Pins
BCLK	GPIO_B[21] / BM[0]	M11	I/O	I2S Bit Clock / GPIO_B[21] / Boot Mode Bit 0
LRCK	GPIO_B[22] / BM[1]	N12	I/O	I2S Word Clock / GPIO_B[22] / Boot Mode Bit 1
MCLK	GPIO_B[23]	M13	I/O	I2S System Clock / GPIO_B[23]
DAO	GPIO_B[24] / BM[2]	N14	I/O	I2S Digital Audio data Output / GPIO_B[24] / Boot Mode Bit 2
DAI	GPIO_B[25]	N15	I/O	I2S Digital Audio data Input / GPIO_B[25]
				CD DSP Interface Pins
CBCLK	GPIO_A[1]	A7	I/O	CD Data Bit Clock Input / GPIO_A[1]
CLRCK	GPIO_A[2]	A6	I/O	CD Data Word Clock Input / GPIO_A[2]
CDAI	GPIO_A[3]	C7	I/O	CD Data Input / GPIO_A[3]
				External Interrupt Pins
EXINT[3]	GPIO_A[15]	E4	I/O	External Interrupt Request [3] / GPIO_A[15]
EXINT[2]	GPIO_A[14] / FGPIO[14]	E3	I/O	External Interrupt Request [2] / GPIO_A[14] / FGPIO[14]
EXINT[1]	GPIO_A[13] / FGPIO[13]	D3	I/O	External Interrupt Request [1] / GPIO_A[13] / FGPIO[13]
EXINT[0]	GPIO_A[12] / FGPIO[12]	B3	I/O	External Interrupt Request [0] / GPIO_A[12] / FGPIO[12]
				General Purpose I/O Pins
GPIO_A[15]	EXINT[3]	E4	I/O	GPIO_A[15] / External Interrupt Request 3
GPIO_A[14]	EXINT[2] / FGPIO[14]	E3	I/O	GPIO_A[14] / External Interrupt Request 2 / Fast GPIO bit 14
GPIO_A[13]	EXINT[1] / FGPIO[13]	D3	I/O	GPIO_A[13] / External Interrupt Request 1 / Fast GPIO bit 13
GPIO_A[12]	EXINT[0] / FGPIO[12]	B3	I/O	GPIO_A[12] / External Interrupt Request 0 / Fast GPIO bit 12
GPIO_A[11]	SDI2 / FGPIO[11] / SCL	E7	I/O	GPIO_A[11] / GSIO2 Data In / Fast GPIO bit 11 / I2C Clock.
GPIO_A[10]	FRM2 / FGPIO[10] / SDA	B1	I/O	GPIO_A[10] / GSIO2 FRM / Fast GPIO bit 10 / I2C Data Line.
GPIO_A[9] / BW[1]	SCK2 / FGPIO[9] / SCL	D7	I/O	GPIO_A[9] / Bus Width bit 1 / GSIO2 Clock / Fast GPIO bit 9 / I2C Clock. The status of BW[1:0] is latched at the rising edge of nRESET and used to determine external bus width. Refer to section "MEMORY CONTROLLER" for BW[1:0] description.
GPIO_A[8] / BW[0]	SDO2 / FGPIO[8] / SDA	A1	I/O	GPIO_A[8] / Bus Width bit 0 / GSIO2 Data Out / Fast GPIO bits 8 / I2C Data Line. The status of BW[1:0] is latched at the rising edge of nRESET and used to determine external bus width. Refer to section "MEMORY CONTROLLER" for BW[1:0] description.
GPIO_A[7]	SDI1 / FGPIO[7]	D5	I/O	GPIO_A[7] / GSIO1 Data In / Fast GPIO bit 7
GPIO_A[6]	FRM1 / FGPIO[6]	C5	I/O	GPIO_A[6] / GSIO1 FRM / Fast GPIO bit 6
GPIO_A[5]	SCK1 / FGPIO[5]	C8	I/O	GPIO_A[5] / GSIO1 Clock / Fast GPIO bit 5
GPIO_A[4]	SDO1 / FGPIO[4]	B7	I/O	GPIO_A[4] / GSIO1 Data Output / Fast GPIO bit 4
GPIO_A[3]	SDI0 / CDAI / FGPIO[3]	C7	I/O	GPIO_A[3] / GSIO0 Data In / CD Interface Data / Fast GPIO bit 3
GPIO_A[2]	FRM0 / CLRCK / FGPIO[2]	A6	I/O	GPIO_A[2] / GSIO0 FRM / CD Interface LRCK / Fast GPIO bit 2
GPIO_A[1]	SCK0 / CBCLK / FGPIO[1]	A7	I/O	GPIO_A[1] / GSIO0 Clock / CD Interface BCLK / Fast GPIO bit 1
GPIO_A[0]	SDO0 / FGPIO[0]	B6	I/O	GPIO_A[0] / GSIO0 Data Out / FGPIO[0]
GPIO_B[29]	USBH_DN	K9	I/O	GPIO_B[29] / USBH_DN
GPIO_B[28]	USBH_DP	R8	I/O	GPIO_B[28] / USBH_DP
GPIO_B[27]	USB_DN	M9	I/O	GPIO_B[27] / USB_DN
GPIO_B[26]	USB_DP	P8	I/O	GPIO_B[26] / USB_DP
GPIO_B[25]	DAI	N15	I/O	GPIO_B[25] / I2S Interface Data In.
GPIO_B[24] / BM[2]	DAO	N14	I/O	GPIO_B[24] / Boot Mode bit 2 / I2S Interface Data Out. The status of BM[2:0] is latched at the rising edge of nRESET and used to determine the system boot mode. Refer to sections "BOOTING PROCEDURE" and "MEMORY CONTROLLER" for detailed description on BM[2:0].
GPIO_B[23]	MCLK	M13	I/O	GPIO_B[23] / I2S Interface Master Clock.
GPIO_B[22] / BM[1]	LRCK	N12	I/O	GPIO_B[22] / Boot Mode bit 1 / I2S Interface LRCK. The status of BM[2:0] is latched at the rising edge of nRESET and used to determine the system boot mode. Refer to sections "BOOTING PROCEDURE" and "MEMORY CONTROLLER" for detailed description on BM[2:0].

Signal Name	Shared Signal	Ball	Type	Description – TCC767
GPIO_B[21] / BM[0]	BCLK	M11	I/O	GPIO_B[21] / Boot Mode bit 0 / I2S Interface BCLK. The status of BM[2:0] is latched at the rising edge of nRESET and used to determine the system boot mode. Refer to sections "BOOTING PROCEDURE" and "MEMORY CONTROLLER" for detailed description on BM[2:0].
GPIO_B[9]	UT_RX	L10	I/O	GPIO_B[9] / UART RX Signal
GPIO_B[8]	UT_TX / SD_nCS	L11	I/O	GPIO_B[8] / UART TX Signal / DDR SDRAM Chip Select
GPIO_B[7]		N11	I/O	GPIO_B[7]
GPIO_B[5]	nCS[3]	M7	I/O	GPIO_B[5] / External Chip Select 3
GPIO_B[4]	nCS[2]	R2	I/O	GPIO_B[4] / External Chip Select 2
GPIO_B[3]	nCS[1]	M3	I/O	GPIO_B[3] / External Chip Select 1
GPIO_B[2]	nCS[0]	N1	I/O	GPIO_B[2] / External Chip Select 0
GPIO_B[1]	SD_nCS / SD_nCLK	P2	I/O	GPIO_B[1] / Chip select for SDRAM / Inverted Clock for DDR SDRAM.
GPIO_B[0]	SD_CKE	M10	I/O	GPIO_B[0] / SDRAM clock control
GPIO_D[17]	FGPIO[10] / SCL	E12	I/O	GPIO_D[17] / Fast GPIO bit 10 / I2C SCL
GPIO_D[16]	FGPIO[9] / SDA	C14	I/O	GPIO_D[16] / Fast GPIO bit 9 / I2C SDA
GPIO_D[15]	FGPIO[8]	B15	I/O	GPIO_D[15] / Fast GPIO bit 8
				ADC Input Pins
ADIN0		F14	AI	General purpose multi-channel ADC input 0
ADIN2		G13	AI	General purpose multi-channel ADC input 2
ADIN4		E15	AI	General purpose multi-channel ADC input 4
				Clock Pins
XIN		K12	I	Main Crystal Oscillator Input for PLL. Input voltage must not exceed VDD_OSC (1.95V max).
XOUT		K11	O	Main Crystal Oscillator Output for PLL
XFILT		G14	AO	PLL filter output
XTIN		L13	I	Sub Crystal Oscillator Input. 32.768kHz is recommended. Input voltage must not exceed VDD_OSC (1.95V max).
XTOUT		M14	O	Sub Crystal Oscillator Output
XSCI		C2	I	Crystal Oscillator Input for USB 2.0
XSCO		B2	O	Crystal Oscillator Output for USB 2.0
				JTAG Interface Pins
TDI		D11	I	JTAG serial data input for ARM940T
TMS		C10	I	JTAG test mode select for ARM940T
TCK		B11	I	JTAG test clock for ARM940T
TDO		A12	I/O	JTAG serial data output for ARM940T. External pull-up resistor is required to prevent floating during normal operation.
nTRST		D10	I	JTAG reset signal for ARM940T. Active low.
				Mode Control Pins
MODE1		C13	I	Mode Setting Input 1. Used for programming internal NOR flash. Pull-down for normal operation.
PKG		F11	I	Package ID. Pull-up for normal operation.
nRESET		J11	I	System Reset. Active low.
				USB 2.0 Interface Pins
DMRS		E2	I/O	USB 1.1 D- signal. Connect to external series resistor (39Ω±1%).
DPRS		F4	I/O	USB 1.1 D+ signal. Connect to external series resistor (39Ω±1%).
DM		C3	I/O	USB 2.0 D- signal.
DP		C1	I/O	USB 2.0 D+ signal.
RREF		B4	I	Connect external reference resistor (12.1kΩ±1%) to ground (VSS_U20).
RPU		D1	I	Connect external pull-up resistor(1.5kΩ±1%) to USB 2.0 analog power (VDDA_U20).
				MS & MSPRO Interface Pins
MS_CLK		L2	O	MS/MSPRO Serial protocol Clock signal.
MS_BS		M2	I/O	MS/MSPRO Serial protocol Bus State signal.
MS_D[3]		M1	I/O	MS/MSPRO Data Line [3]
MS_D[2]		L3	I/O	MS/MSPRO Data Line [2]

Signal Name	Shared Signal	Ball	Type	Description – TCC767
MS_D[1]		R1	I/O	MS/MSPRO Data Line [1]
MS_D[0]		P4	I/O	MS/MSPRO Data Line [0]
MS_CD		P7	I	MS/MSPRO Card Detection Input.
MS_PC		K3	O	MS/MSPRO Power Control.
				MMC & SD Interface Pins
MMC_CLK		B13	O	MMC/SD Clock
MMC_CMD		A14	I/O	MMC/SD Command/Respond.
MMC_D[3]		A11	I/O	MMC/SD Data Line [3].
MMC_D[2]		B10	I/O	MMC/SD Data Line [2].
MMC_D[1]		A13	I/O	MMC/SD Data Line [1].
MMC_D[0]		B12	I/O	MMC/SD Data Line [0].
MMC_CD		R5	I	MMC/SD Card Detection Input.
MMC_PC		J4	O	MMC/SD Power Control.
MST[2]		R6	I	Memory Card Configuration Select Bit 2 MST: 111 – Record in flash memory by AP 001 – Only support MMC/SD card 010 – Only support MS/MS_Pro/New MS card 011 – Support two kinds of card above. And MMC/SD is the first slot in USB mode. 100 – Support two kinds of card above. And MS/MS_Pro/New MS card is the first slot in USB mode.
MST[1]		R7	I	Memory Card Configuration Select Bit 1
MST[0]		N9	I	Memory Card Configuration Select Bit 0
				Flash Memory Interface Pins
ND_D[15]		A15	I/O	Flash Data Bus Bit 15
ND_D[14]		B14	I/O	Flash Data Bus Bit 14
ND_D[13]		E13	I/O	Flash Data Bus Bit 13
ND_D[12]		D14	I/O	Flash Data Bus Bit 12
ND_D[11]		C15	I/O	Flash Data Bus Bit 11
ND_D[10]		F13	I/O	Flash Data Bus Bit 10
ND_D[9]		D15	I/O	Flash Data Bus Bit 9
ND_D[8]		E14	I/O	Flash Data Bus Bit 8
ND_D[7]		P15	I/O	Flash Data Bus Bit 7
ND_D[6]		N13	I/O	Flash Data Bus Bit 6
ND_D[5]		M12	I/O	Flash Data Bus Bit 5
ND_D[4]		R15	I/O	Flash Data Bus Bit 4
ND_D[3]		R14	I/O	Flash Data Bus Bit 3
ND_D[2]		P13	I/O	Flash Data Bus Bit 2
ND_D[1]		R13	I/O	Flash Data Bus Bit 1
ND_D[0]		P12	I/O	Flash Data Bus Bit 0
ND_nCE[1]		P6	O	Flash Chip Enable 1, Low active.
ND_nCE[0]		R3	O	Flash Chip Enable 0, Low active.
ND_ALE		R10	O	Flash Address Latch Enable, High active.
ND_CLE		N10	O	Flash Command Latch Enable, High active.
ND_nOE		R9	O	Flash Read Control signal, Low active.
ND_nWE		P9	O	Flash Write Control signal, Low active.
ND_nWP		R12	O	Flash Write Protect Control signal, Low active.
ND_RDY		R11	I	Flash Ready/Busy signal. Pull-up resistor required.
ND_WP_CTL		A10	I	Flash Write Protect Control Enable. ND_nWP signal output is enabled when this signal is high.
PRTST		K2	I	NAND Flash low level format control. Pull-up for normal operation (low level format disabled).
AGN_nRESET		H15	O	Active low reset signal to AGAND Flash.
				Miscellaneous Pins
ACT_nSPND		J13	O	Power Control Status Output. High indicates power on state (Access Mode), low indicates power off state (Suspend Mode).
ACS_IND		N4	O	Flash Memory Access Indicator. This signal will be blinking when Flash Memory is accessed.

Signal Name	Shared Signal	Ball	Type	Description – TCC767
IIDE_INTRQ		A3	O	Active high Interrupt Request. This pin should be connected to one of EXINT[3:0]/GPIO_A[15:12] pins.
IIDE_nRESET		B8	I	Active low hardware reset.
IIDE_nCS3		P5	I	Chip Select 3 for the internal IDE interface. This signal should be connected to one of nCS[2:0]/GPIO_B[4:2].
IIDE_nCS1		P1	I	Chip Select 1 for the internal IDE interface. This signal should be connected to one of nCS[2:0]/GPIO_B[4:2].
IIDE_nUSB		J14	I	IDE / USB Mode Selection signal. 1: IDE Mode, 0: USB Mode.
U_CF		G15	I	Internal IDE Mode Select Signal. For normal operation, connect this signal to IIDE_nUSB described above.
U_nRESET		C11	I	Reset Signal
U_nEA		H14	I	EAMODE Select for Test. Pull-up for normal operation.
U_nTEST		C12	I	Test Mode. (active low). Pull-up for normal operation.
TEST_MWP		N8	I	Reserved for Chip Test. Pull-up for normal operation.
TEST_AG		C4	I	Reserved for Chip Test. Pull-down for normal operation.
TEST_SP		A4	I/O	Reserved for Chip Test. Pull-down for normal operation.
TESTEASL		C9	I	Reserved for Chip Test. Pull-down for normal operation.
TESTHOE		N7	I/O	Reserved for Chip Test. Pull-down for normal operation.
TESTHWE		R4	I/O	R eserved for Chip Test. Pull-up for normal operation.
TESTREG		J10	I/O	R eserved for Chip Test. Pull-up for normal operation.
TESTPACK		A8	I/O	Reserved for Chip Test.
TESTIS16		A9	I/O	Reserved for Chip Test.
TESTIO7		J3	I/O	Reserved for Chip Test.
TESTIO6		J2	I/O	Reserved for Chip Test.
TESTIO5		J1	I/O	Reserved for Chip Test.
TESTIO4		K1	I/O	Reserved for Chip Test.
TESTCE4		K13	I/O	Reserved for Chip Test.
TESTCE3		M8	I/O	Reserved for Chip Test.
TESTCE2		L8	I/O	Reserved for Chip Test.
TESTFAL		L14	O	Reserved for Chip Test.
TESTFCL		K15	O	Reserved for Chip Test.
TESTFRD		M15	O	Reserved for Chip Test.
TESTFWE		L15	O	Reserved for Chip Test.
				Power Pins
VDDIO		F1	PWR	Digital Power for I/O (3.3V)
VDDIO		L5	PWR	Digital Power for I/O (3.3V)
VDDIO		J12	PWR	Digital Power for I/O (3.3V)
VDDIO		D8	PWR	Digital Power for I/O (3.3V)
VDDIO_USB		P14	PWR	Power for USB I/O (3.3V)
VDD_NOR		A2	PWR	Digital Power for NOR Flash (3.3V)
VDD_OSC		K14	PWR	Digital Power for Oscillators (1.8V)
VDDI		F5	PWR	Digital Power for Internal Core (1.8V)
VDDI		H3	PWR	Digital Power for Internal Core (1.8V)
VDDI		N5	PWR	Digital Power for Internal Core (1.8V)
VDDI		G10	PWR	Digital Power for Internal Core (1.8V)
VDDI		E8	PWR	Digital Power for Internal Core (1.8V)
VDDI		D6	PWR	Digital Power for Internal Core (1.8V)
VDDA_ADC		G11	PWR	Analog Power for ADC (3.3V)
VDDA_PLL		H12	PWR	Analog & Digital Power for PLL (1.8V)
VSSIO		D4	GND	Digital Ground for I/O
VSSIO		L4	GND	Digital Ground for I/O
VSSIO		N6	GND	Digital Ground for I/O
VSSIO		L12	GND	Digital Ground for I/O
VSSIO		D13	GND	Digital Ground for I/O
VSS_NOR		E9	GND	Digital Ground for NOR Flash
VSSI		F3	GND	Digital Ground for Internal
VSSI		K5	GND	Digital Ground for Internal
VSSI		L9	GND	Digital Ground for Internal
VSSI		F12	GND	Digital Ground for Internal
VSSI		F8	GND	Digital Ground for Internal
VSSI		F6	GND	Digital Ground for Internal

Signal Name	Shared Signal	Ball	Type	Description – TCC767
VSSA_ADC		G12	GND	Analog Ground for ADC
VSSA_PLL		H11	GND	Analog Ground for PLL
				Power Pins for USB 2.0
VDDA_U20		J5	PWR	3.3V Analog Power for USB 2.0
VDDA_U20		E1	PWR	3.3V for USB 2.0
VDDA_U20		C6	PWR	3.3V for USB 2.0
VDD_U20		K8	PWR	3.3V for USB 2.0
VDD_U20		F10	PWR	3.3V for USB 2.0
VDDI_U20		B5	PWR	2.5V Power for Internal. Connect to VO25.
VDDI_U20		H13	PWR	2.5V Power for Internal. Connect to VO25.
VO25		G3	PWRO	2.5V Output. Connect to VDDI_U20.
VSSA_U20		D2	GND	Ground for USB 2.0
VSSA_U20		F2	GND	Ground for USB 2.0
VSSA_U20		A5	GND	Ground for USB 2.0
VSS_U20		F15	GND	Ground for USB 2.0
VSS_U20		B9	GND	Ground for USB 2.0
VSS_U20		G4	GND	Ground for USB 2.0
VSS_U20		P11	GND	Ground for USB 2.0

1.4.6 TCC768 Pin Description

Table 1.8 TCC768 Pin Description

Signal Name	Shared Signal	Ball	Type	Description – TCC768
				External Memory Interface Pins
SD_CKE	GPIO_B[0]	J8	I/O	SDRAM Clock Enable signal. Active high. / GPIO_B[0]
SD_CLK	GPO	L5	I/O	SDRAM Clock / GPO. SD_CLK can be used as a general purpose output. Refer to section "MEMORY CONTROLLER". (MCFG register Bit[3] and Bit[1])
SD_nCS	GPIO_B[1]	L6	I/O	Chip select signal for SDRAM, Active low / GPIO_B[1]
XA[21]	DQM[0]	L4	I/O	External Bus Address Bit [21] / Data I/O Mask 0
XA[20]	DQM[1]	K4	I/O	External Bus Address Bit [20] / Data I/O Mask 1
XA[19]		K3	I/O	External Bus Address Bit [19]
XA[18]		L2	I/O	External Bus Address Bit [18]
XA[17]	ND_CLE	L3	I/O	External Bus Address Bit [17] / CLE for NAND Flash
XA[16]	SD_nRAS / ND_ALE	G3	I/O	External Bus Address Bit [16] / SDRAM RAS signal / ALE for NAND Flash
XA[15]	SD_nCAS	M3	I/O	External Bus Address Bit [15] / SDRAM CAS signal
XA[14]	SD_BA[1]	M2	I/O	External Bus Address Bit [14] / SDRAM Bank Address 1
XA[13]	SD_BA[0]	M1	I/O	External Bus Address Bit [13] / SDRAM Bank Address 0.
XA[12]		J4	I/O	External Bus Address Bit [12]
XA[11]		K2	I/O	External Bus Address Bit [11]
XA[10]		M4	I/O	External Bus Address Bit [10]
XA[9]		J1	I/O	External Bus Address Bit [9]
XA[8]		H4	I/O	External Bus Address Bit [8]
XA[7]		H5	I/O	External Bus Address Bit [7]
XA[6]		H1	I/O	External Bus Address Bit [6]
XA[5]		G6	I/O	External Bus Address Bit [5]
XA[4]		H2	I/O	External Bus Address Bit [4]
XA[3]		G5	I/O	External Bus Address Bit [3]
XA[2]		G4	I/O	External Bus Address Bit [2]
XA[1]		G7	I/O	External Bus Address Bit [1]
XA[0]		G8	I/O	External Bus Address Bit [0]
XD[15]		A3	I/O	External Bus Data Bit [15]
XD[14]		F4	I/O	External Bus Data Bit [14]
XD[13]		E2	I/O	External Bus Data Bit [13]
XD[12]		E5	I/O	External Bus Data Bit [12]
XD[11]		D8	I/O	External Bus Data Bit [11]
XD[10]		F7	I/O	External Bus Data Bit [10]
XD[9]		E1	I/O	External Bus Data Bit [9]
XD[8]		F6	I/O	External Bus Data Bit [8]
XD[7]		E3	I/O	External Bus Data Bit [7]
XD[6]		D4	I/O	External Bus Data Bit [6]
XD[5]		C2	I/O	External Bus Data Bit [5]
XD[4]		B1	I/O	External Bus Data Bit [4]
XD[3]		A7	I/O	External Bus Data Bit [3]
XD[2]		B2	I/O	External Bus Data Bit [2]
XD[1]		A10	I/O	External Bus Data Bit [1]
XD[0]		F8	I/O	External Bus Data Bit [0]
NCS[3]	ND_nOE[3] / GPIO_B[5]	H6	I/O	External Bus Chip Select [3] / NAND Flash Output Enable [3] / GPIO_B[5]. This pin should be connected to FCSN.
NCS[2]	ND_nOE[2] / GPIO_B[4]	J6	I/O	External Bus Chip Select [2] / NAND Flash Output Enable [2] / GPIO_B[4]
NCS[1]	ND_nOE[1] / GPIO_B[3]	K6	I/O	External Bus Chip Select [1] / NAND Flash Output Enable [1] / GPIO_B[3]
NCS[0]	ND_nOE[0] / GPIO_B[2]	J5	I/O	External Bus Chip Select [0] / NAND Flash Output Enable [1] / GPIO_B[2]
ND_nWE	GPIO_B[7]	L10	I/O	NAND flash WE. Active low. / GPIO_B[7]
nWE		M5	I/O	Static Memory Write Enable signal. Active low.
nOE		H7	I/O	Static Memory Output Enable signal. Active low.
READY		J11	I	Ready information from external device.

Signal Name	Shared Signal	Ball	Type	Description – TCC768
FCSN		A12	I	NOR Flash Chip Select. Should be connected to nCS[3].
				USB/UART/IrDA Interface Pins
USB_DP	GPIO_B[26]	L7	I/O	USB Function D+ signal / GPIO_B[26]
USB_DN	GPIO_B[27]	K8	I/O	USB Function D- signal / GPIO_B[27]
USBH_DP	GPIO_B[28]	L8	I/O	USB Host D+ signal / GPIO_B[28]
USBH_DN	GPIO_B[29]	M9	I/O	USB Host D- signal / GPIO_B[29]
UT_TX	GPIO_B[8]	M10	I/O	UART or IrDA TX data / GPIO_B[8]
UT_RX	GPIO_B[9] / IDE_nCS1	L9	I/O	UART or IrDA RX data / GPIO_B[9] / IDE Chip Select 1
				Audio Interface Pins
BCLK	GPIO_B[21] / BM[0]	J9	I/O	I2S Bit Clock / GPIO_B[21] / Boot Mode Bit 0. Internal pull-down resistor is active at power up.
LRCK	GPIO_B[22] / BM[1]	L11	I/O	I2S Word Clock / GPIO_B[22] / Boot Mode Bit 1 Internal pull-down resistor is active at power up.
MCLK	GPIO_B[23]	K12	I/O	I2S System Clock / GPIO_B[23]
DAO	GPIO_B[24] / BM[2]	K11	I/O	I2S Digital Audio data Output / GPIO_B[24] / Boot Mode Bit 2
DAI	GPIO_B[25]	K10	I/O	I2S Digital Audio data Input / GPIO_B[25]
ADCDAT		H10	O	I2S Digital Audio data Output of audio CODEC(ADC). Must be connected externally to GPIO_B25 (DAI)
LCH_OUT		E11	AO	DAC Left Channel Output of audio CODEC
RCH_OUT		E12	AO	DAC Right Channel Output of audio CODEC
RCH_IN		F1	AI	ADC Right Channel Input of audio CODEC
MIC_IN		A4	AI	Microphone Input of audio CODEC
LCH_IN		F2	AI	ADC Left Channel Input of internal audio CODEC
VMID		B5	AO	Mid-rail reference decoupling point
MICBIAS		D5	AO	Microphone Bias
WMODE	CSB	F3	I	CODEC I/F Control. Pull-down for normal operation. Internal pull-up resistor is active at power up.
SDIN	GPIO_A[8] / BW[0]	D6	I/O	2-Wire MCU Data Input for CODEC
SCLK	GPIO_A[9] / BW[1]	E7	I/O	2-Wire MCU Clock Input for CODEC
				CD DSP Interface Pins
CBCLK	GPIO_A[1]	D9	I/O	CD Data Bit Clock Input / GPIO_A[1]
CLRCK	GPIO_A[2]	E9	I/O	CD Data Word Clock Input / GPIO_A[2]
CDAI	GPIO_A[3]	E8	I/O	CD Data Input / GPIO_A[3]
				External Interrupt Pins
EXINT[3]	GPIO_A15	A2	I/O	External Interrupt Request [3] / GPIO_A[15]
EXINT[2]	GPIO_A[14] / FGPIO[14]	D3	I/O	External Interrupt Request [2] / GPIO_A[14] / FGPIO[14]
EXINT[1]	GPIO_A[13] / FGPIO[13]	B3	I/O	External Interrupt Request [1] / GPIO_A[13] / FGPIO[13]
EXINT[0]	GPIO_A[12] / FGPIO[12]	C3	I/O	External Interrupt Request [0] / GPIO_A[12] / FGPIO[12]
				General Purpose I/O Pins
GPIO_A[15]	EXINT[3]	A2	I/O	GPIO_A[15] / External Interrupt Request 3
GPIO_A[14]	EXINT[2] / FGPIO[14]	D3	I/O	GPIO_A[14] / External Interrupt 2 / Fast GPIO bit 14
GPIO_A[13]	EXINT[1] / FGPIO[13]	B3	I/O	GPIO_A[13] / External Interrupt 1 / Fast GPIO bit 13
GPIO_A[12]	EXINT[0] / FGPIO[12]	C3	I/O	GPIO_A[12] / External Interrupt 0 / Fast GPIO bit 12
GPIO_A[11]	SDI2 / FGPIO[11] / SCL	E4	I/O	GPIO_A[11] / GSIO2 Data In / Fast GPIO bit 11 / I2C Clock.
GPIO_A[10]	FRM2 / FGPIO[10] / SDA	E6	I/O	GPIO_A[10] / GSIO2 FRM / Fast GPIO bit 10 / I2C Data Line.
GPIO_A[9] / BW[1]	SCK2 / FGPIO[9] / SCL	E7	I/O	GPIO_A[9] / Bus Width bit 1. The status of BW[1:0] is latched at the rising edge of nRESET and used to determine external bus width.
GPIO_A[8] / BW[0]	SDO2 / FGPIO[8] / SDA	D6	I/O	GPIO_A[8] / Bus Width bit 0. The status of BW[1:0] is latched at the rising edge of nRESET and used to determine external bus width.
GPIO_A[7]	SDI1 / FGPIO[7]	B6	I/O	GPIO_A[7] / GSIO1 Data In / Fast GPIO bit 7
GPIO_A[6]	FRM1 / FGPIO[6]	C6	I/O	GPIO_A[6] / GSIO1 FRM / Fast GPIO bit 6
GPIO_A[5]	SCK1 / FGPIO[5]	B7	I/O	GPIO_A[5] / GSIO1 Clock / Fast GPIO bit 5
GPIO_A[4]	SDO1 / FGPIO[4]	B8	I/O	GPIO_A[4] / GSIO1 Data Out / Fast GPIO bit 4
GPIO_A[3]	SDI0 / CDAI / FGPIO[3]	E8	I/O	GPIO_A[3] / GSIO0 Data In / CD Interface Data / Fast GPIO bit 3.
GPIO_A[2]	FRM0 / CLRCK / FGPIO[2]	E9	I/O	GPIO_A[2] / GSIO0 FRM / CD Interface LRCK / Fast GPIO bit 2
GPIO_A[1]	SCK0 / CBCLK / FGPIO[1]	D9	I/O	GPIO_A[1] / GSIO0 Clock / CD Interface BCLK / Fast GPIO bit 1
GPIO_A[0]	SDO0 / FGPIO[0]	C9	I/O	GPIO_A[0] / GSIO0 Data Out / FGPIO[0]
GPIO_B[29]	USBH_DN	M9	I/O	GPIO_B[29] / USBH_DN
GPIO_B[28]	USBH_DP	L8	I/O	GPIO_B[28] / USBH_DP
GPIO_B[27]	USB_DN	K8	I/O	GPIO_B[27] / USB_DN

Signal Name	Shared Signal	Ball	Type	Description – TCC768
GPIO_B[26]	USB_DP	L7	I/O	GPIO_B[26] / USB_DP
GPIO_B[25]	DAI	K10	I/O	GPIO_B[25] / I2S Interface Data In. Should be connected externally to ADCDAT pin.
GPIO_B[24] / BM[2]	DAO	K11	I/O	GPIO_B[24] / Boot Mode bit 2 / I2S Interface Data Out. The status of BM[2:0] is latched at the rising edge of nRESET and used to determine the system boot mode.
GPIO_B[23]	MCLK	K12	I/O	GPIO_B[23] / I2S Interface Master Clock.
GPIO_B[22] / BM[1]	LRCK	L11	I/O	GPIO_B[22] / Boot Mode bit 1 / I2S Interface LRCK. The status of BM[2:0] is latched at the rising edge of nRESET and used to determine the system boot mode. Internal pull-down resistor is active at power up.
GPIO_B[21] / BM[0]	BCLK	J9	I/O	GPIO_B[21] / Boot Mode bit 0 / I2S Interface BCLK. The status of BM[2:0] is latched at the rising edge of nRESET and used to determine the system boot mode. Internal pull-down resistor is active at power up.
GPIO_B[9]	UT_RX	L9	I/O	GPIO_B[9] / UART RX Signal
GPIO_B[8]	UT_TX	M10	I/O	GPIO_B[8] / UART TX Signal
GPIO_B[7]	ND_nWE	L10	I/O	GPIO_B[7] / Write Enable for NAND Flash
GPIO_B[5]	nCS[3]	H6	I/O	GPIO_B[5] / External Chip Select 3
GPIO_B[4]	nCS[2]	J6	I/O	GPIO_B[4] / External Chip Select 2
GPIO_B[3]	nCS[1]	K6	I/O	GPIO_B[3] / External Chip Select 1
GPIO_B[2]	nCS[0]	J5	I/O	GPIO_B[2] / External Chip Select 0
GPIO_B[1]	SD_nCS	L6	I/O	GPIO_B[1] / Chip select for SDRAM
GPIO_B[0]	SD_CKE	J8	I/O	GPIO_B[0] / SDRAM clock control
GPIO_D[17]	FGPIO[10] / SCL	G2	I/O	GPIO_D[17] / Fast GPIO bit 10 / I2C SCL
GPIO_D[16]	FGPIO[9] / SDA	A9	I/O	GPIO_D[16] / Fast GPIO bit 9 / I2C SDA
GPIO_D[15]	FGPIO[8]	G1	I/O	GPIO_D[15] / Fast GPIO bit 8
				ADC Input Pins
ADIN_0		G10	AI	General purpose multi-channel ADC input 0
ADIN_2		F10	AI	General purpose multi-channel ADC input 2
ADIN_4		E10	AI	General purpose multi-channel ADC input 4
				Clock Pins
XIN		H8	I	Main Crystal Oscillator Input for PLL. 12MHz Crystal must be used if USB Boot Mode is required. Input voltage must not exceed VDD_OSC (1.95V max).
XOUT		G9	O	Main Crystal Oscillator Output for PLL
XFILT		G12	AO	PLL filter output. 350pF(±10%) capacitor is required.
XTIN		K9	I	Sub Crystal Oscillator Input. 32.768kHz is recommended. Input voltage must not exceed VDD_OSC (1.95V max).
XTOUT		J10	O	Sub Crystal Oscillator Output
				JTAG Interface Pins
TDI		C11	I	JTAG serial data input. External pull-up resistor is required.
TMS		D11	I	JTAG test mode select. External pull-up resistor is required.
TCK		C10	I	JTAG test clock. External pull-up resistor is required.
TDO		D10	I/O	JTAG serial data output. External pull-up resistor is required.
nTRST		B10	I	JTAG reset signal. Active low.
				Mode Control Pins
MODE1		B11	I	Mode Setting Input 1. Pull-down for normal operation.
PKG1		J7	I	Package ID1. Pull-up for normal operation.
nRESET		J12	I	System Reset. Active low.
				Power Pins
VDDIO		F5	PWR	Digital Power for I/O (3.3V)
VDDIO		L1	PWR	Digital Power for I/O (3.3V)
VDDIO		H9	PWR	Digital Power for I/O (3.3V)
VDDIO		D7	PWR	Digital Power for I/O (3.3V)
VDDIO		A8	PWR	Digital Power for I/O (3.3V)
VDDIO		D2	PWR	Digital Power for I/O (3.3V)
VDDIO		A6	PWR	Digital Power for I/O (3.3V)
VDDIO_USB		M12	PWR	Power for USB I/O (3.3V)
VDD_OSC		M11	PWR	Digital Power for Oscillators (1.8V)

Signal Name	Shared Signal	Ball	Type	Description – TCC768
VDDI		C1	PWR	Digital Power for Internal Core (1.8V)
VDDI		H3	PWR	Digital Power for Internal Core (1.8V)
VDDI		J3	PWR	Digital Power for Internal Core (1.8V)
VDDI		C8	PWR	Digital Power for Internal Core (1.8V)
VDDI		C4	PWR	Digital Power for Internal Core (1.8V)
VDDI		D12	PWR	Digital Power for Internal Core (1.8V)
VDDA_ADC		F11	PWR	Analog Power for ADC (3.3V)
VDDA_PLL		H11	PWR	Analog & Digital Power for PLL (1.8V)
HPVDD		F12	PWR	Analog Power for Headphone Amp
VDDB_CDC		M8	PWR	Digital Buffer Power for CODEC
VDDC_CDC		M6	PWR	Core Power for CODEC
AVDD		A5	PWR	Analog Power for CODEC
VSSIO		A1	GND	Digital Ground for I/O
VSSIO		K1	GND	Digital Ground for I/O
VSSIO		K5	GND	Digital Ground for I/O
VSSIO		L12	GND	Digital Ground for I/O
VSSIO		B12	GND	Digital Ground for I/O
VSSIO		H12	GND	Digital Ground for I/O
VSSIO		B9	GND	Digital Ground for I/O
VSSIO		A11	GND	Digital Ground for I/O
VSS_CDC		M7	GND	Digital Ground for CODEC
VSSI		D1	GND	Digital Ground for Internal
VSSI		J2	GND	Digital Ground for Internal
VSSI		K7	GND	Digital Ground for Internal
VSSI		C7	GND	Digital Ground for Internal
VSSI		B4	GND	Digital Ground for Internal
VSSI		F9	GND	Digital Ground for Internal
VSSA_ADC		C12	GND	Analog Ground for ADC
VSSA_PLL		G11	GND	Analog Ground for PLL
AGND		C5	GND	Analog Ground for CODEC

Table 1.9 Pin Comparison – TCC763 vs. TCC768

Ball #	TCC763 Rev. 1	TCC768	Note
D2	GPIO_D18	VDDIO	Power for I/O and Memory
H12	GPIO_D19	VSSIO	Ground for I/O and Memory
A8	ROUT	VDDIO	Power for I/O and Memory
B9	LOUT	VSSIO	Ground for I/O and Memory
A6	VDD_NOR	VDDIO	Power for I/O and Memory
A11	VSS_NOR	VSSIO	Ground for I/O and Memory
D12	VDDI_ADC	VDDI	Core power. (1.8V)
F9	VSSI_ADC	VSSI	Core ground.

1.5 Package

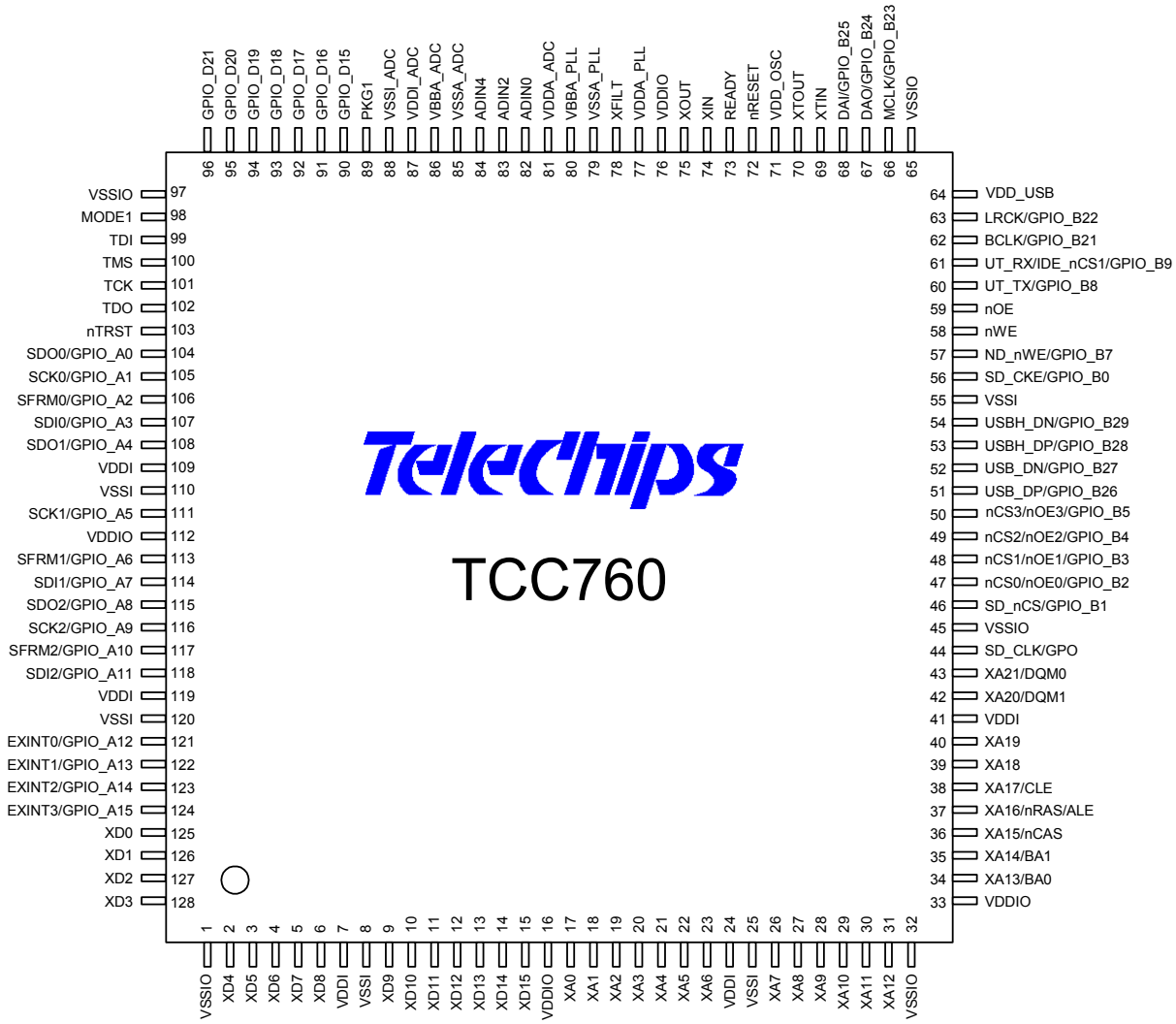


Figure 1.8 TCC760 Package Diagram (128-TQFP-1414 / Top View)

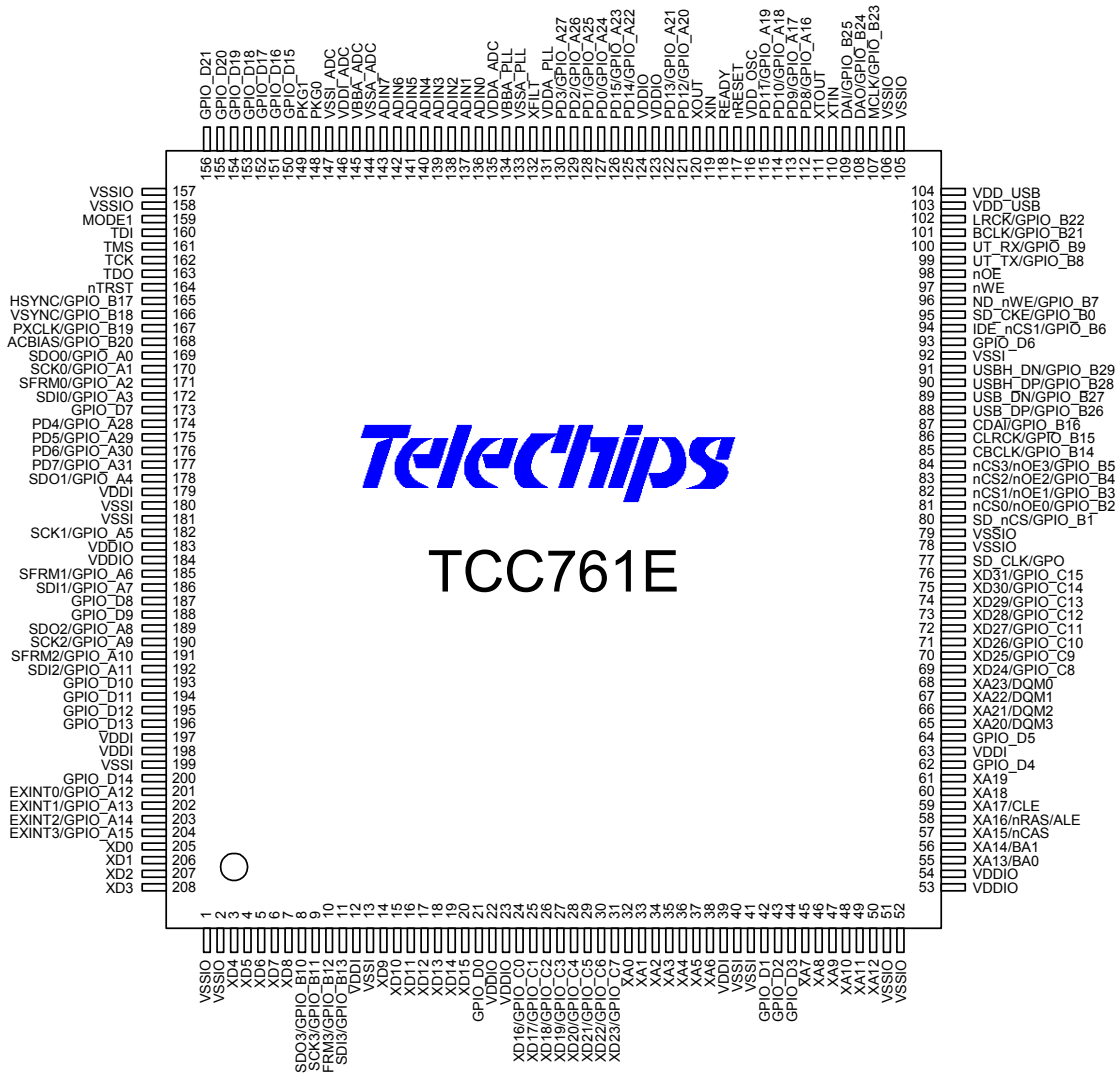


Figure 1.9 TCC761-E Package Diagram (208-LQFP-2828 / Top View)

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	
1	VSSIO	XD5	XD6	GPIO_B11	VSSI	XD12	GPIO_D0	XD17	XD21	XA1	XA5	VSSI	GPIO_D3	XA7	XA10	XA11	VDDIO	1
2	XD0	XD3	VSSIO	XD7	GPIO_B12	XD9	XD13	VDDIO	XD18	XD22	XA2	XA6	GPIO_D1	XA8	XA12	VSSIO	XA14	2
3	GPIO_A15	XD1	XD2	XD8	GPIO_B13	XD10	XD14	VDDIO	XD19	XD23	XA3	VDDI	GPIO_D2	XA9	VSSIO	VDDIO	XA15	3
4	GPIO_A12	GPIO_A13	GPIO_A14	XD4	GPIO_B10	VDDI	XD11	XD15	XD16	XD20	XA0	XA4	VSSI	XA13	XA17	XA16	XA19	4
5	GPIO_D14	VDDI	VSSI	GPIO_D13										XA18	VDDI	GPIO_D4	XA20	5
6	VDDI	GPIO_D11	GPIO_D12	GPIO_A11										GPIO_D5	XA22	XA21	XD24	6
7	GPIO_D10	GPIO_A9	GPIO_A10	GPIO_D9										XA23	XD26	XD25	XD28	7
8	GPIO_A8	GPIO_A7	GPIO_D8	VDDIO										XD27	XD30	XD29	SD_CLK	8
9	GPIO_A6	GPIO_A5	VDDIO	VSSI										XD31	VSSIO	VSSIO	GPIO_B2	9
10	VSSI	GPIO_A4	VDDI	GPIO_A30										GPIO_B1	GPIO_B4	GPIO_B3	GPIO_B14	10
11	GPIO_A31	GPIO_A28	GPIO_A29	GPIO_A3										GPIO_B5	GPIO_B16	GPIO_B15	USB_DN	11
12	GPIO_D7	GPIO_A1	GPIO_A2	GPIO_B20										USB_DP	USBH_DN	USBH_DP	GPIO_D6	12
13	GPIO_A0	GPIO_B18	GPIO_B19	nTRST										VSSI	GPIO_B0	GPIO_B6	GPIO_B7	13
14	GPIO_B17	TCK	TDO	MODE1	VSSA_ADC	ADIN_4	ADIN_0	XFILT	GPIO_A25	VDDIO	XOUT	VDDI	GPIO_A16	GPIO_B23	GPIO_B8	nOE	nWE	14
15	TMS	VSSIO	GPIO_D20	GPIO_D16	VSSI_ADC	ADIN_7	ADIN_3	VDDA_ADC	VDDA_PLL	GPIO_A24	VDDIO	XIN	GPIO_A19	XTOUT	VDD_USB	GPIO_B22	GPIO_B9	15
16	TDI	GPIO_D21	GPIO_D19	GPIO_D15	VDDI_ADC	ADIN_6	ADIN_2	VBBA_PLL	GPIO_A27	GPIO_A23	GPIO_A21	MODE0	GPIO_A18	XTIN	VSSIO	VDD_USB	GPIO_B21	16
17	VSSIO	GPIO_D18	GPIO_D17	PKG1	PKG0	VBBA_ADC	ADIN_5	ADIN_1	VSSA_PLL	GPIO_A26	GPIO_A22	GPIO_A20	nRESET	GPIO_A17	GPIO_B25	GPIO_B24	VSSIO	17
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	

Figure 1.10 TCC761-Y Package Diagram (208-TBGA-1515 / Bottom View)

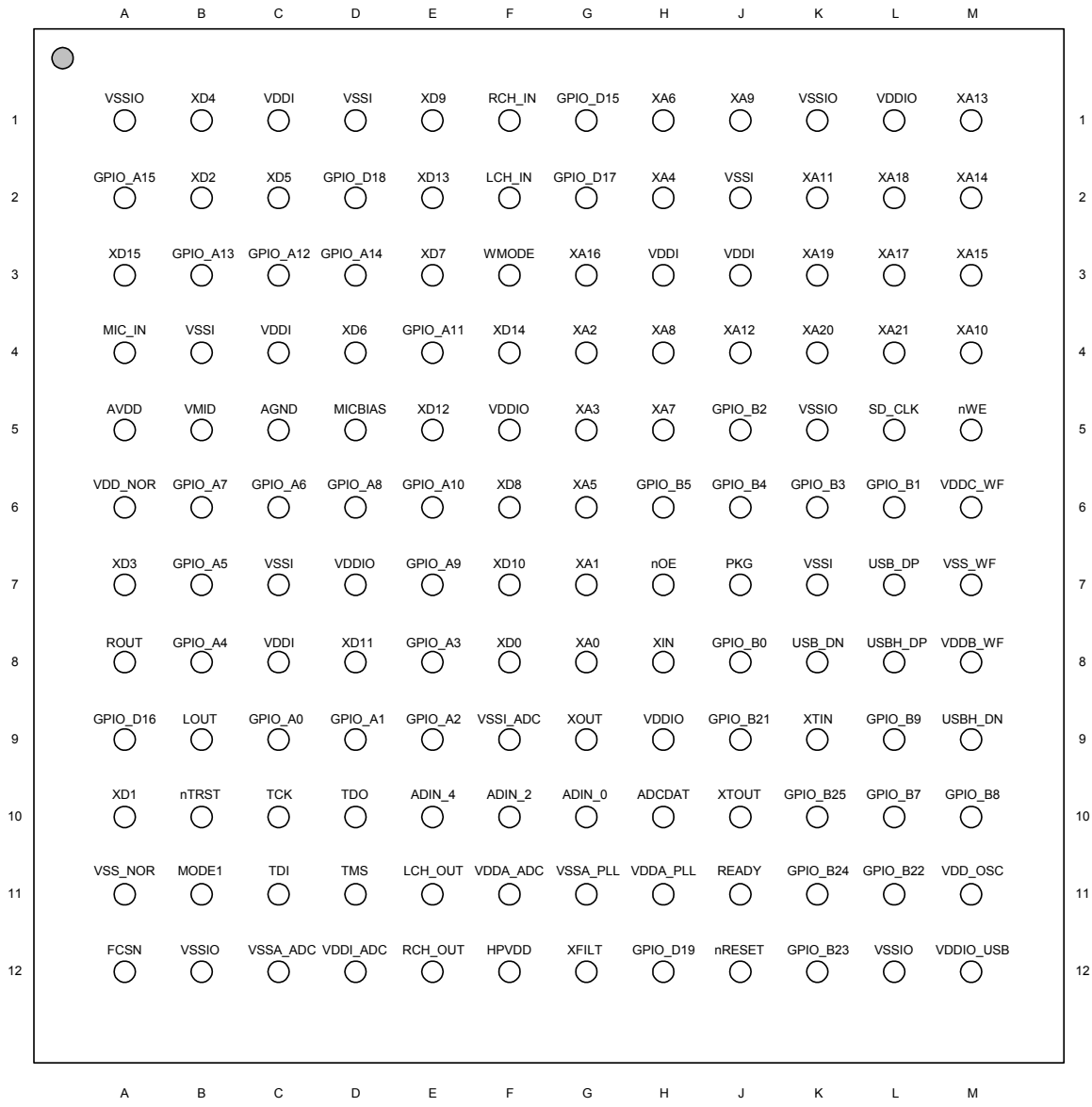


Figure 1.11 TCC763/TCC764 Package Diagram (144-BGA-1010 / Bottom View)

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	
1	GPIO_A[14] EXINT[2] FGPIO[14]	XD[7]	DPRS	XD[9]	XD[12]	RCH_IN	VDDA_U20	WMODE	VO25	PRTST	MS_PC	XA[11]	ACS_IND	MS_D[3]	VSS_CDC	TESTCE3	1
2	XD[8]	GPIO_A[13] EXINT[1] FGPIO[13]	XD[5]	DMRS	VSSA_U20	XD[13]	VSSA_U20	VSS_U20	XA[3]	VDDI	XA[8]	VSSIO	XA[14] SD_BA[1]	MS_CLK	ND_nCE[0]	MMC_CD	2
3	MIC_IN	DM	VSS_NOR	XD[4]	RPU	XD[10]	VDDA_U20	VDDIO	XA[2]	XA[6]	XD[14]	XA[9]	XA[13] SD_BA[0]	MS_BS	ND_nCE[1]	TESTCE2	3
4	VMID	GPIO_A[9] BW[1] SCLK	DP	GPIO_A[15] EXINT[3]	VDDI	VSSI	LCH_IN	XA[0]	XA[5]	VSSI	XA[7]	GPIO_A[0] SDO0 FGPIO[0] TESTIO4	XA[15] SD_nCAS	MMC_PC	VDDC_CDC	TESTHOE	4
5	AVDD	XSCO	RREF	XA[16] SD_nRAS	VSSIO	XD[6]	XD[3]	XD[15]	XA[1]	VSSIO	XA[18] DQS[0]	XA[10]	XA[12]	MS_D[2]	MS_D[1]	MS_CD	5
6	XSCI	VDDA_U20	MICBIAS	VSSA_U20	GPIO_A[12] EXTINT[0] FGPIO[12] TESTIRQ	VDD_NOR					XA[19] DQS[1]	VDDIO	GPIO_B[23] MCLK	GPIO_B[2] nCS[0] TESTCS0	MS_D[0]	VDDB_CDC	6
7	GPIO_A[6] TESTRST	GPIO_A[7] SDI1 FGPIO[7]	GPIO_A[11] SDI2 FGPIO[11] SCL	VSSI	GPIO_A[8] BW[0] SDIN	VDDI					XA[21] DQM[0]	VDDI	XA[20] DQM[1]	XA[17]	GPIO_B[4] nCS[2] TESTCS2	TEST_MWP	7
8	VDDI_U20	AGND	ROUT	VSSI	VDDIO	GPIO_A[10] FRM2 FGPIO[10] SDA					nRESET	GPIO_B[1] SD_nCS SD_nCLK	nWE	SD_CLK GPO	GPIO_B[3] nCS[1]	USB_DN GPIO_B[27]	8
9	TEST_AG	TESTPACK	VDDI	GPIO_A[3] SDI0 CDAI FGPIO[3] TESTIO7	XD[11]	GPIO_A[5] TESTUSB					GPIO_B[0] SD_CKE	GPIO_B[5] nCS[3]	VDD_U20	USB_DP GPIO_B[26]	TESTHWE	MST[1]	9
10	TEST_SP	GPIO_A[4] SDO1 FGPIO[4]	LOUT	VSS_U20	GPIO_A[2] FRM0 CLRCK FGPIO[2] TESTIO6	XD[2]					GPIO_B[7]	VSSI	USBH_DN GPIO_B[29]	MST[2]	USBH_DP GPIO_B[28]	MST[0]	10
11	TESTEASL	TESTIS16	MMC_D[3]	nTRST	GPIO_A[1] SCK0 CBCLK FGPIO[1] TESTIO5	XD[0]					XTIN	GPIO_B[8] UT_TX SD_nCS	GPIO_B[9] UT_RX	ND_nOE	ND_ALE	ND_nWE	11
12	ND_WP_CTL	MMC_D[2]	TCK	nOE	VSSIO	TDI	VDDI	ADIN0	TESTREG	VDDA_PLL	XTOUT	VDDIO_USB	GPIO_B[21] BM[0] BCLK	ND_nWP	ND_CLE	ND_RDY	12
13	TDO	TMS	U_nTEST	MODE1	PKG	VSSI	ADIN2	VDDA_ADC	XFILT	READY	VDD_OSC	GPIO_B[25] DAI	VSSIO	ND_D[0]	ND_D[1]	VSS_U20	13
14	MMC_D[1]	MMC_D[0]	FCSN	GPIO_D[15] FGPIO[8]	VDD_U20	ND_D[9]	ADIN4	VSSA_PLL	VSS_U20	ADCDAT	GPIO_B[22] BM[1] LRCK	GPIO_B[24] BM[2] DAO	TESTFAL	XA[4]	ND_D[3]	ND_D[4]	14
15	MMC_CMD	U_nRESET	GPIO_D[16] FGPIO[9] SDA	ND_D[14]	ND_D[11]	ND_D[10]	RCH_OUT	LCH_OUT	HPVDD	XOUT	U_nEA	AGN_nRESET	TESTFCL	ND_D[6]	ND_D[5]	ND_D[2]	15
16	MMC_CLK	GPIO_D[17] FGPIO[10] SCL	ND_D[15]	ND_D[13]	ND_D[12]	ND_D[8]	VSSA_ADC	XD[1]	U_CF	VDDIO	XIN	ACT_nSPND	TESTCE4	TESTFWE	TESTFRD	ND_D[7]	16
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	

Figure 1.12 TCC766 Package Diagram (232-FPBGA-1414 / Bottom View)

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	
1	GPIO_A[8] BW[0] SDO2	GPIO_A[10] FRM2 SDA	DP	RPU	VDDA_U20	VDDIO	XA[6]	XA[10]	TESTIO5	TESTIO4	XA[11]	MS_D[3]	nCS[0] GPIO_B[2]	IIDE_nCS1	MS_D[1]	1
2	VDD_NOR	XSCO	XSCI	VSSA_U20	DMRS	VSSA_U20	XA[4]	XA[7]	TESTIO6	PRTST	MS_CLK	MS_BS	SD_CLK GPO	SD_nCS SD_nCLK GPIO_B[1]	nCS[2] GPIO_B[4]	2
3	IIDE_INTRQ	GPIO_A[12] EXINT[0]	DM	GPIO_A[13] EXINT[1]	GPIO_A[14] EXINT[2]	VSSI	VO25	VDDI	TESTIO7	MS_PC	MS_D[2]	nCS[1] GPIO_B[3]	XA[15] SD_nCAS	XA[20] DQM[1]	ND_nCE[0]	3
4	TEST_SP	RREF	TEST_AG	VSSIO	GPIO_A[15] EXINT[3]	DPRS	VSS_U20	XA[5]	MMC_PC	XA[12]	VSSIO	XA[13] SD_BA[0]	ACS_IND	MS_D[0]	TESTHWE	4
5	VSSA_U20	VDDI_U20	GPIO_A[6] FRM1	GPIO_A[7] SDI1	XD[7]	VDDI	XA[16]	XD[14]	VDDA_U20	VSSI	VDDIO	XA[14] SD_BA[1]	VDDI	IIDE_nCS3	MMC_CD	5
6	GPIO_A[2] CLRCK	GPIO_A[0] SDO0	VDDA_U20	VDDI	XD[3]	VSSI	XD[6]	XD[15]	XD[13]	XA[9]	XA[21] DQM[0]	XA[19] DQS[1]	VSSIO	ND_nCE[1]	MST[2]	6
7	GPIO_A[1] CBCLK	GPIO_A[4] SDO1	GPIO_A[3] SDI0 CDAI	GPIO_A[9] BW[1] SCK2	GPIO_A[11] SDI2 SCL	XD[4]	XD[5]	XD[12]	XA[3]	XA[8]	XA[18] DQS[0]	nCS[3] GPIO_B[5]	TESTHOE	MS_CD	MST[1]	7
8	TESTPACK	IIDE_nRESET	GPIO_A[5] SCK1	VDDIO	VDDI	VSSI	XD[10]	XD[11]	nWE	VDD_U20	TESTCE2	TESTCE3	TEST_MWP	USB_DP GPIO_B[26]	USBH_DP GPIO_B[28]	8
9	TESTIS16	VSS_U20	TESTEASL	XD[2]	VSS_NOR	XD[8]	XA[0]	XA[1]	XA[2]	USBH_DN GPIO_B[29]	VSSI	USB_DN GPIO_B[27]	MST[0]	ND_nWE	ND_nOE	9
10	ND_WP_CTL	MMC_D[2]	TMS	nTRST	XD[0]	VDD_U20	VDDI	XD[9]	TESTREG	nOE	GPIO_B[9] UT_RX	GPIO_B[0]	ND_CLE	XA[17]	ND_ALE	10
11	MMC_D[3]	TCK	U_nRESET	TDI	XD[1]	PKG	VDDA_ADC	VSSA_PLL	nRESET	XOUT	GPIO_B[8] UT_TX	GPIO_B[21] BM[0] BCLK	GPIO_B[7]	VSS_U20	ND_RDY	11
12	TDO	MMC_D[0]	U_nTEST	FCSN	GPIO_D[17] SCL	VSSI	VSSA_ADC	VDDA_PLL	VDDIO	XIN	VSSIO	ND_D[5]	GPIO_B[22] BM[1] LRCK	ND_D[0]	ND_nWP	12
13	MMC_D[1]	MMC_CLK	MODE1	VSSIO	ND_D[13]	ND_D[10]	ADIN2	VDDI_U20	ACT_nSPND	TESTCE4	XTIN	GPIO_B[23] MCLK	ND_D[6]	ND_D[2]	ND_D[1]	13
14	MMC_CMD	ND_D[14]	GPIO_D[16] SDA	ND_D[12]	ND_D[8]	ADIN0	XFILT	U_nEA	IIDE_nUSB	VDD_OSC	TESTFAL	XTOUT	GPIO_B[24] BM[2] DAO	VDDIO_USB	ND_D[3]	14
15	ND_D[15]	GPIO_D[15]	ND_D[11]	ND_D[9]	ADIN4	VSS_U20	U_CF	AGN_nRESET	READY	TESTFCL	TESTFWE	TESTFRD	GPIO_B[25] DAI	ND_D[7]	ND_D[4]	15
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	

Figure 1.13 TCC767 Package Diagram (225-FPBGA-1313 / Bottom View)

Figure 1.14 TCC768 Package Diagram (144-BGA-1010 / Bottom View)

2 ADDRESS & REGISTER MAP

2.1 Address Map

The TCC76x has fixed address maps for digital audio en-decoder system. The address space is separated MSB 4bits of address bus, the following table represents overall address space of TCC76x system.

Table 2.1 Address Allocation Map of the TCC76x

Address Space	Device Name
0x00000000 ~ 0x0FFFFFFF	1) if Remap is 0, External ROM of chip select 3 or internal ROM. 2) if Remap is 1, Other type memory according to base value. 3) if any other type of memory is not assigned to this area, then Internal SRAM is assigned.
0x10000000 ~ 0x1FFFFFFF	Not Used
0x20000000 ~ 0x2FFFFFFF	Assigned to SDRAM initially.
0x30000000 ~ 0x3FFFFFFF	Assigned to internal SRAM
0x40000000 ~ 0x4FFFFFFF	Assigned to chip select 0 Initially the configuration register is set to SRAM
0x50000000 ~ 0x5FFFFFFF	Assigned to chip select 1 Initially the configuration register is set to IDE type device
0x60000000 ~ 0x6FFFFFFF	Assigned to chip select 2 Initially the configuration register is set to NAND flash
0x70000000 ~ 0x7FFFFFFF	Assigned to chip select 3 Initially the configuration register is set to ROM
0x80000000 ~ 0x8FFFFFFF	Various internal peripheral devices
0x90000000 ~ 0x9FFFFFFF	Not Used
0xA0000000 ~ 0xAFFFFFFF	
0xB0000000 ~ 0xBFFFFFFF	
0xC0000000 ~ 0xCFFFFFFF	
0xD0000000 ~ 0xDFFFFFFF	
0xE0000000 ~ 0xEFFFFFFF	Assigned to internal boot ROM
0xF0000000 ~ 0xFFFFFFFF	Assigned to memory controller configuration register space

The address space (0x00000000 ~ 0x0FFFFFFF) is initially allocated to internal or external PROM for booting procedure, and a special flag exists in memory controller unit for remapping this space to other type of memories. That is, if the remap flag is set to 1, this space is released from the external ROM of chip select 3 or internal boot ROM. Refer to the description of memory controller for detailed operation.

The TCC76x has one chip select for SDRAM, and four chip selects for other type of memories. Their address space is dependent on the configuration registers for each chip selects. The above address map is only at the initial state of the TCC76x; these maps can be changed at user requests.

The TCC76x has various peripherals for controlling a digital audio en-decoder system. These peripherals can be configured appropriately by it's own registers that can be accessed through specially allocated address. These address maps are represented in the following table. In case of memory controller, its space is separated for preventing illegal accessing.

Refer to corresponding sections for detail information of each peripheral.

Table 2.2 Address Allocations for Internal Peripherals (Base = 0x80000000)

Offset Address Space	Peripheral
0x000 ~ 0x0FF	DAI & CDIF
0x100 ~ 0x1FF	Interrupt Controller
0x200 ~ 0x2FF	Timer Counter
0x300 ~ 0x3FF	GPIO
0x400 ~ 0x4FF	Clock Generator & Power Management
0x500 ~ 0x5FF	USB1.1 Device
0x600 ~ 0x6FF	UART/IrDA
0x700 ~ 0x7FF	GSIO (General Purpose Serial Input/Output)
0x800 ~ 0x8FF	I2C
0x900 ~ 0x9FF	ECC
0xA00 ~ 0xAFF	ADC Control & Etc.
0xB00 ~ 0xBFF	Camera Interface
0xC00 ~ 0xCFF	Reserved
0xD00 ~ 0xDFF	USB1.1 Host
0xE00 ~ 0xEFF	DMA Controller
0xF00 ~ 0xFFF	LCD controller (TCC761 only)

- Address decoding logic only monitors base address (for example, 0x8xxxxxxx, 0x4xxxxxxx, etc.), and bit11~bit8 of accessing address bus. There can be a lot of mirror images of address space that are repeated at every 4Kbyte boundary, user can access certain registers by these mirror images also, so care must be taken not to modify these registers unintentionally.

2.2 Register Map

Table 2.3 DAI & CDIF Register Map (Base = 0x80000000)

Name	Address	Type	Reset	Description
DADI_L0	0x00	R	-	Digital Audio Left Input Register 0
DADI_R0	0x04	R	-	Digital Audio Right Input Register 0
DADI_L1	0x08	R	-	Digital Audio Left Input Register 1
DADI_R1	0x0C	R	-	Digital Audio Right Input Register 1
DADI_L2	0x10	R	-	Digital Audio Right Input Register 2
DADI_R2	0x14	R	-	Digital Audio Right Input Register 2
DADI_L3	0x18	R	-	Digital Audio Right Input Register 3
DADI_R3	0x1C	R	-	Digital Audio Right Input Register 3
DADO_L0	0x20	R/W	-	Digital Audio Left Output Register 0
DADO_R0	0x24	R/W	-	Digital Audio Right Output Register 0
DADO_L1	0x28	R/W	-	Digital Audio Left Output Register 1
DADO_R1	0x2C	R/W	-	Digital Audio Right Output Register 1
DADO_L2	0x30	R/W	-	Digital Audio Left Output Register 2
DADO_R2	0x34	R/W	-	Digital Audio Right Output Register 2
DADO_L3	0x38	R/W	-	Digital Audio Left Output Register 3
DADO_R3	0x3C	R/W	-	Digital Audio Right Output Register 3
DAMR	0x40	R/W	0x0000	Digital Audio Mode Register
DAVC	0x44	R/W	0x0000	Digital Audio Volume Control Register
CDDI_0	0x80	R	-	CD Digital Audio Input Register 0
CDDI_1	0x84	R	-	CD Digital Audio Input Register 1
CDDI_2	0x88	R	-	CD Digital Audio Input Register 2
CDDI_3	0x8C	R	-	CD Digital Audio Input Register 3
CICR	0x90	R/W	0x0000	CD Interface Control Register

Table 2.4 Interrupt Controller Register Map (Base = 0x80000100)

Name	Address	Type	Reset	Description
IEN	0x00	R/W	0x0000	Interrupt Enable Register
CREQ	0x04	W	-	Clear Interrupt Request Register
IREQ	0x08	R	0x0000	Interrupt Request Flag Register
IRQSEL	0x0C	R/W	0x0000	IRQ/FIQ Select Register
ICFG	0x10	R/W	0x0000	External interrupt configuration register
MREQ	0x14	R	0x0000	Masked interrupt request flag register
TSTREQ	0x18	R/W	0x0000	Test Mode Register (must be remained zero)
IRQ	0x20	R	-	IRQ Raw Status (IREQ & IRQSEL)
FIQ	0x24	R	-	FIQ Raw Status (~IREQ & IRQSEL)
MIRQ	0x28	R	-	Masked IRQ Status (IRQ & IEN)
MFIQ	0x2C	R	-	Masked FIQ Status (FIQ & IEN)
TMODE	0x30	R/W	0x000007C0	Trigger Mode (0: edge, 1:level)
SYNC	0x34	R/W	0x00000000	Synchronizer Control
WKUP	0x38	R/W	0x00000000	Wakeup Control

Table 2.5 Timer/Counter Register Map (Base = 0x80000200)

Name	Address	Type	Reset	Description
TCFG0	0x0000	R/W	0x00	Timer/Counter 0 Configuration Register
TCNT0	0x0004	R/W	0x0000	Timer/Counter 0 Counter Register
TREF0	0x0008	R/W	0xFFFF	Timer/Counter 0 Reference Register
TMREF0	0x000C	R/W	0x0000	Timer/Counter 0 Middle Reference Register
TCFG1	0x0010	R/W	0x00	Timer/Counter 1 Configuration Register
TCNT1	0x0014	R/W	0x0000	Timer/Counter 1 Counter Register
TREF1	0x0018	R/W	0xFFFF	Timer/Counter 1 Reference Register
TMREF1	0x001C	R/W	0x0000	Timer/Counter 1 Middle Reference Register
TCFG2	0x0020	R/W	0x00	Timer/Counter 2 Configuration Register
TCNT2	0x0024	R/W	0x0000	Timer/Counter 2 Counter Register
TREF2	0x0028	R/W	0xFFFF	Timer/Counter 2 Reference Register
TMREF2	0x002C	R/W	0x0000	Timer/Counter 2 Middle Reference Register
TCFG3	0x0030	R/W	0x00	Timer/Counter 3 Configuration Register
TCNT3	0x0034	R/W	0x0000	Timer/Counter 3 Counter Register
TREF3	0x0038	R/W	0xFFFF	Timer/Counter 3 Reference Register
TMREF3	0x003C	R/W	0x0000	Timer/Counter 3 Middle Reference Register
TCFG4	0x0040	R/W	0x00	Timer/Counter 4 Configuration Register
TCNT4	0x0044	R/W	0x00000	Timer/Counter 4 Counter Register
TREF4	0x0048	R/W	0xFFFFF	Timer/Counter 4 Reference Register
TCFG5	0x0050	R/W	0x00	Timer/Counter 5 Configuration Register
TCNT5	0x0054	R/W	0x00000	Timer/Counter 5 Counter Register
TREF5	0x0058	R/W	0xFFFFF	Timer/Counter 5 Reference Register
TIREQ	0x0060	R/W	0x0000	Timer/Counter n Interrupt Request Register
TWDCFG	0x0070	R/W	0x0000	Watchdog Timer Configuration Register
TWDCLR	0x0074	W	-	Watchdog Timer Clear Register
TC32EN	0x0080	R/W	0x00007FFF	32-bit Counter Enable / Pre-scale Value
TC32LDV	0x0084	R/W	0x00000000	32-bit Counter Load Value
TC32CMP0	0x0088	R/W	0x00000000	32-bit Counter Match Value 0
TC32CMP1	0x008C	R/W	0x00000000	32-bit Counter Match Value 1
TC32PCNT	0x0090	R/W	-	32-bit Counter Current Value (pre-scale counter)
TC32MCNT	0x0094	R/W	-	32-bit Counter Current Value (main counter)
TC32EN	0x0080	R/W	0x00007FFF	32-bit Counter Enable / Pre-scale Value

Table 2.6 GPIO Register Map (Base = 0x80000300)

Name	Address	Type	Reset	Description
GDATA_A	0x00	R/W	0xFFFFFFFF	GPIO_A Data Register
GIOCON_A	0x04	R/W	0x00000000	GPIO_A Direction Control Register
GSEL_A	0x08	R/W	0x00000000	GPIO_A Function Select Register 1
GTSEL_A	0x0C	R/W	0x00000000	GPIO_A Function Select Register 2
GDATA_B	0x10	R/W	0x3FFFFFFF	GPIO_B Data Register
GIOCON_B	0x14	R/W	0x000000FF	GPIO_B Direction Control Register
GSEL_B	0x18	R/W	0x3C0000FF	GPIO_B Function Select Register 1
GTSEL_B	0x1C	R/W	0x00000000	GPIO_B Function Select Register 2
GDATA_C	0x20	R/W	0xFFFF	GPIO_C Data Register
GIOCON_C	0x24	R/W	0x0000	GPIO_C Direction Control Register
GDATA_D	0x30	R/W	0x7FFF	GPIO_D Data Register
GIOCON_D	0x34	R/W	0x0000	GPIO_D Direction Control Register

- Shaded registers are only valid in TCC761.

Table 2.7 Clock Generator Register Map (Base = 0x80000400)

Name	Address	Type	Reset	Description
CKCTRL	0x00	R/W	0x00007FFE	Clock Control Register
PLLMODE	0x04	R/W	0x00002E02	PLL Control Register
SCLKmode	0x08	R/W	0x00082000	System Clock Control Register
DCLKmode	0x0C	R/W	0x00000800	DCLK (DAI/CODEC) Control Register
EACLKmode	0x10	R/W	0x00000000	ADCLK and EX2CLK Control Register
EX1CLKmode	0x14	R/W	0x00000000	EX1CLK Control Register
UTCLKmode	0x18	R/W	0x000001BE	UTCLK (UART) Control Register
UBCLKmode	0x1C	R/W	0x00000000	UBCLK (USB) Control Register
LCLKmode	0x20	R/W	0x00000000	LCLK (LCD) Control Register
TCLKmode	0x24	R/W	0x00000000	TCLK (Timer) Control Register
GCLKmode	0x28	R/W	0x00000000	GCLK (GSIO) Control Register
CIFCLKmode	0x2C	R/W	0x00000000	CIFCLK Control Register
SW_nRST	0x3C	R/W	0x0000FEFF	Software Reset for each peripherals
PWDCTL	0x40	R/W	0x00000000	Power Down Control
DIVMODE	0x44	R/W	0x00000000	Divider Mode Enable (DCO Disable)
HCLKSTOP	0x48	R/W	0x00000000	HCLK Stop Control

Table 2.8 USB Register Map (Base = 0x80000500)

Name	Address	Type	Reset	Description
NON INDEXED REGISTERS				
UBFADR	0x00	R/W	0x00	Function Address Register
UBPWR	0x04	R/W	0x00	Power Management Register
UBEIR	0x08	R/W	0x00	Endpoint Interrupt Flag Register
UBIR	0x18	R/W	0x00	USB Interrupt Flag Register
UBEIEN	0x1C	R/W	0x07	Endpoint Interrupt Enable Register
UBIEN	0x2C	R/W	0x04	Interrupt Enable Register
UBFRM1	0x30	R	0x00	Frame Number 1 Register
UBFRM2	0x34	R	0x00	Frame Number 2 Register
UBIDX	0x38	W	0x00	Index Register
COMMON INDEXED REGISTER				
MAXP	0x40	R/W	0x01	IN Max Packet Register
IN INDEXED REGISTERS				
INCSR1	0x44	R/W	0x00	IN CSR1 Register (EP0 CSR Register)
INCSR2	0x48	R/W	0x20	IN CSR2 Register
OUT INDEXED REGISTERS				
OCSR1	0x50	R	0x00	OUT CSR1 Register
OCSR2	0x54	R/W	0x00	OUT CSR2 Register
OFIFO1	0x58	R	0x00	OUT FIFO Write Count 1 Register
OFIFO2	0x5C	R	0x00	OUT FIFO Write Count 2 Register
FIFO REGISTERS				
EP0FIFO	0x80	R/W	Unknown	EP0 FIFO Register
EP1FIFO	0x84	R/W	Unknown	EP1 FIFO Register
EP2FIFO	0x88	R/W	Unknown	EP2 FIFO Register
DMA REGISTERS				
DMACON	0xC0	R/W	0x00	DMA Control Register
DMAEP1	0xC4	R/W	Unknown	EP1 FIFO Access Register for DMA
DMAEP2	0xC8	R/W	Unknown	EP2 FIFO Access Register for DMA

Table 2.9 USBH Register Map (Base = 0x80000D00)

Name	Address	Type	Reset	Description
HcRevision	0x00	R	0x00000010	Control and status registers
HcControl	0x04	R/W	0x00000000	
HcCommandStatus	0x08	R	0x00000000	
HcInterruptStatus	0x0C	R	0x00000000	
HcInterruptEnable	0x10	R/W	0x00000000	
HcInterruptDisable	0x14	W	0x00000000	
HcHCCA	0x18	R/W	0x00000000	Memory pointer registers
HcPeriodCurrentED	0x1C	R	0x00000000	
HcControlHeadED	0x20	R/W	0x00000000	
HcControlCurrentED	0x24	R/W	0x00000000	
HcBulkHeadED	0x28	R/W	0x00000000	
HcBulkCurrentED	0x2C	R/W	0x00000000	
HcDoneHead	0x30	R	0x00000000	
HcRmInterval	0x34	R/W	0x00002EDF	Frame counter registers
HcFmRemaining	0x38	R/W	0x00000000	
HcFmNumber	0x3C	R/W	0x00000000	
HcPeriodStart	0x40	R/W	0x00000000	
HcLSThreshold	0x44	R/W	0x00000628	
HcRhDescriptorA	0x48	R/W	0x02001202	Root hub registers
HcRhDescriptorB	0x4C	R/W	0x00000000	
HcRhStatus	0x50	R/W	0x00000000	
HcRhPortStatus1	0x54	R/W	0x00000100	
HcRhPortStatus2	0x58	R/W	0x00000100	

Table 2.10 UART/IrDA Register Map (Base = 0x80000600)

Name	Address	Type	Reset	Description
UTRXD	0x00	R	Unknown	Receiver Buffer Register
UTTXD	0x00	W	Unknown	Transmitter Holding Register
UTDL	0x04	W	0x0000	Divisor Latch Register
UTIR	0x08	R/W	0x000	Interrupt Register
UTCR	0x0C	R/W	0x000	UART Control Register
UTLSR	0x10	R	0x0101	Status Register
IrDACFG1	0x14	R/W	0x0003	IrDA Configuration Register 1
IrDACFG2	0x18	R/W	0x4da1	IrDA Configuration Register 2

Table 2.11 GSIO Register Map (Base = 0x80000700)

Name	Address	Type	Reset	Description
GSDO0	0x00	R/W	Unknown	GSIO0 Output Data Register
GSDI0	0x04	R/W	Unknown	GSIO0 Input Data Register
GSCR0	0x08	R/W	0x0000	GSIO0 Control Register
GSGCR	0x0C	R/W	0x0000	GSIO Global Control Register
GSDO1	0x10	R/W	Unknown	GSIO1 Output Data Register
GSDI1	0x14	R/W	Unknown	GSIO1 Input Data Register
GSCR1	0x18	R/W	0x0000	GSIO1 Control Register
GSDO2	0x20	R/W	Unknown	GSIO2 Output Data Register
GSDI2	0x24	R/W	Unknown	GSIO2 Input Data Register
GSCR2	0x28	R/W	0x0000	GSIO2 Control Register
GSDO3	0x30	R/W	Unknown	GSIO3 Output Data Register
GSDI3	0x34	R/W	Unknown	GSIO3 Input Data Register
GSCR3	0x38	R/W	0x0000	GSIO3 Control Register

Table 2.12 I2C Register Map (Base Address = 0x80000800)

Name	Address	Type	Reset	Description
PRES	0x00	RW	0xFFFF	Clock Prescale register
CTRL	0x04	RW	0x0000	Control Register
TXR	0x08	W	0x0000	Transmit Register
CMD	0x0C	W	0x0000	Command Register
RXR	0x10	R	0x0000	Receive Register
SR	0x14	R	0x0000	Status Register

Table 2.13 ECC Register Map (Base Address = 0x80000900)

Name	Address	Type	Reset	Description
ECC_CTRL	0x00	R/W	0x00000000	ECC Control Register
ECC_BASE	0x04	R/W	0x00000000	Base Address for ECC Calculation
ECC_MASK	0x08	R/W	0x00000000	Address mask for ECC area.
ECC_CLR	0x0C	W	-	Clear ECC output register
SLC_ECC0	0x10	R	0x00000000	1st Block ECC output for SLC NAND
SLC_ECC1	0x14	R	0x00000000	2nd Block ECC output for SLC NAND
SLC_ECC2	0x18	R	0x00000000	3rd Block ECC output for SLC NAND
SLC_ECC3	0x1C	R	0x00000000	4th Block ECC output for SLC NAND
SLC_ECC4	0x20	R	0x00000000	5th Block ECC output for SLC NAND
SLC_ECC5	0x24	R	0x00000000	6th Block ECC output for SLC NAND
SLC_ECC6	0x28	R	0x00000000	7th Block ECC output for SLC NAND
SLC_ECC7	0x2C	R	0x00000000	8th Block ECC output for SLC NAND
MLC_ECC0W	0x40	W	-	MLC NAND ECC calculation register 0
MLC_ECC1W	0x44	W	-	MLC NAND ECC calculation register 1
MLC_ECC0R	0x48	R/W	0x00000000	Calculated ECC output 0 for MLC NAND
MLC_ECC1R	0x4C	R/W	0x00000000	Calculated ECC output 1 for MLC NAND

Table 2.14 ADC Interface & ETC Register Map (Base = 0x80000A00)

Name	Address	Type	Reset	Description
ADCCON	0x00	R/W	0x00000000	ADC Control Register
ADCDATA	0x04	R	Unknown	ADC Data Register
USBCTR	0x14	R/W	0x00000004	USB Port Control Register
TSTSEL	0x18	R/W	0x00000000	Test Mode Control Register
MISCCFG	0x1C	R/W	0x00000000	Miscellaneous Configuration Register
CFGPUA	0x20	R/W	0x00000000	Pull-up Enable for GPIO_A
CFGPUB	0x24	R/W	0x00000000	Pull-up Enable for GPIO_B
CFGPUC	0x28	R/W	0x00000000	Pull-up Enable for GPIO_C
CFGPUD	0x2C	R/W	0x003C0000	Pull-up Enable for GPIO_D
CFGDRVAL	0x30	R/W	0x00000000	Buffer Drive Strength Select AL
CFGDRVAH	0x34	R/W	0x00000000	Buffer Drive Strength Select AH
CFGDRVBL	0x38	R/W	0x00000000	Buffer Drive Strength Select BL
CFGDRVBH	0x3C	R/W	0x00000000	Buffer Drive Strength Select BH
CFGDRVCL	0x40	R/W	0x00000000	Buffer Drive Strength Select CL
CFGDRVCH	0x44	R/W	0x00000000	Buffer Drive Strength Select CH
CFGDRVDL	0x48	R/W	0x00000000	Buffer Drive Strength Select DL
CFGDRVDH	0x4C	R/W	0x00000000	Buffer Drive Strength Select DH
CFGDRVXL	0x50	R/W	0x03FFFFFF	Buffer Drive Strength Select XL
CFGDRVXH	0x54	R/W	0x04000000	Buffer Drive Strength Select XH
CFGSYS	0x60	R/W	0x00000000	System Configuration
ADCCONA	0x80	R/W	0x00000018	ADC Control Register A
ADCSTATUS	0x84	R/W	Unknown	ADC Status Register
ADCCFG	0x88	R/W	0x00002400	ADC Configuration Register

Table 2.15 CIF Register Map (Base Address = 0x80000B00)

Name	Address	Type	Reset	Description
CPCR	0x00	W	0x00000402	Color/Pattern Configuration Register
656FCR1	0x04	W	0x06FF0000	CCIR656 Configuration Register 1
656FCR2	0x08	W	0x0000010B	CCIR656 Configuration Register 2
IICR1	0x0C	W	0x028001E0	Input Image Configuration Register 1
IICR2	0x10	W	0x00000000	Input Image Configuration Register 2
CDCR1	0x14	W	0x00000003	CIF DMA Configuration Register
CDCR2	0x18	W	0x20000000	Memory Address for Y Channel
CDCR3	0x1C	W	0x28000000	Memory Address for Cb(U) Channel
CDCR4	0x20	W	0x2C000000	Memory Address for Cr(V) Channel
FIFOSTATE	0x24	R	0x00000000	FIFO Status Register
CIRQ	0x28	W/R	0x00000000	Interrupt & CIF Operating Register
ICCTRL	0x2C	W	0x00000000	Image Clock Control

Table 2.16 DMA Controller Register Map (Base = 0x80000E00)

Name		Address	Type	Reset	Description
CHANNEL0	ST_SADR0	0x00	R/W	-	Start Address of Source Block
	SPARAM0	0x04/0x08	R/W	-	Parameter of Source Block
	C_SADR0	0x0C	R	-	Current Address of Source Block
	ST_DADR0	0x10	R/W	-	Start Address of Destination Block
	DPARAM0	0x14/0x18	R/W	-	Parameter of Destination Block
	C_DADR0	0x1C	R	-	Current Address of Destination Block
	HCOUNT0	0x20	R/W	0x00000000	Initial and Current Hop count
	CHCTRL0	0x24	R/W	0x00000000	Channel Control Register
CHCONFIG		0x2C	R/W	-	Channel Configuration Register
CHANNEL1	ST_SADR1	0x30	R/W	-	Start Address of Source Block
	SPARAM1	0x34/0x38	R/W	-	Parameter of Source Block
	C_SADR1	0x3C	R	-	Current Address of Source Block
	ST_DADR1	0x40	R/W	-	Start Address of Destination Block
	DPARAM1	0x44/0x48	R/W	-	Parameter of Destination Block
	C_DADR1	0x4C	R	-	Current Address of Destination Block
	HCOUNT1	0x50	R/W	0x00000000	Initial and Current Hop count
	CHCTRL1	0x54	R/W	0x00000000	Channel Control Register

Table 2.17 LCD Controller Register Map (Base = 0x80000F00)

Name	Address	Type	Reset	Description
LCTRL	0x00	R/W	0x00000006	control register
LCLKDIV	0x04	R/W	0x00000000	ac-bias clock and pixel clock divisor
LHTIME1	0x08	R/W	0x00000000	Horizontal axis timing control register1
LHTIME2	0x0C	R/W	0x00000000	Horizontal axis timing control register2
LVTIME1	0x10	R/W	0x00000000	Vertical axis timing control register1
LVTIME2	0x14	R/W	0x00000000	Vertical axis timing control register2
LVTIME3	0x18	R/W	0x00000000	Vertical axis timing control register3
LVTIME4	0x1C	R/W	0x00000000	Vertical axis timing control register4
LLUTRD	0x20	R/W	0x00000000	Lookup table for red color
LLUTGR	0x24	R/W	0x00000000	Lookup table for green color
LLUTBL	0x28	R/W	0x00000000	Lookup table for blue color
LDP7L	0x2C	R/W	0x4D2B3401	modulo 7 dithering pattern low register
LDP7H	0x30	R/W	0x0000003F	modulo 7 dithering pattern high register
LDP5	0x34	R/W	0x1D0B0610	modulo 5 dithering patterns
LDP4	0x38	R/W	0x00000768	modulo 4 dithering patterns
LDP3	0x3C	R/W	0x00000034	Modulo 3 dithering patterns
LDS	0x40	R/W	0x00000000	Display size register
LSTATUS	0x44	R/Clear	0x00000000	Status register
LIM	0x48	R/W	0x00000007	Interrupt mask register
LIP	0x4C	R/W	0x00000000	Image position register
LIS	0x50	R/W	0x00000000	Image size register
LIBA0	0x54	R/W	0x00000000	Image base address register 0
LICA0	0x58	R	0x00000000	Image current address register
LIBA1	0x5C	R/W	0x00000000-	Image base address register 1
LIBA2	0x60	R/W	0x00000000	Image base address register 2

Table 2.18 Memory Controller Register Map (Base = 0xF0000000)

Name	Address	Type	Reset	Description
SDCFG	0x00	R/W	0x62E97010	SDRAM Configuration Register
SDFSM	0x04	R	-	SDRAM FSM Status Register
MCFG	0x08	R/W	0xZZZZ_02	Miscellaneous Configuration Register
TST	0x0C	W	0x00000000	Test mode register (must be remained zero)
CSCFG0	0x10	R/W	0x0B405649	External Chip Select 0 Configuration Register (Initially set to SRAM)
CSCFG1	0x14	R/W	0x0150569A	External Chip Select 1 Configuration Register (Initially set to IDE)
CSCFG2	0x18	R/W	0x006056BA	External Chip Select 2 Configuration Register (Initially set to NAND)
CSCFG3	0x1C	R/W	0x0A70569A	External Chip Select 3 Configuration Register (Initially set to NOR)
CLKCFG	0x20	R/W	0xXXXXXX00	Memory Controller Clock Count Register
SDCMD	0x24	W	-	SDRAM Command Register

- Z means that it is determined by the status of some external pins.

Table 2.19 NAND flash Register Map (Base = N * 0x10000000)

Name	Address	Type	Reset	Description
NDCMD	0x00	R/W	Unknown	Command Cycle Register
NDLADR	0x04	W	-	Linear Address Cycle Register
NDBADR	0x08	W	-	Block Address Cycle Register
NDIADR	0x0C	W	-	Single Address Cycle Register
NDDATA	0x10	R/W	Unknown	Data Access Cycle Register

- N represents BASE field of CSCFGn registers that is configured as NAND flash chip select.

3 CPU

3.1 Overview

The TCC76x has adopted the ARM940T core for controlling system and processing various kinds of digital signals. It has a Harvard cache architecture with separate 4Kbyte data and 4Kbytes instruction caches, each with 4-word of line length.

A protection unit allows eight regions of memory to be defined, each with individual cache and write buffer configurations and access permissions. The cache system is software configurable to provide highest average of performance or to meet the needs of real-time systems.

The followings are key features of ARM940T core.

- CPU ARM940T
- Cache 4KB for Data / 4KB for Instruction
- Operating State ARM state / THUMB state
- Operating Mode 7 different modes (SVC/UND/ABT/FIQ/IRQ/SYS/USR)
- Memory Format Little endian (ARM940T itself supports big-endian type also, but the memory controller in the TCC76x only support for little-endian type)
- Address Space 32bit of 4Gbyte
- Instruction 32bit (in ARM state) / 16bit (in THUMB state)

3.2 Functional Description

For detailed description of the CPU, refer to "ARM940T Technical Reference Manual".

3.2.1 Operating States

The ARM9TDMI core allows user application programs to freely switch between ARM state using 32bit of instruction set and THUMB state using 16bit of instruction set.
The switching between two states does not affect internal registers and operating modes.

3.2.2 Memory Formats

The ARM940T itself can treat words in memory as being stored either in big-endian or little-endian, but in the TCC76x, there is only little-endian supported by the memory controller. The following figure illustrates the structure of little-endian type of memories.

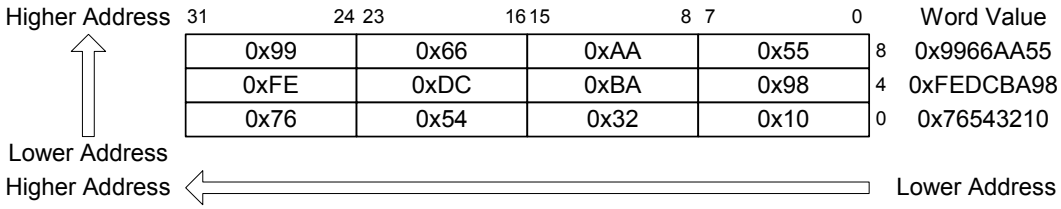


Figure 3.1 Little-Endian Addresses of Bytes-Words

3.2.3 Instruction Length

The instruction length can be either 32 bits (ARM state) or 16 bits (THUMB state).

3.2.4 Data Types

ARM940T supports byte (8 bits), half-word (16 bits), and word (32 bits) data types. Words must be aligned to 4-byte boundaries and half words to 2-byte boundaries.

3.2.5 Operating Modes

ARM940T supports seven modes of operation:

- USER (usr) The normal ARM program execution mode
- FIQ (fiq) Designed to support a data transfer or channel process
- IRQ (irq) Used for general purpose interrupt handling
- Supervisor (svc) Protected mode for the operating system
- Abort (abt) Entered after a data or instruction prefetch abort
- System (sys) A privileged user mode for the operating system
- Undefined (und) Entered when an undefined instruction is executed

Switching between these modes may be made under software control, or may be brought about by interrupts or exception processing. Most application programs will execute in User mode. The non-user mode known as privileged modes are entered in order to service interrupts or exceptions, or to access protected resources.

3.2.6 Coprocessor CP15

The ARM940T cached processor macrocell includes the ARM9TDMI microprocessor core, instruction and data caches, a write-buffer, and a protection unit for defining the attributes of regions of memory.

The ARM940T incorporates two coprocessors:
- CP14 which allows software access to the debug communications channel
- CP15 which allows configuration of the caches, protection unit, and other system options such as clock operation.

The register map of CP15 is shown in the following table.

Table 3.1 CP15 Register Map

Register	Function	Access
0	ID code / Cache type	note
1	Control	Read / Write
2	Cacheable	note
3	Write buffer control	Read / Write
4	Reserved	-
5	Protection region access permissions	note
6	Protection region base/size control	note
7	Cache operations	Write only
8	Reserved	-
9	Cache lockdown	Read / Write
10 – 14	Reserved	-
15	Test	Not accessed in normal operation

NOTE: Register of 0, 2, 5, and 6 each provide access to more than one register. The register accessed depends on the value of the opcode_2 field. Refer to the register descriptions for further information.

3.2.7 Protection Unit

The protection unit is used to partition memory and set individual protection attributes for each partition. The instruction address space and the data address space can each be divided up to 8 regions of variable size.

The protection unit is programmed via CP15 registers 1, 2, 3, 5 and 6.

Before the protection unit is enabled, at least one valid data and instruction region must be programmed. If they are not programmed, the ARM940T can enter a state that is recoverable only by reset. Setting bit 0 of the CP15 register 1 (the control register) enables the protection unit.

When the protection unit is disabled, all instruction fetches are non-cacheable and all data accesses are non-cacheable and non-bufferable.

3.2.8 Caches and Write Buffer

3.2.8.1 Cache Architecture

The ARM940T incorporates a 4KB of instruction cache, a 4KB of data cache, and an 8-word write buffer. The Icache and Dcache have similar architectures, as illustrated in the following figure.

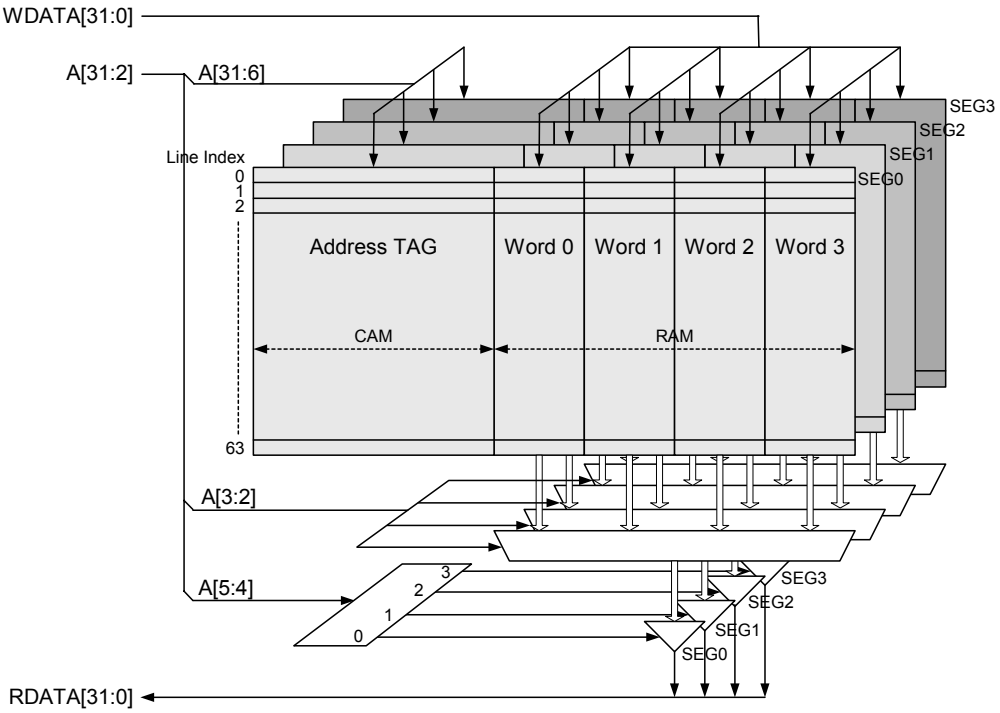


Figure 3.2 4KB Cache Architecture in ARM940T

Each cache comprises four, fully associative 1KB segments which support single-cycle reads, and either one or two-cycle writes depending on the sequentiality of the access.

Each cache segment consists of 64 CAM (Content Addressable Memory) rows which each select one of 64 RAM four-word long lines. during a cache access, a segment is selected and the access address is compared with the 64 TAGs in the CAM. If a match occurs (or a hit), the matched line is enabled and the data can be accessed. If none of the TAGs match (or a miss), then external memory must be accessed, unless the access is a buffered write in which case the write buffer is used.

If a read access from a cacheable memory region misses, new data is loaded into one of the 64 row lines of the selected segment. This is an *allocate on read-miss* replacement policy. Selection is performed by a randomly clocked target row counter.

Critical or frequently-accessed instructions or data can be locked into the cache by restricting the range of the target counter. Locked lines cannot be replaced and remain in the cache until they are unlocked or flushed.

The CAM allows 64 address TAGs to be stored for an address that selects a given segment (64-way associativity). This reduces the chance of an address sequence in,

for example, a program loop that constantly selects the same segment, from replacing data that is required again in a later iteration of the loop. The overhead for high associativity is the need to store a larger TAG. In the case of the ARM940T, this is 26 bits per line.

The address bits are assigned as follows:

Bits 31:6	Selects an address tag in CAM
Bits 5:4	Selects one of the four cache segments
Bits 3:2	Selects a word in the cache line.

3.2.8.2 Instruction Cache

The ARM940T has a 4KB Icache comprising four 64-way associative segments of 16 bytes per line per segment. The Icache uses the physical address generated by the processor core. It employs a policy of allocate on read-miss and is always reloaded one cache line (four words) at a time, through the external interface.

The Icache is always disabled on reset.

3.2.8.3 Data Cache

The ARM940T has a 4KB Dcache comprising 256 lines of 16 bytes (four words), arranged as four 64-way associative segments. It employs an allocate on read-miss policy, and is always reloaded a cache line (four words) at a time through the external interface. The Dcache supports both Write-back (WB) and Write-through (WT) modes.

The GCd (Gated Cacheable for data) bit and the GBd (Gated Bufferable for data) bit control the Dcache behavior. For this reason, the protection unit must be enabled before the Dcache is enabled.

3.2.8.4 The Write Buffer

The ARM940T provides a write buffer to improve system performance. The write buffer can buffer up to eight words of data and four separate non-sequential addresses.

Write buffer behavior is controlled by the protection region attributes of the region that store being performed and by the Dcache and control bits (GCd and GBd) from the protection unit. These control bits are generated as follows:

GCd bit	The GCd bit is generated from the cacheable attribute of the protection region AND the Dcache enable AND the protection unit enable.
GBd bit	The GBd bit is generated from the bufferable attribute for the protection region AND the protection unit enable

All accesses are initially non-cacheable and non-bufferable until the protection unit has been programmed and enabled. It follows that the write buffer cannot be used while the protection unit is disabled.

On reset, the buffer is flushed.

3.3 Clock Modes

3.3.1 About clocking modes

The ARM940T has two clock inputs HCLK and FCLK that allow flexible clocking configurations. There are three different modes of operation, selected using bits 30 and 31 of CP15 register 1 (C1), the control register. These modes are:

- FastBus
- Synchronous
- Asynchronous

The TCC76x does not support Synchronous Mode. Do not enable Synchronous Mode.

The ARM940T is a pseudo-static desing and both clocks can be stopped. Typically when accessing slow memory systems or peripherals, wait states are applied using the HREADY signal. Refer to *AMBA Specification* for more details.

3.3.2 FastBus mode

In this mode of operation the HCLK input is used to control:

- the internal ARM9TDMI
- cache operations
- the AMBA bus interface

The FCLK input is ignored. This mode is typically used in systems with high-speed memories.

3.3.3 Asynchronous mode

This mode is typically used in systems with low-speed memory. In this mode both the HCLK and FCLK inputs are used. HCLK is used to control the AMBA bus interface. FCLK is used to control the internal ARM9TDMI processor core and any cache operations. The one restriction is that FCLK must have a higher frequency than HCLK. An example is shown in Figure 3.3.

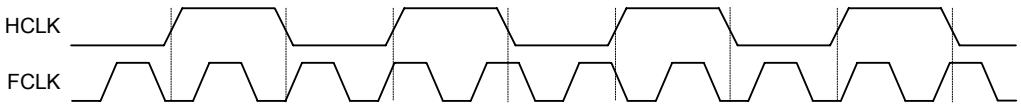


Figure 3.3 Asynchronous Clocking Mode

If the ARM940T performs an external access, the ARM940T switches to HCLK to perform the access. The delay when switching from FCLK to HCLK is a minimum of one HCLK cycle and a maximum of one and a half of HCLK cycles. An example of the clock switching is shown in Figure 3.4. When switching from HCLK to FCLK, the maximum delay is one FCLK cycle and the maximum delay is one and a half of FCLK cycles.

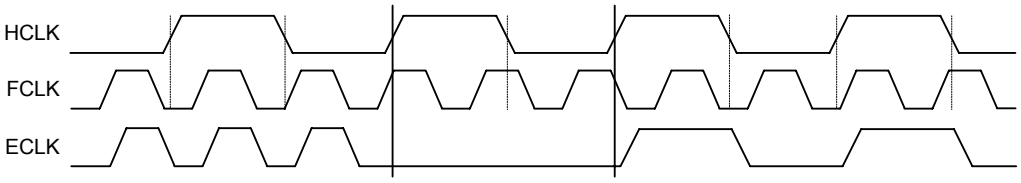


Figure 3.4 Switching from FCLK to HCLK in asynchronous mode

4 DAI & CDIF

4.1 DAI (Digital Audio Interface)

The block diagram of DAI is shown in Figure 4.1.

The TCC76x provides digital audio interface that complies with IIS (Inter-IC Sound). The DAI has five input/output pins for IIS interface, MCLK, BCLK, LRCK, DAI and DAO. All DAI input/output pins are multiplexed with GPIO pins; GPIO_B<21:25>.

The MCLK is the system clock pin that is used for CODEC system clock. In master mode, the MCLK can be generated from clock generator in which that is known as a DCLK, or fed from the outside of chip in slave mode. The DAI can process 256fs, 384fs and 512fs as a system clock. 256fs means that the system clock has 256 times of sampling frequency (fs).

The BCLK is the serial bit clock for IIS data exchange. The DAI can generate 64fs, 48fs and 32fs by dividing a system clock. The polarity of BCLK can be programmed. That is, the serial bit can be stable either rising edge of BCLK or falling edge of BCLK.

The LRCK is the frame clock for the stereo audio channel Left and Right. The frequency of LRCK is known as the "fs" – sampling frequency. Generally, for audio application such as MP3 Player and CD player, the fs can be set to 8kHz, 16kHz, 11.05kHz, 24kHz, 32kHz, 44.1kHz and 48kHz. For supporting the wide range of sampling frequency in audio application, the DCO function is very useful to generate a system clock. Refer the chapter of clock generator for detail information.

All three clocks (MCLK, BCLK, LRCK) are selectable as master or slave.

The DAI, DAO are the serial data input output pins respectively.

The DAI has two 8-word input/output buffers. It has a banked buffer structure so that one side of buffer is receiving/transmitting data while the other side of that can be read/written through the DADI_XX/DADO_XX registers. The maximum data word size is 24 bit. Data is justified to MSB of 32bits and zeros are padded to LSB.

There are two types of interrupt from IIS; transmit done interrupt, receive done interrupt. The transmit-done interrupt is generated when the 8 words are transferred successfully in the output buffer. At this interrupt, user should fill another 8 more words into the other part of the output buffer in the interrupt service routine (ISR). In this ISR routine, 8 consecutive stores of word data to the DADO registers are needed. The receive-done interrupt is generated when the 8 words are received successfully in the input buffer. At this interrupt, user should read 8 received words from the input buffer using 8 consecutive load instructions from the DADI registers.

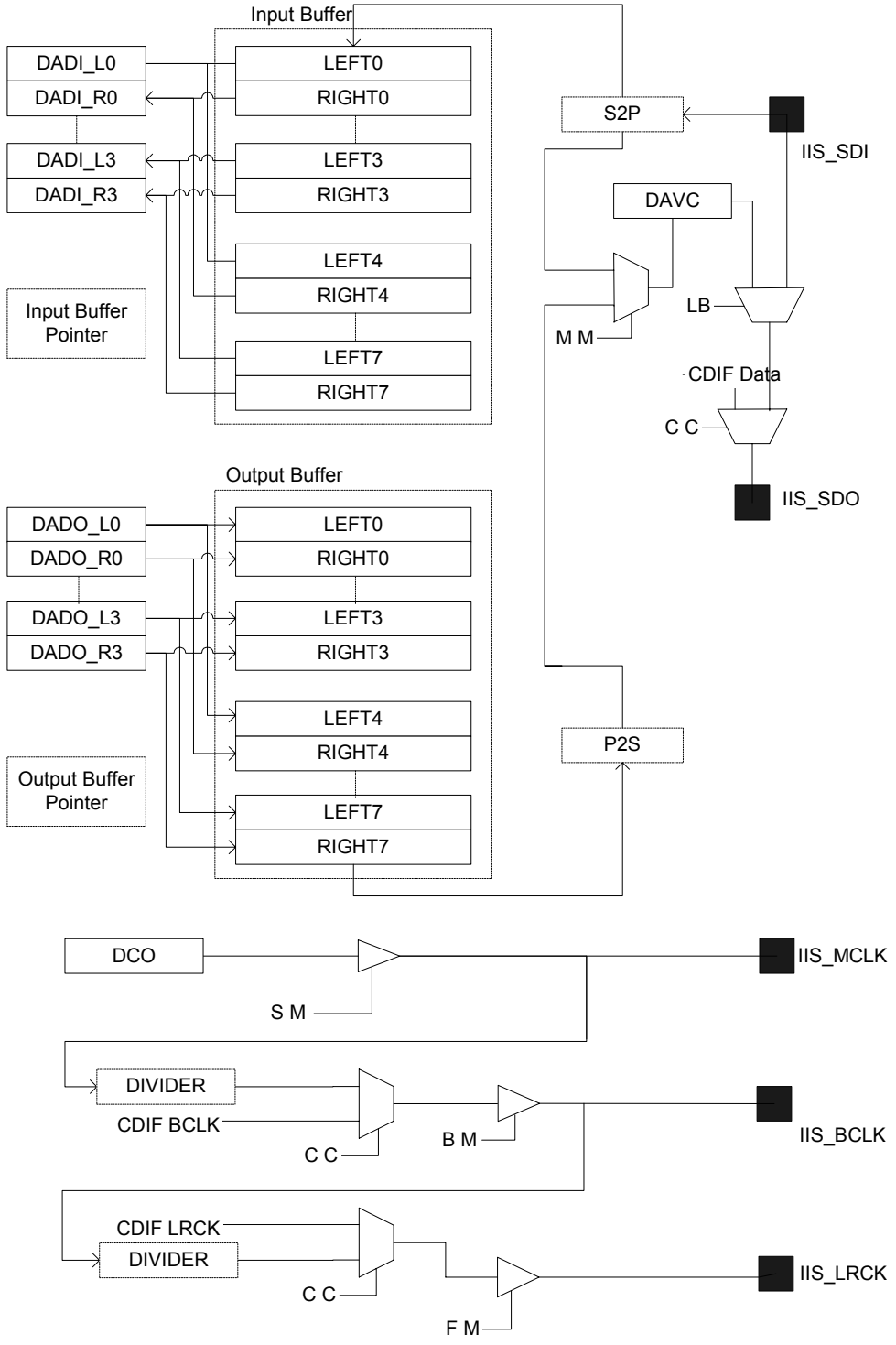
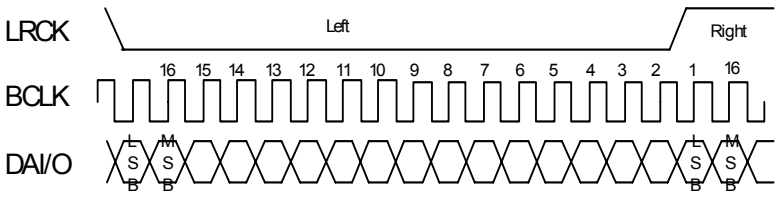
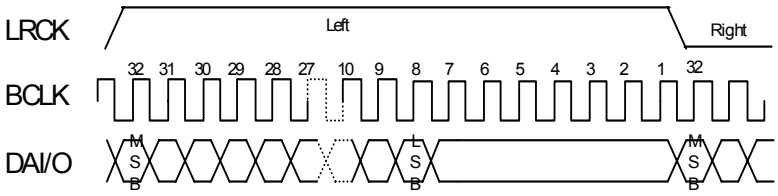


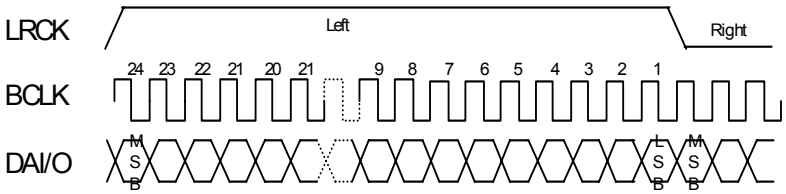
Figure 4.1 DAI Block Diagram



MD=0 (IIS mode), BP=0, BCLK = 32fs



MD=1(MSB justified mode), BP=0, BCLK=64fs



MD=1(MSB justified mode), BP=1, BCLK=48fs

Figure 4.2 DAI Bus Timing Diagram

4.2 Register Description - DAI

Table 4.1 DAI Register Map (Base Address = 0x80000000)

Name	Address	Type	Reset	Description
DADI_L0	0x00	R	-	Digital Audio Left Input Register 0
DADI_R0	0x04	R	-	Digital Audio Right Input Register 0
DADI_L1	0x08	R	-	Digital Audio Left Input Register 1
DADI_R1	0x0C	R	-	Digital Audio Right Input Register 1
DADI_L2	0x10	R	-	Digital Audio Right Input Register 2
DADI_R2	0x14	R	-	Digital Audio Right Input Register 2
DADI_L3	0x18	R	-	Digital Audio Right Input Register 3
DADI_R3	0x1C	R	-	Digital Audio Right Input Register 3
DADO_L0	0x20	R/W	-	Digital Audio Left Output Register 0
DADO_R0	0x24	R/W	-	Digital Audio Right Output Register 0
DADO_L1	0x28	R/W	-	Digital Audio Left Output Register 1
DADO_R1	0x2C	R/W	-	Digital Audio Right Output Register 1
DADO_L2	0x30	R/W	-	Digital Audio Left Output Register 2
DADO_R2	0x34	R/W	-	Digital Audio Right Output Register 2
DADO_L3	0x38	R/W	-	Digital Audio Left Output Register 3
DADO_R3	0x3C	R/W	-	Digital Audio Right Output Register 3
DAMR	0x40	R/W	0x0000	Digital Audio Mode Register
DAVC	0x44	R/W	0x0000	Digital Audio Volume Control Register

Digital Audio Mode Register (DAMR) **0x80000040**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EN	TE	RE	MD	SM	BM	FM	CC	BD<1:0>		FD<1:0>		BP	CM	MM	LB

EN [15]	DAI Master Enable
0	Disable DAI module
1	Enable DAI module

TE [14]	DAI Transmitter Enable
0	Disable DAI transmitter
1	Enable DAI transmitter

RE [13]	DAI Receiver Enable
0	Disable DAI receiver
1	Enable DAI receiver

MD [12]	DAI Bus Mode
0	Set DAI bus as IIS bus mode
1	Set DAI bus as MSB justified mode

SM [11]	DAI System Clock Master Select
0	Set that DAI system clock is come from external pin
1	Set that DAI system clock is generated by the clock generator block

- The DAI system clock in clock generator is known as DCLK. It's frequency can be determined by setting DCLKmode register.

BM [10]	DAI Bit Clock Master Select
0	Set that DAI bit clock is come from external pin
1	Set that DAI bit clock is generated by dividing DAI system clock

FM [9]	DAI Frame Clock Master Select
0	Set that DAI frame clock is come from external pin
1	Set that DAI frame clock is generated by dividing DAI bit clock

CC [8]	CDIF Clock Select
0	Disable CDIF Clock master mode
1	Enable CDIF Clock master mode

BD [7:6]	DAI Bit Clock Divider select
00	Select Div 4 (256fs->64fs)
01	Select Div 6 (384fs->64fs)
10	Select Div 8 (512fs->64fs, 384fs->48fs , 256fs->32fs)
11	Select Div16 (512fs->32fs)

FD [5:4]	DAI Frame Clock Divider select
00	Select Div 32 (32fs->fs)
01	Select Div 48 (48fs->fs)
10	Select Div 64 (64fs->fs)

- The combination of BD & FD determines that the ratio between main system clock and the sampling frequency. The multiplication between the division factor of BD and FD must be equal to this ratio.

BP [3]	DAI Bit Clock Polarity
0	Set that data is captured at positive edge of bit clock
1	Set that data is captured at negative edge of bit clock

CM [2]	CDIF Monitor Mode
0	Disable CDIF monitor mode
1	Enable CDIF monitor mode. Data bypass from CDIF

MM [1]	DAI Monitor Mode
0	Disable DAI monitor mode
1	Enable DAI monitor mode. Transmitter should be enabled. (TE = 1)

LB [0]	DAI Loop-back Mode
0	Disable DAI Loop back mode
1	Enable DAI Loop back mode

Digital Audio Volume Control Register (DAVC) **0x80000044**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												VC<3:0>			

The volume of audio output can be manipulated by this register. It has –6dB unit so the output

volume can be set from 0 dB to –90 dB as the following table.

VC [3:0]	DAI Volume control
0000	0dB
0001	-6dB
0010	-12dB
0011	-18dB
0100	-24dB
0101	-30dB
0110	-36dB
0111	-42dB
1000	-48dB
1001	-54dB
1010	-60dB
1011	-66dB
1100	-72dB
1101	-78dB
1110	-84dB
1111	-90dB

4.3 CDIF (CD-DSP Interface)

The block diagram of CDIF is illustrated in Figure 4.3.

The TCC76x provides CD-ROM interface for feasible implementation of CD-ROM application such as CD-MP3 player. The CDIF supports the industry standard IIS format and the LSB justified format that is used as the most popular format for CD-ROM interface by Sony and Samsung.

The CDIF has three pins for interface; CBCLK, CLRCK, CDAI. These are multiplexed with GPIO_B14, GPIO_B15 and GPIO_B16, respectively in the TCC76x or with GPIO_A1, GPIO_A2 and GPIO_A3 in other derivatives of the TCC76x. The CBCLK is the bit clock input pins of which frequency can be programmed by CICR for selection of 48fs and 32fs. The CLRCK is the frame clock input pin that indicates the channel of CD stereo digital audio data. The CDAI is the input data pin.

The CDIF has five registers; CDDI_0 to CDDI_3 and CICR. The CDDI_0 to the CDDI_3 are the banked read only registers for access of data input buffer. The data input buffer is composed of sixteen 32 bit wide registers of which upper 16 bit is left channel data and lower is right channel data.

The CDIF receive the serial data from CDAI pin and store the data into the buffer through the serial to parallel register. Whenever the half of buffer is filled, the receive interrupt is generated. Only the half of input buffer can be accessible through the CDDI_0 to the CDDI_3.

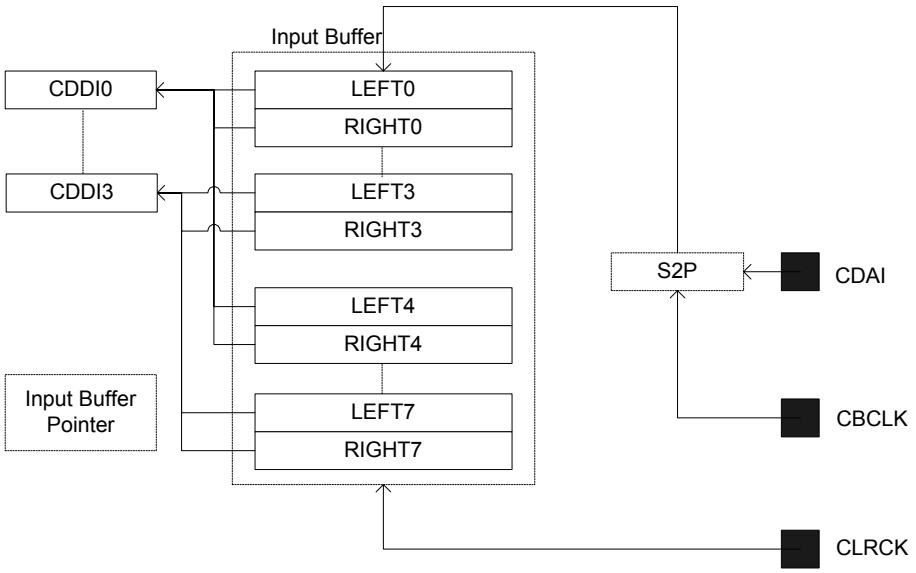
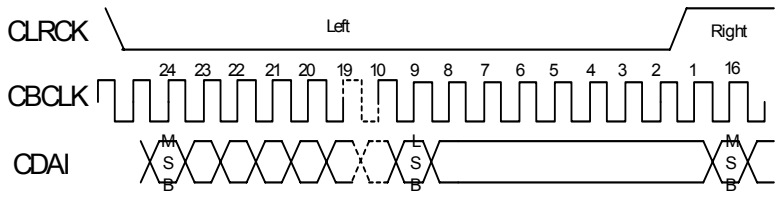
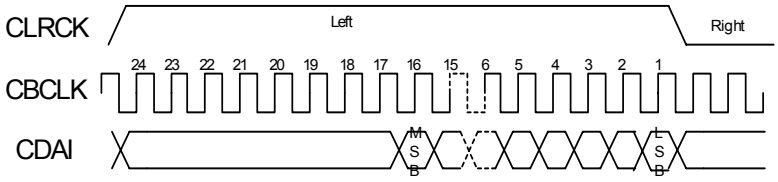


Figure 4.3 CDIF Block Diagram



MD=0 (IIS mode), BP=0, CBCLK=48fs



MD=1(LSB justified mode), BP=0, CBCLK=48fs

Figure 4.4 CDIF Bus Timing Diagram

4.4 Register Description - CDIF

Table 4.2 CDIF Register Map (Base Address = 0x80000080)

Name	Address	Type	Reset	Description
CDDI_0	0x80	R		CD Digital Audio Input Register 0
CDDI_1	0x84	R		CD Digital Audio Input Register 1
CDDI_2	0x88	R		CD Digital Audio Input Register 2
CDDI_3	0x8C	R		CD Digital Audio Input Register 3
CICR	0x90	R/W	0x0000	CD Interface Control Register

CD Data Input (CDDI0) **0x80000080**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Left Channel Data															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Right Channel Data															

CD Data Input (CDDI1) **0x80000084**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Left Channel Data															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Right Channel Data															

CD Data Input (CDDI2) **0x80000088**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Left Channel Data															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Right Channel Data															

CD Data Input (CDDI3) **0x8000008C**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Left Channel Data															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Right Channel Data															

CD Interface Control Register (CICR) **0x80000090**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								EN	Reserved			BS		MD	BP

EN [7]	CDIF Enable
0	Disable CDIF
1	Enable CDIF

BS [3:2]	CDIF Bit Clock select
00	64fs
01	32fs
10	48fs

MD [1]	Interface Mode select
0	Select IIS format
1	Select LSB justified format

BP [0]	CDIF Bit Clock Polarity
0	Set that data is captured at positive edge of bit clock
1	Set that data is captured at negative edge of bit clock

5 INTERRUPT CONTROLLER

5.1 Overview

The following figure represents the block diagram of interrupt controller. Interrupt controller can manage up to 19 interrupt sources. In the TCC76x, there are four external interrupt sources. The polarity and edge of the external interrupts are all programmable. There are four dedicated noise filter for each external interrupt source.

There are two types of interrupt in ARM940T; IRQ type, FIQ type.
Interrupt controller can select these two types for each interrupt source individually.

The WakeUp Event control logic is provided to generate fully asynchronous wakeup signal for Power Down Mode or IDLE Mode.

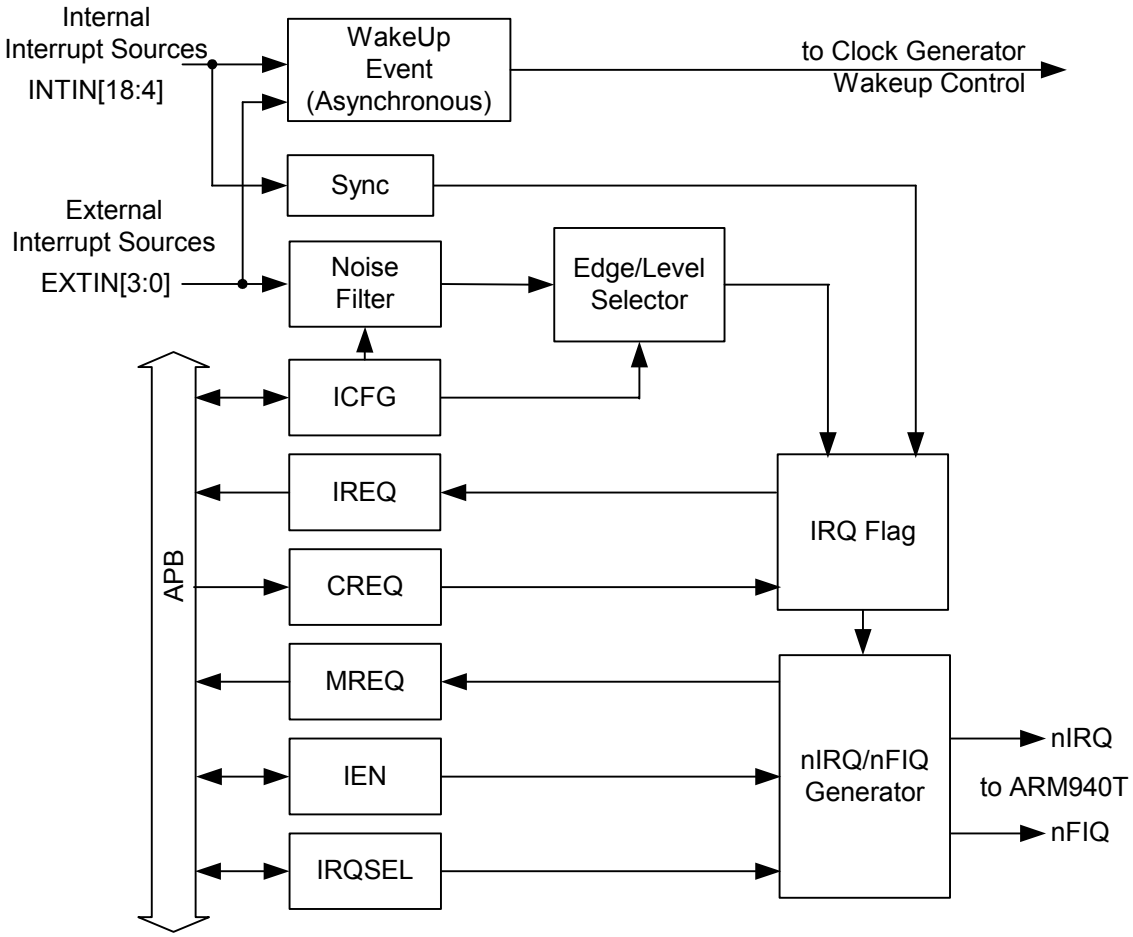


Figure 5.1 Interrupt Controller Block Diagram

5.2 Register Description

Table 5.1 Interrupt Controller Register Map (Base Address = 0x80000100)

Name	Address	Type	Reset	Description
IEN	0x00	R/W	0x00000000	Interrupt Enable Register
CREQ	0x04	W	-	Clear Interrupt Request Register
IREQ	0x08	R	0x00000000	Interrupt Request Flag Register
IRQSEL	0x0C	R/W	0x00000000	IRQ/FIQ Select Register
ICFG	0x10	R/W	0x00000000	External Interrupt Configuration Register
MREQ	0x14	R	0x00000000	Masked Interrupt Request Flag Register
TSTREQ	0x18	R/W	0x00000000	Test Mode Register (must be remained zero)
IRQ	0x20	R	-	IRQ Raw Status (IREQ & IRQSEL)
FIQ	0x24	R	-	FIQ Raw Status (~IREQ & IRQSEL)
MIRQ	0x28	R	-	Masked IRQ Status (IRQ & IEN)
MFIQ	0x2C	R	-	Masked FIQ Status (FIQ & IEN)
TMODE	0x30	R/W	0x000007C0	Trigger Mode (0: edge, 1:level)
SYNC	0x34	R/W	0x00000000	Synchronizer Control
WKUP	0x38	R/W	0x00000000	Wakeup Control

Caution)

Some peripherals have their own request flags as well as the flag in interrupt controller, so in the interrupt service routine, user should clear their own request flags in the peripherals ahead of clearing the flag in the interrupt controller.

The following pseudo code illustrates the sequence of processing the timer interrupt flags.

```
if (MREQ & TimerREQ) {                  // If timer interrupt flag is set
    if (TIREQ & Timer0) {
        process_timer0();               // Process Timer0 interrupt
        TIREQ = Timer0;                 // Clear the flag of Timer0
    }
    if (TIREQ & Timer1) {
        process_timer1();               // Process Timer0 interrupt
        TIREQ = Timer1;                 // Clear the flag of Timer1
    }
    if (TIREQ & Timer2) {
        process_timer2();               // Process Timer0 interrupt
        TIREQ = Timer2;                 // Clear the flag of Timer2
    }
    if (TIREQ & Timer3) {
        process_timer3();               // Process Timer0 interrupt
        TIREQ = Timer3;                 // Clear the flag of Timer3
    }
    if (TIREQ & Timer4) {
        process_timer4();               // Process Timer0 interrupt
        TIREQ = Timer4;                 // Clear the flag of Timer4
    }
    if (TIREQ & Timer5) {
        process_timer5();               // Process Timer0 interrupt
        TIREQ = Timer5;                 // Clear the flag of Timer5
    }
    CREQ  = TimerREQ;                   // Clear the flag of Timer
}
```

Interrupt Enable Register (IEN) 0x80000100

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved													CIF	I2C	ADC
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MEN	TC32	DMA	LCD	CDIF	UBH	GS	UB	UT	TC	I2T	I2R	E3	E2	E1	E0

MEN [15]	Master Enable
0	All interrupts are disabled.
1	Any interrupt enabled by corresponding bit[18:0] can be generated to CPU

*) Master Enable functionality is not effective if RDYIRQEN bit of Miscellaneous Configuration Register is set as "1".

Bit Field	Interrupt Request Control 1 = Interrupt enabled, 0 = Interrupt disabled
CIF [18]	Camera Interface interrupt control
I2C [17]	I2C interrupt control
ADC [16]	ADC interrupt control
RDY [15]	External Bus READY interrupt control. This bit is effective only when RDYIRQEN bit of Miscellaneous Configuration Register is set to high.
TC32 [14]	32-bit Timer interrupt control
DMA [13]	DMA interrupt control
LCD [12]	LCD interrupt control
CDIF [11]	CDIF interrupt control
UBH [10]	USB Host interrupt control
GS [9]	GSIO interrupt control
UB [8]	USB interrupt control
UT [7]	UART/IrDA interrupt control
TC [6]	Timer/Counter interrupt control
I2T [5]	I2S TX interrupt control
I2R [4]	I2S RX interrupt control
E3 [3]	External interrupt request 3 control
E2 [2]	External interrupt request 2 control
E1 [1]	External interrupt request 1 control
E0 [0]	External interrupt request 0 control

Clear Interrupt Request Register (CREQ) 0x80000104

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved													CIF	I2C	ADC
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDY	TC32	DMA	LCD	CDIF	UBH	GS	UB	UT	TC	I2T	I2R	E3	E2	E1	E0

By writing "1" to each field, the interrupt request flag of corresponding interrupt is cleared. Writing to "0" doesn't mean anything and the corresponding flag remains its previous state.

Interrupt Request Register (IREQ) 0x80000108

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved													CIF	I2C	ADC
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDY	TC32	DMA	LCD	CDIF	UBH	GS	UB	UT	TC	I2T	I2R	E3	E2	E1	E0

If each field is "1", it means that the corresponding interrupt has been requested. If each peripheral has its own request flags, it means at least one of those flags has been set.

IRQ Interrupt Select Register (IRQSEL) **0x8000010C**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved													CIF	I2C	ADC
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RDY	TC32	DMA	LCD	CDIF	UBH	GS	UB	UT	TC	I2T	I2R	E3	E2	E1	E0

If each field is "1", it means that the corresponding interrupt is considered as IRQ interrupt, if each field is '0' it means that its interrupt is considered as FIQ interrupt. Refer to chapter 3 for more information about IRQ / FIQ interrupts.

External Interrupt Configuration Register (ICFG) **0x80000110**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FE3	DTYPE3		FT3	FE2	DTYPE2		FT2	FE1	DTYPE1		FT1	FE0	DTYPE0		FT0

FE3~FE0	Filter Enable
0	Noise filter is enabled (in case of DTYPEn != 3)
1	Noise filter is disabled (in case of DTYPEn != 3)

If DTYPEn == 3, noise filter is always enabled, and this field sets which level generates the interrupt. If it is set to 1, level high triggers interrupt, and if it is set to 0, level low triggers interrupt.

DTYPE3~0	Detection Type
0	Falling edge triggered external interrupt
1	Rising edge triggered external interrupt
2	Both edge triggered external interrupt
3	Level high / low triggered external interrupt FEn field determines which level triggers the interrupt. If FEn == 1, level high triggers the interrupt and FEn == 0, level low triggers the interrupt.

FT3~FT0	Filter Type
X	Reserved

Following is the summary of all above fields.

Table 5.2 Summary of External Interrupt Configuration

FEn, DTYPEn	Triggering	Noise Filter
000	Set falling edge triggered	Filter Enabled
001	Set rising edge triggered	Filter Enabled
010	Set both edge triggered	Filter Enabled
011	Set low level triggered	Filter Enabled
100	Set falling edge triggered	Filter disabled
101	Set rising edge triggered	Filter disabled
110	Set both edge triggered	Filter disabled
111	Set high level triggered	Filter Enabled

"011" and "111" are recommended to avoid conflicts caused by the different interpretation between Wakup Event logic and Interrupt Generation logic. (Refer to "Wakeup Control Register" description).

Masked Interrupt Request Register (MREQ) **0x80000114**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved													CIF	I2C	ADC
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RDY	TC32	DMA	LCD	CDIF	UBH	GS	UB	UT	TC	I2T	I2R	E3	E2	E1	E0

Same meaning as IREQ except that it represents only that of the enabled interrupts. Only the flags of enabled interrupts can be checked by this register. It is recommended that use MREQ register instead of IREQ in the interrupt handler routine.

Test Mode Register (TSTREQ) **0x80000118**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved													CIF	I2C	ADC
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RDY	TC32	DMA	LCD	CDIF	UBH	GS	UB	UT	TC	I2T	I2R	Reserved			

This register can be used to generate an interrupt by writing 1 at the corresponding bit of the internal interrupt source. This register is for testing purpose only. It must be remained zero during normal operation.

IRQ Raw Status Register (IRQ) **0x80000120**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved													CIF	I2C	ADC
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RDY	TC32	DMA	LCD	CDIF	UBH	GS	UB	UT	TC	I2T	I2R	E3	E2	E1	E0

This register reflects IREQ bits selected when the corresponding IRQSEL bit is low (IREQ & IRQSEL)

FIQ Raw Status Register (FIQ) **0x80000124**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved													CIF	I2C	ADC
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RDY	TC32	DMA	LCD	CDIF	UBH	GS	UB	UT	TC	I2T	I2R	E3	E2	E1	E0

This register reflects IREQ bits selected when corresponding IRQSEL bit is high (~IREQ & IRQSEL).

Masked IRQ Raw Status Register (MIRQ) **0x80000128**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved													CIF	I2C	ADC
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RDY	TC32	DMA	LCD	CDIF	UBH	GS	UB	UT	TC	I2T	I2R	E3	E2	E1	E0

MIRQ = IRQ & IEN

Masked FIQ Raw Status Register (MFIQ) **0x8000012C**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved													CIF	I2C	ADC
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RDY	TC32	DMA	LCD	CDIF	UBH	GS	UB	UT	TC	I2T	I2R	E3	E2	E1	E0

MFIQ = FIQ & IEN

Trigger Mode Register (TMODE) **0x80000130**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved													CIF	I2C	ADC
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RDY	TC32	DMA	LCD	CDIF	UBH	GS	UB	UT	TC	I2T	I2R	Reserved			

This register selects trigger mode (0: edge, 1:level) for each internal interrupt source.

Synchronization Control Register (SYNC) **0x80000134**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved													CIF	I2C	ADC
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RDY	TC32	DMA	LCD	CDIF	UBH	GS	UB	UT	TC	I2T	I2R	Reserved			

By default, all internal interrupt source lines are synchronized to HCLK. This register disables synchronization registers (0: sync enabled, 1:sync disabled). Do not disable synchronization if an interrupt source is asynchronous to HCLK

Wakeup Control Register (WKUP) **0x80000138**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved													CIF	I2C	ADC
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RDY	TC32	DMA	LCD	CDIF	UBH	GS	UB	UT	TC	I2T	I2R	E3	E2	E1	E0

This register enables each interrupt source to be used as an asynchronous wakup event for Power Down or IDLE mode. By default, all interrupt source lines are used for system wakeup events in power down mode. (0: enabled, 1: disabled). Appropriate bits must be enabled before the system enters power down mode (clock stop mode). Otherwise, system cannot wakeup. Refer to section "Power Down Mode" and "IDLE mode" in Chapter "Clock Generator".

Before enable E3 ~ E0 (external interrupt pins), FE3 ~ FE0 bits of ICFG register must be changed to control the polarity of each external interrupt pin. In wakup event control logic, FE3 ~ FE0 bits of ICFG are used as polarity control bits for the external interrupt pins ("0" indicates active low, "1" indicates active high). Watch out for the different interpretation of ICFG register between two logics.

Table 5.3 ICFG Usage for WakeUp Event

FEn, DTYPEn of ICFG Register	Interrupt Generation Logic		WakeUp Event Control Logic
	Triggering	Noise Filter	
000	Falling edge triggered	Filter enabled	Low level trigger, filter disabled
001	Rising edge triggered	Filter enabled	
010	Both edge triggered	Filter enabled	
011	Low level triggered	Filter enabled	
100	Falling edge triggered	Filter disabled	High level trigger, filter disabled
101	Rising edge triggered	Filter disabled	
110	Both edge triggered	Filter disabled	
111	High level triggered	Filter enabled	

As long as the HCLK is alive, any interrupt source lines with the corresponding Interrupt Enable bit active can wakeup the system from Power Down or IDLE Mode. (The TCC76x Clock Generator also accepts nIRQ and nFIQ for wakeup). But when the HCLK is stopped, the Interrupt Controller is stopped also, and no event output is generated to the clock generation logic. Thus, the system can never be woke up if Wakup Control Register is not used at all.
Wakeup Control Register must be used in Power Down or IDLE Mode if the HCLK is to be disabled.
It is recommended to disable Interrupt Enable Register if Wakeup Control Register bits are used.

6 TIMER / COUNTER

6.1 Overview

The TCC76x has four 16bit and two 20bit timer/counters. Each timer counter has three registers for basic operation modes. Refer to register description table for details. When operating in counter modes, External interrupt pin is used as counting clock for that counter.

The main clock frequency of timer counter can be configured by setting TCLK frequency. (Refer to Clock generator block) With the 12bit internal basic counter, the timer counter can generate various intervals from microseconds to seconds unit.

In addition to TCC72x compatible timers/counters, the TCC76x provides a 32-bit general-purpose up counter. (Refer to Figure 6.3).

The following figure represents the block diagram of timer/counter.

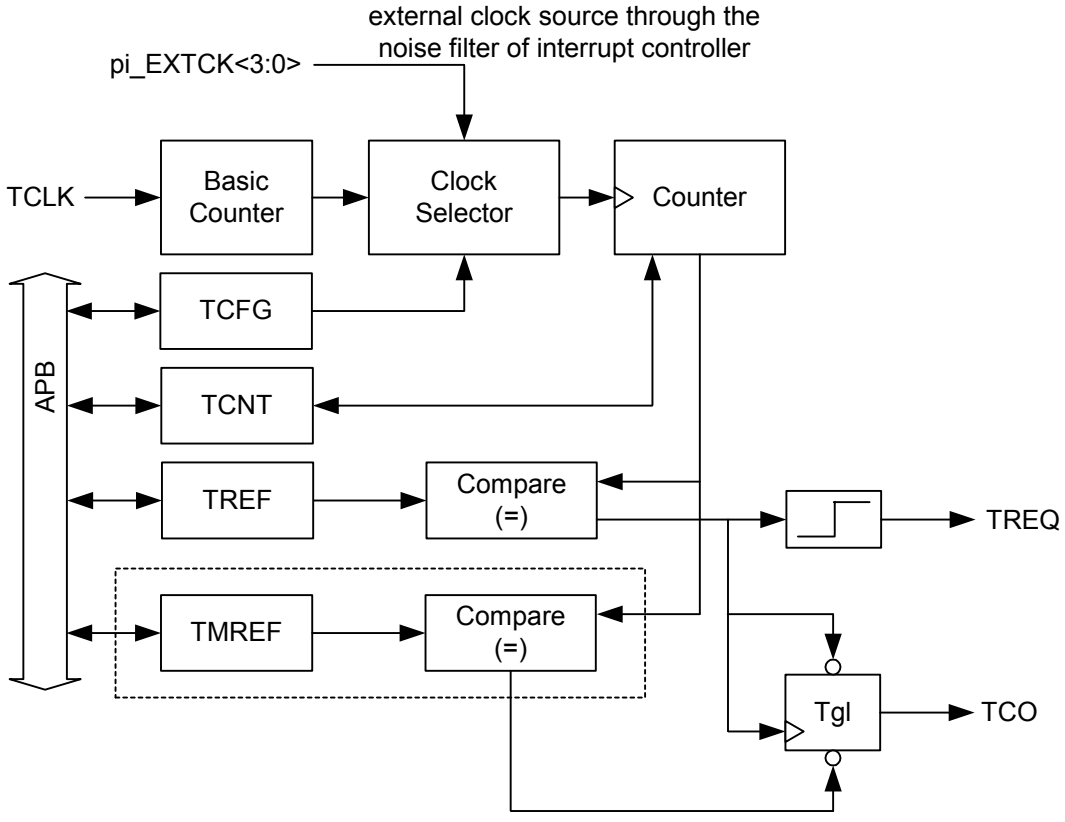


Figure 6.1 Timer Counter Block Diagram

The following table explains the registers of each timer counter. The address of each timer counter is 16bytes aligned. The base address of timer counter is 0x80000200.

The number n represents for each timer/counter. In case of timer/counter 4, 5 (that is n = 4 or 5) the TREF, TCNT register has 20bit resolution. It can be used for generating long time of event.

6.2 Register Description

Table 6.1 Timer/Counter Register Map (Base Address = 0x80000200)

Name	Address	Type	Reset	Description
TCFG0	0x0000	R/W	0x00	Timer/Counter 0 Configuration Register
TCNT0	0x0004	R/W	0x0000	Timer/Counter 0 Counter Register
TREF0	0x0008	R/W	0xFFFF	Timer/Counter 0 Reference Register
TMREF0	0x000C	R/W	0x0000	Timer/Counter 0 Middle Reference Register
TCFG1	0x0010	R/W	0x00	Timer/Counter 1 Configuration Register
TCNT1	0x0014	R/W	0x0000	Timer/Counter 1 Counter Register
TREF1	0x0018	R/W	0xFFFF	Timer/Counter 1 Reference Register
TMREF1	0x001C	R/W	0x0000	Timer/Counter 1 Middle Reference Register
TCFG2	0x0020	R/W	0x00	Timer/Counter 2 Configuration Register
TCNT2	0x0024	R/W	0x0000	Timer/Counter 2 Counter Register
TREF2	0x0028	R/W	0xFFFF	Timer/Counter 2 Reference Register
TMREF2	0x002C	R/W	0x0000	Timer/Counter 2 Middle Reference Register
TCFG3	0x0030	R/W	0x00	Timer/Counter 3 Configuration Register
TCNT3	0x0034	R/W	0x0000	Timer/Counter 3 Counter Register
TREF3	0x0038	R/W	0xFFFF	Timer/Counter 3 Reference Register
TMREF3	0x003C	R/W	0x0000	Timer/Counter 3 Middle Reference Register
TCFG4	0x0040	R/W	0x00	Timer/Counter 4 Configuration Register
TCNT4	0x0044	R/W	0x00000	Timer/Counter 4 Counter Register
TREF4	0x0048	R/W	0xFFFFF	Timer/Counter 4 Reference Register
TCFG5	0x0050	R/W	0x00	Timer/Counter 5 Configuration Register
TCNT5	0x0054	R/W	0x00000	Timer/Counter 5 Counter Register
TREF5	0x0058	R/W	0xFFFFF	Timer/Counter 5 Reference Register
TIREQ	0x0060	R/W	0x0000	Timer/Counter n Interrupt Request Register
TWDCFG	0x0070	R/W	0x0000	Watchdog Timer Configuration Register
TWDCLR	0x0074	W	-	Watchdog Timer Clear Register
TC32EN	0x0080	R/W	0x00007FFF	32-bit Counter Enable / Pre-scale Value
TC32LDV	0x0084	R/W	0x00000000	32-bit Counter Load Value
TC32CMP0	0x0088	R/W	0x00000000	32-bit Counter Match Value 0
TC32CMP1	0x008C	R/W	0x00000000	32-bit Counter Match Value 1
TC32PCNT	0x0090	R/W	-	32-bit Counter Current Value (pre-scale counter)
TC32MCNT	0x0094	R/W	-	32-bit Counter Current Value (main counter)
TC32IRQ	0x0098	R/W	0x0000----	32-bit Counter Interrupt Control

Timer/Counter n Configuration Register (TCFGn) 0x80000200 + (0x10 * n)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0							CC	POL	TCKSEL			IEN	PWM	CON	EN

CC [8]	Clear Count
0	TCNTn is not cleared.
1	TCNTn is cleared to zero.

POL [7]	TCK Polarity
0	TCNTn is incremented at rising edge of the selected counting clock
1	TCNTn is incremented at falling edge of the selected counting clock

TCKSEL [6:4]	TCK Select
k = 0 ~ 4	TCK is internally generated from divider circuit. It is driven by TCLK, and this value determines the division factor of this circuit. Division factor is $2^{(k+1)}$.
k = 5, 6	TCK is internally generated from divider circuit. It is driven by TCLK, and this value determines the division factor of this circuit. Division factor is 2^{2k}
k = 7	TCK is the external pin shared by external interrupt signal. In the TCC76x, there are 4 external pins for this purpose, so this configuration is valid only for timer/counter 3 ~ 0. (not for timer/counter 5, 4)

IEN [3]	Interrupt Enable
1	Enable Timer/Counter interrupt
0	Disable Timer/Counter interrupt

PWM [2]	PWM Mode Enable
1	Enable PWM mode Timer/Counter output is changed at every time the TCNTn is equal to TREFn and TMREFn value. It can be used to generate PWM waveform, by changing TMREFn while fixing TREFn. (where, TREFn > TMREFn)
0	Disable PWM mode Timer/Counter output can be changed only when the TCNTn is equal to TREFn. It can be used to generate a rectangular pulse of variable frequency.

The output of 6 Timer/Counters can be monitored through GPIO_A ports.
Refer to GPIO chapter for more information.

CON [1]	Continue Counting
0	When the TCNTn is reached to TREFn, TCNTn restarts counting from 0 at the next pulse of selected clock source.
1	The TCNTn continues counting from the TREFn.

EN [0]	Timer/Counter Enable
1	Timer counter is enabled.

Following figure illustrates the basic behavior of timer / counter.

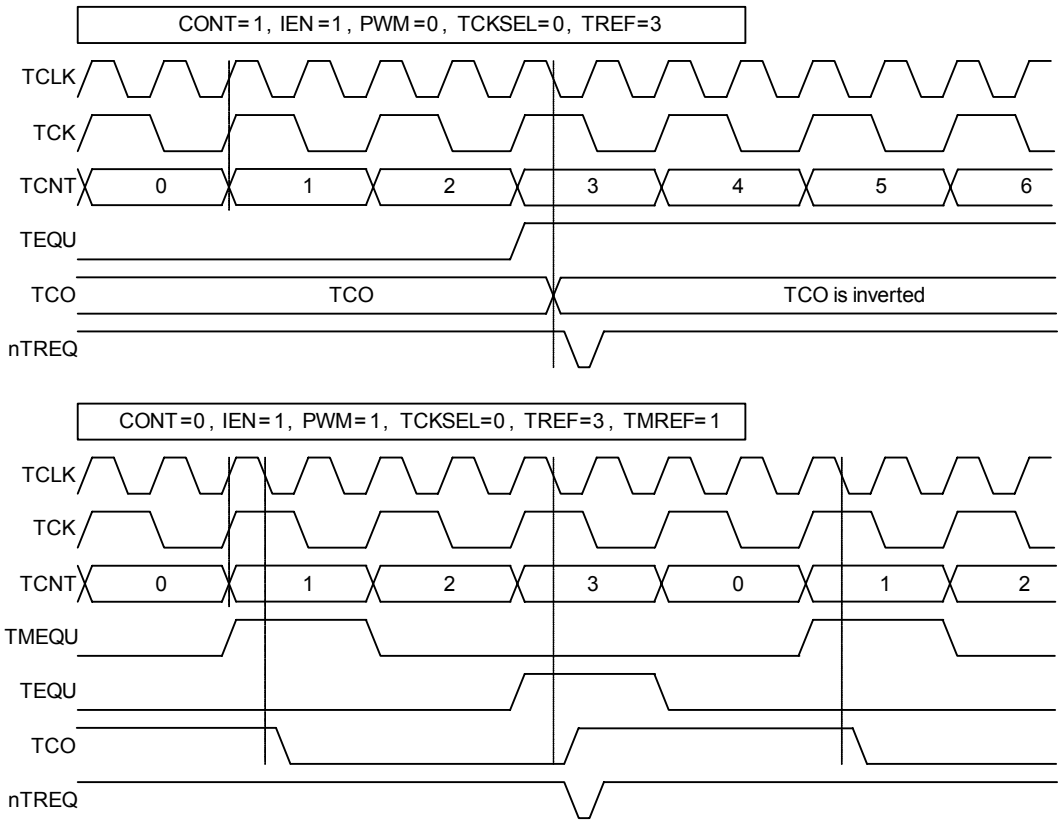


Figure 6.2 Timing diagram of timer/counter

Timer/Counter n Counting Register (TCNTn) 0x80000204 + (0x10 * n)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0												TCNTn[19:16]			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TCNTn[15:0]															

TCNTn is increased by 1 at every pulse of selected clock source. TCNTn can be set to any value by writing to this register. In case of timer 4 and timer 5, it has 20 bits, otherwise it has 16 bits.

Timer/Counter n Counting Reference Register (TREFn) 0x80000208 + (0x10 * n)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0												TREFn[19:16]			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TREFn[15:0]															

When TCNTn is reached at TREFn and the CON flag of TCFGn register is set to 1, the TCNTn is cleared to 0 at the next pulse of selected clock source. According to the TCFGn settings, various kinds of operations may be done. In case of timer 4 and timer 5, it has 20 bit, otherwise it has 16 bit.

Timer/Counter n Middle Reference Register (TMREFn) 0x8000020C + (0x10 * n)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0												TMREFn[19:16]			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMREFn[15:0]															

When TCNTn is reached at TMREFn and the PWM flag of TCFGn register is set to 1, the timer output of TCOn is cleared to 0 at the negative edge of that pulse of selected clock source. The TCOn is set to 1 when the TCNTn is reached at TREFn. (refer Figure 6.1). So you can generate PWM signal by modifying TMREFn between 0 ~ (TREFn-1). In case of timer 4 and timer 5, it has 20 bit, otherwise it has 16 bit.

Timer/Counter Interrupt Request Register (TIREQ) 0x80000260

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	TWF	TF5	TF4	TF3	TF2	TF1	TF0	0	TWI	TI5	TI4	TI3	TI2	TI1	TI0

TWF [14]	Watchdog Timer Flag
1	Watchdog timer has reached to its reference value.

TFn [13:8]	Timer/Counter n Flag
1	Timer/counter n has reached to its reference value.

TWI [6]	Type	Watchdog Timer Interrupt Request Flag
1	Read	Watchdog timer has generated its interrupt.
1	Write	Watchdog timer interrupt is cleared.

TIn [5:0]	Type	Timer/Counter n Interrupt Request Flag
1	Read	Timer/counter n has generated its interrupt.
1	Write	Timer/counter n interrupt flag is cleared.

If a timer n has reached its reference value, the TFn is set. (bit n represents for Timer n). If its interrupt request is enabled by set bit 3 of TCFGn register, then the TIn is set. If the TC bit of IEN register is set, the timer interrupt is really generated and this TIREQ register can be used to determine which timer has requested the interrupt. After checking these flags, user can clear these TFn and TIn field by writing "1" to corresponding TFn or TIn bit field.

Watchdog Timer Configuration Register (TWDCFG) **0x80000270**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0									TCKSEL			IEN	0	ISEL	EN

Watchdog timer is used for the system not to be stuck by generating a reset pulse or interrupt automatically when the watchdog timer counter overflows to zero.
The programmer must clear the watchdog counter before it overflows by writing any value to TWDCLR register. The duration can be chosen by selecting TCKSEL field appropriately.

TCKSEL [6:4]	TCK Select
k = 0 ~ 3	Undefined. Should not be used.
k = 4	TCK is internally generated from divider circuit. It is driven by TCLK, and this value determines the division factor of this circuit. Division factor is 2^5.
k = 5, 6	TCK is internally generated from divider circuit. It is driven by TCLK, and this value determines the division factor of this circuit. Division factor is 2^{2k}
k = 7	Undefined. Should not be used.

IEN [3]	Interrupt Enable
1	Watchdog Timer Interrupt is enabled. This field is valid only if RST field is set to 0.

ISEL [1]	Interrupt Select
0	Watchdog timer generates the reset signal when it reaches to the reference value, the reset signal is applied to every component in the chip.
1	Watchdog timer does not generate reset signal although it reaches to the reference value, and it continue counting from 0.

EN [0]	Watchdog Timer Enable
1	Watchdog timer is enabled. If the watchdog timer is disabled, its counter goes to 0xE0, so when it is first enabled, user must clear the counter by writing to TWDCLR register.

Watchdog Timer Clear Register (TWDCLR) **0x80000274**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
any value															

The watchdog timer counter can be cleared to 0 by writing any value to this register. If it is not cleared before it overflows, the watchdog timer generate reset signal to the entire component of chip.

As illustrated in the figure below, TC32 consists of a pre-scale counter, main counter and two comparators. The pre-scale counter is a simple 24-bit up-counter which always counts from zero to PRESCALE value programmed in TC32EN register. The 32-bit main counter is incremented only when the prescale counter reaches PRESCALE value.
The clock input of TC32 module can be either XTIN (default) or XIN. Refer to Clock Generator description (XTTC32 bit of PWDCTL register).

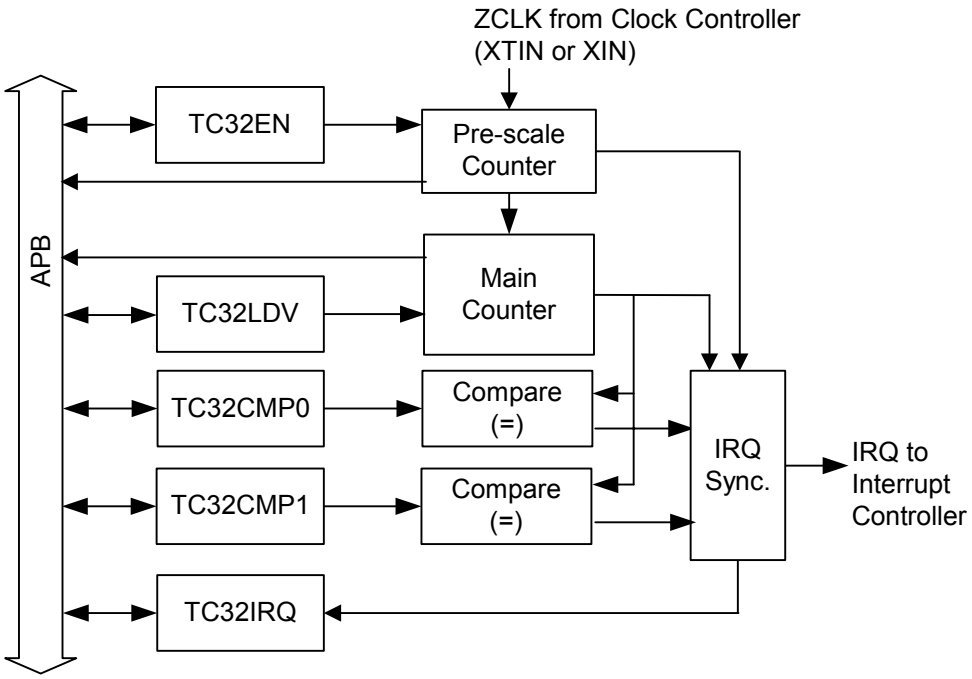


Figure 6.3 32-bit Counter Block Diagram

Possible counter modes are described in the table below.

Table 6.2 TC32 Count Mode

Mode	TC32EN Register Bits			Main Counter Operation	
	LOADZERO	LDM1	LDM0	Start Count Value	End Count Value
0	0	0	0	LOADVAL	0xFFFFFFFF
1	0	0	1	LOADVAL	CMP0 (if LOADVAL < CMP0)
2	0	1	0	LOADVAL	CMP1 (if LOADVAL < CMP1)
3	0	1	1	LOADVAL	CMP0 (if LOADVAL < CMP0 ≤ CMP1) or CMP1 (if LOADVAL < CMP1 ≤ CMP0)
4	1	0	0	0	LOADVAL – 1
5	1	0	1	0	CMP0 (if LOADVAL > CMP0)
6	1	1	0	0	CMP1 (if LOADVAL > CMP1)
7	1	1	1	0	CMP0 (if LOADVAL > CMP1 ≥ CMP0) or CMP1 (if LOADVAL > CMP0 ≥ CMP1)

Refer to register descriptions below for CMP0, CMP1 and LOADVAL.
Mode0 can be used as 1Hz counter mode, if PRESCALE = 0x007FFF, STOPMODE = 0, ZCLK = XTIN(32.768kHz)

TC32 Enable / Pre-scale Value Register (TC32EN) 0x80000280

Bit	Name	Default	R/W	Description
31:30	Reserved	0	R	
29	LDM1	0	R/W	Re-load counter when the counter value matched with CMP1. LOADZERO bit below selects the couter load(start) value.
28	LDM0	0	R/W	Re-load counter when the counter value matched with CMP0 LOADZERO bit below selects the couter load(start) value.
27	Reserved	0	R	
26	STOPMODE	0	R/W	0 = Free Running Mode, 1 = Stop Mode.
25	LOADZERO	0	R/W	By default, counter starts from LOADVAL. When this bit is enabled (1), the counter is forced to count from “0” to “LOADVAL – 1”.
24	ENABLE	0	R/W	Counter Enable
23:0	PRESCALE	0x007FFF	R/W	Pre-scale counter load value. The pre-scale counter always runs from “0” up to PRESCALE. The default value is for 1Hz counter when ZCLK = XTIN (32.768kHz).

TC32 Load Value Register (TC32LDV) 0x80000284

Bit	Name	Default	R/W	Description
31: 0	LOADVAL	0x00000000	R/W	Counter Load Value.

The counter is restarted whenenver one of the TC32En and TC32LDV is written.

TC32 Match Value 0 Register (TC32CMP0) 0x80000288

Bit	Name	Default	R/W	Description
31: 0	CMP0	0x00000000	R/W	Counter Match Value

TC32 Match Value 1 Register (TC32CMP1) 0x8000028C

Bit	Name	Default	R/W	Description
31: 0	CMP1	0x00000000	R/W	Counter Match Value

TC32 Pre-scale Counter Current Value Register (TC32PCNT) 0x80000290

Bit	Name	Default	R/W	Description
31:24	Reserved	0x00	R	
23: 0	PCNT	0x000000	R	Pre-scale counter current value. The AHB system clock must be three times faster than the frequency of ZCLK to read valid value.

TC32 Main Counter Current Value Register (TC32MCNT) 0x80000294

Bit	Name	Default	R/W	Description
31: 0	MCNT	0x00000000	R	Main counter current value. When RSYNC is enabled, the AHB system clock must be faster than the frequency calculated below. (ZCLK frequency) / (PRESCALE + 1) * 3

TC32 Interrupt Control Register (TC32IRQ) 0x80000298

Bit	Name	Default	R/W	Description
31	IRQCLR	0	R/W	Interrupt Clear Control. When this bit is 0, interrupt status bits (IRQRSTAT) are cleared by reading this register. When this bit is set, IRQSTAT bits are cleared only if written with non-zero value.
30	RSYNC	0	R/W	Synchronization control for Counter Current Value Registers (TC32PCNT and TC32MCNT). 0 = Enable, 1 = Disable.
29:24	BITSEL	0x00	R/W	Counter bit selection value for interrupt generation. Any one of the counter bits {MCNT[31:0], PCNT[23:0]} selected by BITSEL is used to generate an interrupt. 0x00 ~ 0x17 : PCNT[0] ~ PCNT[23] 0x18 ~ 0x38: MCNT[0] ~ MCNT[31]

23:21	Reserved	0	R/W	
20	IRQEN[4]	0	R/W	Enable Interrupt at the rising edge of a counter bit selected by BITSEL.
19	IRQEN[3]	0	R/W	Enable Interrupt at the end of pre-scale count
18	IRQEN[2]	0	R/W	Enable Interrupt at the end of count
17	IRQEN[1]	0	R/W	Enable Interrupt when the counter value matched with CMP1
16	IRQEN[0]	0	R/W	Enable Interrupt when the counter value matched with CMP0
15:13	Reserved	0	R/W	
12:8	IRQRSTAT	0x00	R/W	Interrupt Raw Status. Refer to the description for IRQEN above.
7:5	Reserved	0	R/W	
4:0	IRQMSTAT	0x00	R/W	Masked Interrupt Status = IRQRSTAT & IRQEN

7 GPIO PORT

7.1 Overview

The TCC76x has a lot of general purpose I/Os that can be programmed by setting internal registers. All I/Os are set to input mode at reset. Except for GPIO_B[29:26] (USB transceiver I/Os), all pins named with GPIO have the following features.

- Programmable internal pull-up resistor
- Programmable drive strength control (4/6/8/12mA) for output mode
- Programmable I/O direction control

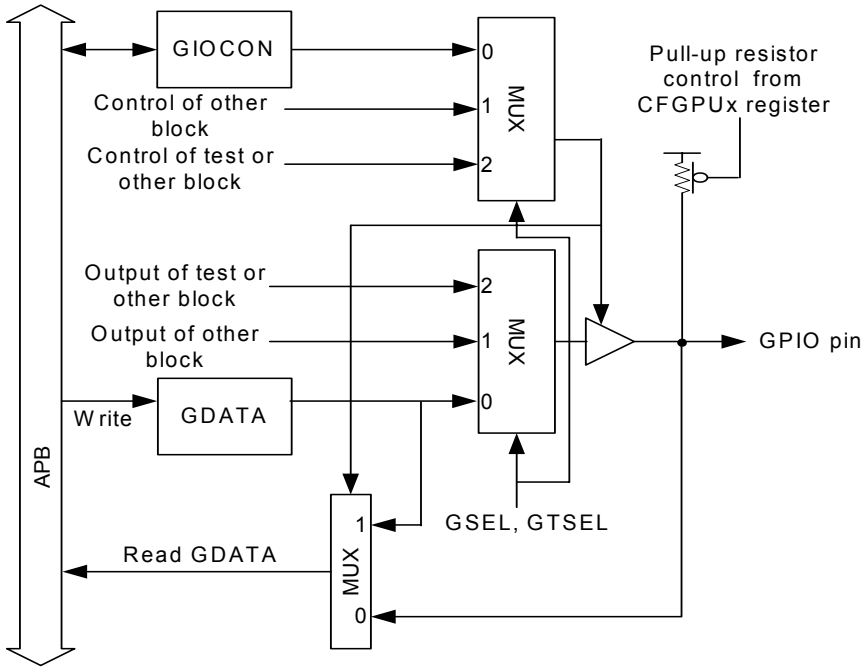


Figure 7.1 GPIO Block Diagram

The I/O mode can be set by the state of GIOCON register.
If a bit of GIOCON register is 1, the corresponding GPIO pin has come to output mode, and if 0, which is the default state of GIOCON register, the corresponding GPIO pin is set to input mode.

If GPIO pin is set to input mode, GPIO pin's state can be fed to CPU by reading GDATA register and when output mode, GPIO pin's state can be controlled by the state of the corresponding bit of GDATA register.
If GDATA register is read when the mode is output mode, the value that CPU gets is the one that CPU has written before.

In the TCC76x, there are various kinds of peripherals that generate its own control signals. These peripherals can occupy the dedicated GPIO pins. This option is controlled by the state of the GSEL and GTSEL register.
If a bit of these GSEL or GTSEL is 1, the corresponding GPIO pin is entered to other function mode, so used by other peripherals not by GPIO block. The direction control method of GPIO pins in the other function mode is determined case by case. One of them follows the normal direction control method using GIOCON register, the other method uses a its own direction control signals.

For drive strength and internal pull-up resistor control, refer to section 12.2 Miscellaneous Register Description.

7.2 Register Description

Table 7.1 GPIO Register Map (Base Address = 0x80000300)

Name	Addr	Type	Reset	Description
GDATA_A	0x00	R/W	0xFFFFFFFF	GPIO_A Data Register
GIOCON_A	0x04	R/W	0x00000000	GPIO_A Direction Control Register
GSEL_A	0x08	R/W	0x00000000	GPIO_A Function Select Register 1
GTSEL_A	0x0C	R/W	0x00000000	GPIO_A Function Select Register 2
GDATA_B	0x10	R/W	0x3FFFFFFF	GPIO_B Data Register
GIOCON_B	0x14	R/W	0x000000FF	GPIO_B Direction Control Register
GSEL_B	0x18	R/W	0x3C0000FF	GPIO_B Function Select Register 1
GTSEL_B	0x1C	R/W	0x00000000	GPIO_B Function Select Register 2
GDATA_C	0x20	R/W	0xFFFF	GPIO_C Data Register
GIOCON_C	0x24	R/W	0x0000	GPIO_C Direction Control Register
GDATA_D	0x30	R/W	0x007FFF	GPIO_D Data Register
GIOCON_D	0x34	R/W	0x000000	GPIO_D Direction Control Register

Reset values are valid only for the TCC761. All the other derivatives of the TCC76x may have different reset values. For those bits without external pins, reset values should not be changed. Read-modify-write sequence is recommended for all the GPIO registers

Special GPIO pins

A special GPIO register (MCFG register) exists in Memory controller. It can control MODE0(READY) pin and SD_CLK pin as general purpose input and output pin each other.
That is, by setting appropriate field of MCFG register, user can monitor the state of MODE0(READY) pin and can manipulate the state of SD_CLK pin as low or high.
Refer to Chapter 15 for more information of MCFG register.

GPIO_A Data Register (GDATA_A) 0x80000300

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Data for GPIO_A[31:16] pin															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Data for GPIO_A[15:0] pin															

If a certain GPIO_A pin is set to output mode and act as GPIO, the corresponding bit of this register controls the status of GPIO_A pin; Low or High. If it is set to input mode and act as GPIO, the corresponding bit represents the status of GPIO_A pin; Low or High.

GPIO_A Direction Control Register (GIOCON_A) 0x80000304

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Direction control for GPIO_A[31:16] pin															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Direction control for GPIO_A[15:0] pin															

If a bit is set to 1, the corresponding GPIO_A pin is set to output mode. If set to 0, the corresponding GPIO_A pin is set to input mode.

GPIO_A Function Select Register (GSEL_A) **0x80000308**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PD[15:0]															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0					GS2[2:0]			-	GS1[2:0]			-	GS0[2:0]		

If a bit is set to 1, the corresponding GPIO_A pin is used by the other dedicated peripherals. The dedicated peripherals for these GPIO_A pins are LCD controller, and three of four GSIO ports.

PD[15:0]	GPIO_A[31:16] Function Select
0	GPIO_A[31:16] pin is working as Normal GPIO Function
if bit n = 1	GPIO_A[n+16] : Pixel Data[n] of LCD block

*These fields are valid only in TCC761.

GSn[2:0]	GPIO_A[10:8], GPIO_A[6:4], GPIO_A[2:0] Function
0	GPIO_A[10:8], GPIO_A[6:4], GPIO_A[2:0] pin is working as Normal GPIO Function
GS2[2] = 1 GS2[1] = 1 GS2[0] = 1	GPIO_A[10] : FRM signal of GSIO2 block GPIO_A[9] : SCK signal of GSIO2 block GPIO_A[8] : SDO signal of GSIO2 block
GS1[2] = 1 GS1[1] = 1 GS1[0] = 1	GPIO_A[6] : FRM signal of GSIO1 block GPIO_A[5] : SCK signal of GSIO1 block GPIO_A[4] : SDO signal of GSIO1 block
GS0[2] = 1 GS0[1] = 1 GS0[0] = 1	GPIO_A[2] : FRM signal of GSIO0 block GPIO_A[1] : SCK signal of GSIO0 block GPIO_A[0] : SDO signal of GSIO0 block

SDI signal for GSIO2, GSIO1, GSIO0 block is always fed through GSIO_A[11], GSIO_A[7], GSIO_A[3] pin regardless of these GS[2:0] bit. But to use GSIO, these pins must be set to input mode ahead.

GPIO_A Test Select Register (GTSEL_A) **0x8000030C**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0				TC2	EX2CLK		TC5	TC1	0		TC4	TC0	0		TC3

If a bit is set to 1, and the corresponding bit of GSEL_A is 0, GPIO_A pin is used by the other dedicated peripherals. It is used to set the output of timer

TC5 ~ TC0	GPIO_A[11,8,7,4,3,0] Function Select
0	GPIO_A[11,8,7,4,3,0] pin is working as Normal GPIO Function
1	GPIO_A[11,8,7,4,3,0] is the output of six timer/counters

*) These fields are valid only if the corresponding bit of GSEL_A is set to 0

GPIO_B Data Register (GDATA_B) **0x80000310**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0		Data for GPIO_B[29:16] pin													
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Data for GPIO_B[15:0] pin															

If a certain GPIO_B pin is set to output mode and act as GPIO, the corresponding bit of this register controls the status of GPIO_B pin; Low or High. If it is set to input mode and act as GPIO, the corresponding bit represents the status of GPIO_B pin; Low or High.

GPIO_B Direction Control Register (GIOCON_B) **0x80000314**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0		Direction control for GPIO_B[29:16] pin													
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Direction control for GPIO_B[15:0] pin															

If a bit is set to 1, the corresponding GPIO_B pin is set to output mode. If set to 0, GPIO_B pin is set to input mode.

The GPIO_B[29:28] and GPIO_B[27:26] pin is unable to be set to different I/O mode. That is, GPIO_B[29] have always same direction with GPIO_B[28], and it is same for GPIO_B[27] and GPIO_B[26]. So to make GPIO_B[29:28] or GPIO_B[27:26] output port you must set both GIOCON_B[29] and GIOCON_B[28] to 1 or both GPIO_B[27] and GPIO_B[26] to 1 concurrently.

GPIO_B Function Select Register (GSEL_B) **0x80000318**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0		USBH[1:0]		USB[1:0]		0	DAI[3:0]				LCD[3:0]				0
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0			GS3[2:0]			0	UTX	NWE	IDE	CS[3:0]				SCS	CKE

If a bit is set to 1, the corresponding GPIO_B pin is used by the other dedicated peripherals. The dedicated peripherals for these GPIO_B pins are USB controller, DAI & CDIF controller., UART, memory controller, and one of four GSIO ports.

JSBH [29:28	**GPIO_B[29:28] Function Select**
0	GPIO_B[29:28] pin is working as Normal GPIO Function
3	GPIO_B[29:28] pin are working as USBH D- / D+ Port

USB [27:26]	**GPIO_B[27:26] Function Select**
0	GPIO_B[27:26] pin is working as Normal GPIO Function
3	GPIO_B[27:26] pin are working as USB D- / D+ Port

DAI [24:21]	**GPIO_B[24:21] Function Select**
0	GPIO_B[24:21] pin is working as Normal GPIO Function
DAI[3] = 1	GPIO_B[24] pin is working as DAO signal of DAI block
DAI[2] = 1	GPIO_B[23] pin is working as MCLK signal of DAI block
DAI[1] = 1	GPIO_B[22] pin is working as LRCK signal of DAI block
DAI[0] = 1	GPIO_B[21] pin is working as BCLK signal of DAI block

LCD [20:17]	GPIO_B[20:17] Function Select
0	GPIO_B[20:17] pin is working as Normal GPIO Function
LCD[3] = 1 LCD[2] = 1 LCD[1] = 1 LCD[0] = 1	GPIO_B[20] pin is working as AC_BIAS of LCD block GPIO_B[19] pin is working as PXCLK of LCD block GPIO_B[18] pin is working as VSYNC of LCD block GPIO_B[17] pin is working as HSYNC of LCD block

* These fields are valid only in TCC761.

GS3 [12:10]	GPIO_B[12:10] Function Select
0	GPIO_B[12:10] pin is working as Normal GPIO Function
GS3[2] = 1 GS3[1] = 1 GS3[0] = 1	GPIO_B[12] pin is working as FRM of GSIO3 block GPIO_B[11] pin is working as SCK of GSIO3 block GPIO_B[10] pin is working as SDO of GSIO3 block

* These fields are valid only in TCC761.

UTX [8]	GPIO_B[8] Function Select
0	GPIO_B[8] pin is working as Normal GPIO Function
1	GPIO_B[8] : UART TX signal of UART block

NWE [7]	GPIO_B[7] Function Select
0	GPIO_B[7] pin is working as Normal GPIO Function
1	GPIO_B[7] : ND_nWE (write enable for NAND flash)

IDE [6]	GPIO_B[6] Function Select
0	GPIO_B[6] pin is working as Normal GPIO Function
1	GPIO_B[6] : IDE_nCS1 (chip select for IDE device)

* These fields are valid only in TCC761.

CS [5:2]	GPIO_B[5:2] Function Select
0	GPIO_B[5:2] pin is working as Normal GPIO Function
CS[3] = 1 CS[2] = 1 CS[1] = 1 CS[0] = 1	GPIO_B[5] : nCS3 or ND_nOE3 of memory controller GPIO_B[4] : nCS2 or ND_nOE2 of memory controller GPIO_B[3] : nCS1 or ND_nOE1 of memory controller GPIO_B[2] : nCS0 or ND_nOE0 of memory controller

SCS [1]	GPIO_B[1] Function Select
0	GPIO_B[1] pin is working as Normal GPIO Function
1	GPIO_B[1] : SD_nCS (chip select for SDRAM)

CKE [0]	GPIO_B[0] Function Select
0	GPIO_B[0] pin is working as Normal GPIO Function
1	GPIO_B[0] : SD_CKE (clock enable for SDRAM)

GPIO_B Test Select Register (GTSEL_B) **0x8000031C**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0		EX1A	EX2	0			EX1E	GST[2:0]			0				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0						IDECS	0			EX1CLK				0	FOUT

If a bit is set to 1, and the corresponding bit of GSEL_B is 0, GPIO_B pin is used by the other dedicated peripherals.

EX1A [29]	GPIO_B[29] Function Select
0	GPIO_B[29] pin is working as Normal GPIO Function or USB DN
1	GPIO_B[29] pin is working as EX1CLK from Clock Controller

EX2 [28]	GPIO_B[28] Function Select
0	GPIO_B[28] pin is working as Normal GPIO Function or USB DP
1	GPIO_B[28] pin is working as EX2CLK from Clock Controller

EX1A [24]	GPIO_B[24] Function Select
0	GPIO_B[24] pin is working as Normal GPIO Function or I2S Data Output
1	GPIO_B[24] pin is working as EX1CLK from Clock Controller

GST [23:21]	GPIO_B[23:21] Function Select
0	GPIO_B[23:21] pin is working as Normal GPIO Function
GST[2] = 1	GPIO_B[23] pin is working as FRM of 1 of 4 GSIO blocks
GST[1] = 1	GPIO_B[22] pin is working as SCK of 1 of 4 GSIO blocks
GST[0] = 1	GPIO_B[21] pin is working as SDO of 1 of 4 GSIO blocks

IDECS [9]	GPIO_B[9] Function Select
0	GPIO_B[9] pin is working as Normal GPIO Function
1	GPIO_B[9] pin is working as IDE_nCS1

EX1CLK [5:2]	GPIO_B[5:2] Function Select
0	GPIO_B[5:2] pin is working as Normal GPIO Function
1	GPIO_B[5:2] pin is working as EX1CLK from Clock Controller

FOUT [0]	GPIO_B[0] Function Select
0	GPIO_B[0] pin is working as Normal GPIO Function
1	GPIO_B[0] pin is working as FOUT from Clock Controller

GPIO_C Data Register (GDATA_C) **0x80000320**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Data for GPIO_C[15:0] pin															

* This register is valid only in TCC761.

If a certain GPIO_C pin is set to output mode and act as GPIO, the corresponding bit of this register controls the status of GPIO_C pin; Low or High. If it is set to input mode and act as GPIO, the corresponding bit represents the status of GPIO_C pin; Low or High.

GPIO_C Direction Control Register (GIOCON_C) **0x80000324**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Direction control for GPIO_C[15:0] pin															

* This register is valid only in TCC761.

If a bit is set to 1, the corresponding GPIO pin is set to output mode. GPIO_C port works only in 16-bit bus mode. In 32-bit bus mode, this port works as an upper half bus of 32-bit data bus.

GPIO_D Data Register (GDATA_D) **0x80000330**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0										Data for GPIO_D[21:16]					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Data for GPIO_D[15:0] pins (Bits [14:0] are valid only in TCC761)															

GPIO_D Direction Control Register (GIOCON_D) **0x80000334**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0										Direction Control for GPIO_D[21:16]					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Direction control for GPIO_D[15:0] pin (Bits [14:0] are valid only in TCC761)															

* At power on reset, internal pull-up resistors are enabled for GPIO_D[21:18] pins.

If a bit is set to 1, the corresponding GPIO_D pin is set to output mode. If set to 0, GPIO_D pin is set to input mode.

8 CLOCK GENERATOR

8.1 Overview

The TCC76x has a lot of peripherals with different operating frequency. To provide an appropriate clock to each peripheral, the TCC76x has a clock generator unit. There is also a power management feature that can manage several operating modes, such as initialization mode, normal operation mode, idle mode, stop mode.

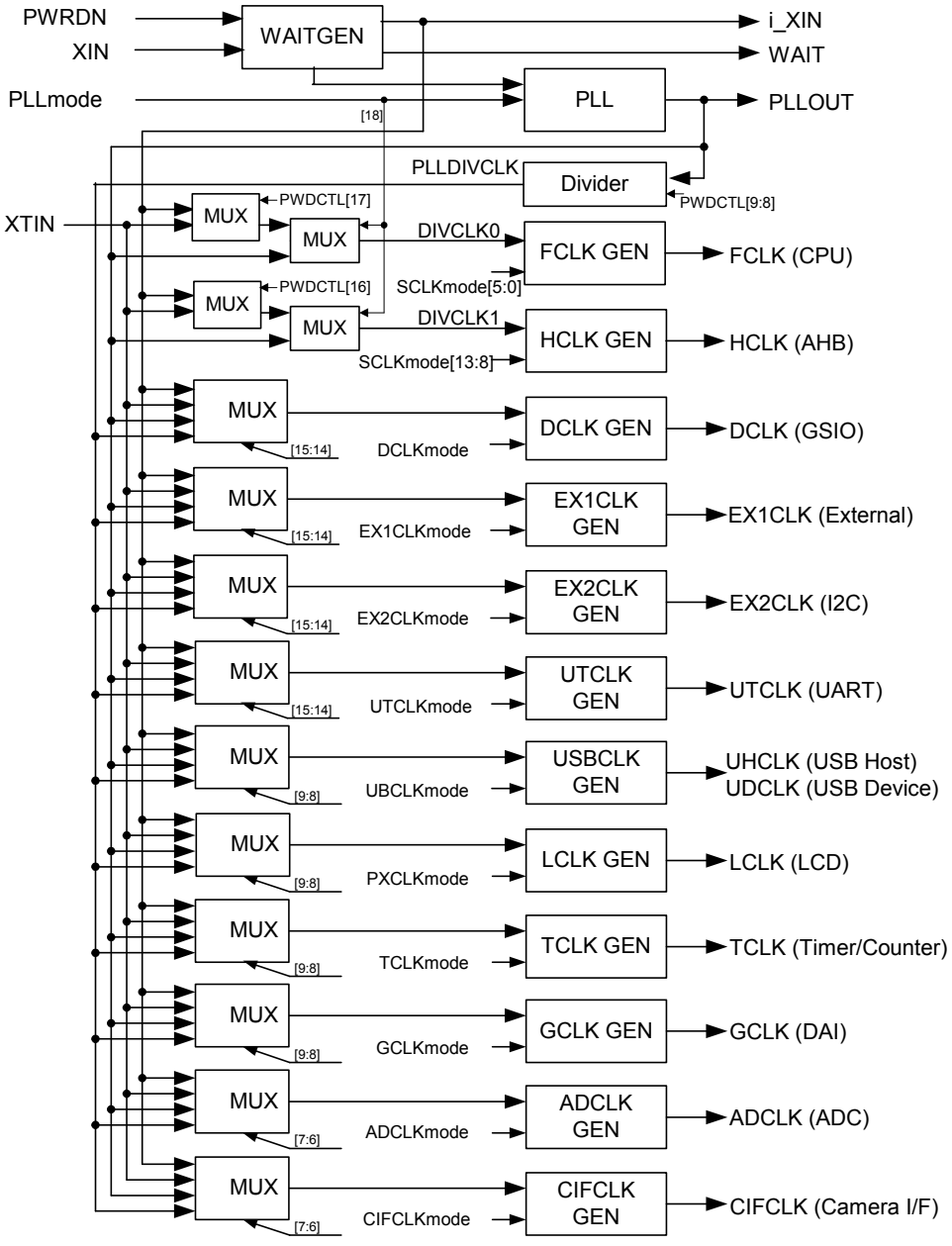


Figure 8.1 Clock Generator Block Diagram

WAITGEN module is for waiting until oscillation is stabilized. It blocks internal clocks until about 2^{18} transitions occur on XIN after reset is released. If frequency of XIN is 16MHz, the wait time is about 16.4 ms (21.85ms @12MHz). The source of the system clocks (FCLK and HCLK) can be selected among XIN (main oscillator), PLLOUT (PLL output clock) and XTIN (sub-oscillator). The other clocks that are dedicated to each

peripheral can be driven by one of three clock sources (XIN, PLLOUT, XTIN) or divided PLL output.
Each clock generation module has two modes of clock division - normal divider mode and DCO mode that is described below. The two modes can be selected by DIVMODE register.

8.1.1 DCO Control

DCLK is used as the master clock of DAI (Digital Audio Interface) block if it is in master mode. EXTCLK is used for external usage especially for CD application. UTCLK is used as the main clock of UART controller.

These clocks are generated by 14bit DCO (Digital Controlled Oscillator) that can generate a stable and flexible frequency as long as its frequency is below about one tenth of the divisor clock. That is, if the frequency of DCO source clock is more than ten times of that of DCO output clock, the jitter of DCO output clock can be less than 10%.

For reliable operation of DAI, the frequency of divisor clock must be higher than about 240MHz as the frequency of DCLK usually has about 10 to 22 MHz. The target frequency can be acquired by writing the phase value calculated by the following equation to each PHASE register.

D_PHASE = 16384 * f_{DCLK} / f_{DIV}
EX1_PHASE = 16384 * f_{EX1CLK} / f_{DIV}
EX2_PHASE = 16384 * f_{EX2CLK} / f_{DIV}
UT_PHASE = 16384 * f_{UTCLK} / f_{DIV}

Where, f_{DIV} is the frequency of divisor clock that is normally frequency of PLLOUT clock. For example, when you use 44.1KHz sampling rate and want to set DCLK as 256fs, the target frequency of DCLK is 256 * 44.1k = 11.2896 MHz, and if you set PLL to 266MHz, the D_PHASE value must be set to 696 (~= 16384 * 11.2896 / 266).

The other clocks have 6bit DCO, so the formula for setting frequency is different from that of 14bit DCO clocks. The main difference is that the multiplication factor is changed to 64 instead of 16384. For 6bit DCO clocks, they have poorer resolution than that of 14bit DCO clocks. So it is strongly recommended to use n power of 2 as a phase value of those clocks. In that case, the DCO simply act as a clock divider circuit. For example, if the source clock of DCO has 200MHz, the preferred frequencies for it are 100MHz, 50MHz, 25MHz, 12.5MHz, etc.

For both type of DCOs, it has limited frequency that can be generated with it. The maximum frequency of DCO is a half of its divisor clock's frequency. But, by setting to 0 at its phase value, it is possible to get the same frequency as its divisor clock's frequency.

Table 8.1 Example of Phase for Several Target Frequencies

Target	6bit DCO	14bit DCO	Description
f_{IN}	0x00	0x0000	Bypass ($f_{OUT} = f_{IN}$)
f_{IN} / 2	0x20	0x2000	Divide by 2 ($f_{OUT} = f_{IN}$ / 2)
f_{IN} / 4	0x10	0x1000	Divide by 4 ($f_{OUT} = f_{IN}$ / 4)
f_{IN} / 8	0x08	0x0800	Divide by 8 ($f_{OUT} = f_{IN}$ / 8)
f_{IN} / 16	0x04	0x0400	Divide by 16 ($f_{OUT} = f_{IN}$ / 16)
f_{IN} / 32	0x02	0x0200	Divide by 32 ($f_{OUT} = f_{IN}$ / 32)

8.1.2 Power Down Mode

In power down mode, all the clocks including the main oscillator (XIN) can be disabled for maxmum power saving. There are three possible cases in power down mode.

1. All the clocks stopped
2. 32-bit counter running with XTIN clock input.
3. All or part of the peripherals running with XTIN clock input.

The XTIN clock can be managed to remain enabled, by setting either XTE bit of PLLmode to 1 or XTTC32 bit of PWDCTL to 0. (Refer to Figure 8.2 for control bit usages).

Before power down mode is enabled, “Interrupt Enable Register” and “Wakeup Event Register” must be programmed appropriately. Any bit enabled in these registers can wakeup the system from the power down mode.

If sub-oscillator (XTIN) is not used or disabled in power down mode (case 1 above), only the external interrupt pins (GPIO_A[15:12]/EXINT[3:0]) can wake up the system. In this case, the corresponding bit(s) of “Wakeup Event Register” must be enabled. Refer to Section “Interrupt Controller” for “Wakeup Event Register” description.

When HCLK is stopped (case 2 above), the TCC76x interrupt controller stops immediately and does not work. Only the following events are masked by “Wakeup Event Register” and sent to the clock wakup circuitry.

- 32-bit timer interrupt
- external interrupt pins (GPIO_A[15:12]/EXINT[3:0])

It is recommended to disable “Interrupt Enable Register” and use “Wakeup Event Register” in all cases.

Right after exit from power down mode, the XIN crystal starts oscillation and the processor waits until the input frequency is stabilized, and continues to operate at the next instruction. Note that the XTIN input has no wait logic for crystal stabilization. Thus, do not disable XTIN oscillator input when the CPU is running with XTIN.

Power down mode can be entered by writing a “1” to PDN bit of CKCTRL register.

8.1.3 IDLE Mode

In idle mode, the FCLK of the ARM940T is disabled and HCLK can be disabled optionally by using HD bit of SCLKmode register.

Before Idle mode is enabled, “Interrupt Enable Register” and “Wakeup Event Register” must be programmed appropriately. Any bit enabled in these registers can wakeup the system from the Idle mode.

As explained in previous section, the TCC76x interrupt controller does not work when HCLK is stopped. So, make sure to disable “Interrupt Enable Register” and use “Wakeup Event Register” if HCLK is to be stopped.

Idle mode can be entered by writing a “1” to IDLE bit of CKCTRL register. Refer to the description of PWDCTL and HCLKSTOP register for additional power control options which can be used in idle mode.

8.2 Register Description

Table 8.2 Clock Generator Register Map (Base Address = 0x80000400)

Name	Address	Type	Reset	Description
CKCTRL	0x00	R/W	0x00007FFE	Clock Control Register
PLLMODE	0x04	R/W	0x00002E02	PLL Control Register
SCLKmode	0x08	R/W	0x00082000	System Clock Control Register
DCLKmode	0x0C	R/W	0x00000800	DCLK (DAI/CODEC) Control Register
EACLKmode	0x10	R/W	0x00000000	ADCLK and EX2CLK Control Register
EX1CLKmode	0x14	R/W	0x00000000	EX1CLK Control Register
UTCLKmode	0x18	R/W	0x000001BE	UTCLK (UART) Control Register
UBCLKmode	0x1C	R/W	0x00000000	UBCLK (USB) Control Register
LCLKmode	0x20	R/W	0x00000000	LCLK (LCD) Control Register
TCLKmode	0x24	R/W	0x00000000	TCLK (Timer) Control Register
GCLKmode	0x28	R/W	0x00000000	GCLK (GSIO) Control Register
CIFCLKmode	0x2C	R/W	0x00000000	CIFCLK Control Register
SW_nRST	0x3C	R/W	0x0000FEFF	Software Reset for each peripherals
PWDCTL	0x40	R/W	0x00000000	Power Down Control
DIVMODE	0x44	R/W	0x00000000	Divider Mode Enable (DCO Disable)
HCLKSTOP	0x48	R/W	0x00000000	HCLK Stop Control

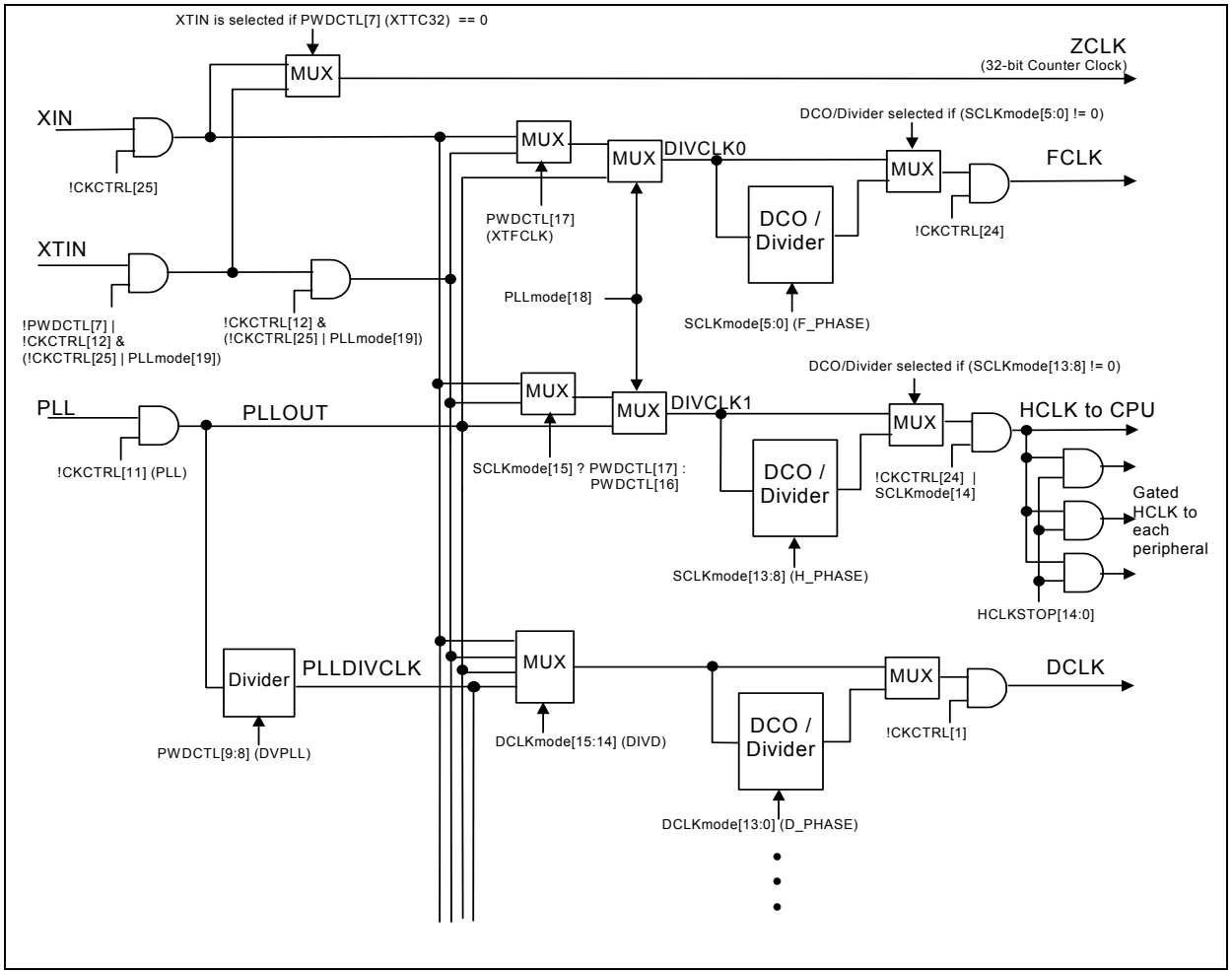


Figure 8.2 Clock Generator Register Signals

Clock Control Register (CKCTRL) 0x80000400

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0						PDN	IDLE	0				TSTCK			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	CIF	ADC	XTIN	PLL	UBH	GCK	TCK	LCK	USB	UART	EX1	EX2	0	DAI	0

This register controls various sources of clocks fed to each peripheral. If each control bit (Bit [14:0]) is set to 1, the corresponding clock is disabled and the peripherals using that clock are also disabled. To enable the clock, clear the control bit to 0.

Bit	Name	Type	Default	Description
31:26	Reserved	R	0	Reserved
25	PDN	W	0	Power Down Mode Enable. When this bit is written with "1", all blocks are disabled. Do not enable this bit when the PLL is enabled and PLLOUT is selected. This bit is write-only, always read as zero.
24	IDLE	W	0	Idle Mode Enable. When this bit is written with "1", only the CPU is disabled. Do not enable this bit when the PLL is enabled and PLLOUT is selected. This bit is write-only, always read as zero.
23:20	Reserved	R	0	Reserved
19:16	TSTCK	R/W	0	Test Clock Output Selection (GPIO_B0 with GTSEL_B0 = 1). Prior to use this field, user must set GPIO_B0 port appropriately. The GTSEL_B0 should be set to 1, and the GSEL_B0 should be set to 0. Care must be taken not to use SDRAM in this mode, because the GPIO_B0 pin is shared with SD_CKE signal. 0x0 ~ 0x8: Set to Low 0x9: PLLOUT 0xA: PLLOUT xor DIVCLK1(either PLLOUT or XIN) 0xB: DIVCLK1 xor TCLK xor GCLK 0xC: CIFCLK xor DCLK xor EX2CLK 0xD: FCLK xor UHCLK xor EX1CLK 0xE: UTCLK xor UDCLK 0xF: LCLK xor ADCLK xor EX1CLK
15	Reserved	R	0	Reserved
14	CIF	R/W	1	CIF Clock Control (0 = Enable, 1 = Disable)
13	ADC	R/W	1	ADC Clock Control (0 = Enable, 1 = Disable)
12	XTIN	R/W	1	Sub Oscillator Clock Control (0 = Enable, 1 = Disable) This bit has no effect if XTTC32 of PWDCTL is "0" (XTIN always enabled).
11	PLL	R/W	1	PLL Control (0 = Enable, 1 = Disable)
10	UBH	R/W	1	USB Host Clock Control (0 = Enable, 1 = Disable)
9	GCK	R/W	1	GSIO Clock Control (0 = Enable, 1 = Disable)
8	TCK	R/W	1	Timer Clock Control (0 = Enable, 1 = Disable)
7	LCK	R/W	1	LCD Clock Control (0 = Enable, 1 = Disable)
6	USB	R/W	1	USB Device Clock Control (0 = Enable, 1 = Disable)
5	UART	R/W	1	UART Clock Control (0 = Enable, 1 = Disable)
4	EX1	R/W	1	EXT1 Clock Control (0 = Enable, 1 = Disable) The EX1 clock can be monitored through GPIO_B29, GPIO_B24, GPIO_B5, GPIO_B4, GPIO_B3, and GPIO_B2 pins. (Refer to Chapter GPIO)
3	EX2	R/W	1	EXT2 (I2C) Clock Control (0 = Enable, 1 = Disable) The EX2 clock can be monitored through GPIO_B28, GPIO_A9 and GPIO_A10 pins. Refer to GPIO chapter for more information. The EX2 clock is also a source clock for the I2C core module.
2	Reserved	R	1	Reserved
1	DAI	R/W	1	DAI Clock Control (0 = Enable, 1 = Disable)
0	Reserved	R	0	Reserved

PLL Control Register (PLLmode) **0x80000404**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0											LOCK	XTE	DIV1	S	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved		M						0	0	P					

Bit	Name	Type	Default	Description
31:21	Reserved	R	0	Reserved
20	LOCK	R	0	PLL Lock Counter Flag indicates that the internal PLL is in lock state. This flag is generated from a counter, which runs with XIN oscillator clock input. In case of 12MHz frequency, this bit will be set at about 341μs after PLL is enabled. This bit is cleared when PLL bit (Bit [11]) of CKCTRL register is set. Do not look up this flag when PLL S/M/P parameter values are changed.
19	XTE	R/W	0	XTIN Enable in Power Down Mode. 0 XTIN is disabled in power down mode 1 XTIN is controlled by XTIN bit of CKCTRL register This bit has no effect if XTTC32 bit of PWDCTL register is 0 (XTIN is always enabled).
18	DIV1	R/W	0	Divisor Clock Select 0 Use Oscillator input as DIVCLK1 and DIVCLK0 1 Use PLL output as DIVCLK1 and DIVCLK0
17:16	S	R/W	0	PLL Post-Scaler ($0 \le S \le 3$)
15:14	Reserved	R	0	Reserved
13:8	M	R/W	0x2E	PLL Main-Divider ($1 \le P \le 62$)
7:6	Reserved	R	0	Reserved
5:0	P	R/W	0x0E	PLL Pre-Divider ($1 \le P \le 62$)

S/M/P	PLL Frequency Setting	
S [1:0]	Post-Scaler	($0 \le S \le 3$)
M[5:0]	Main-Divider	($1 \le P \le 62$)
P [5:0]	Pre-Divider	($1 \le P \le 62$)

The PLL output frequency can be acquired by the following equation.

$$f_{PLL} = f_{Xin} * 8 * (M + 2) / ((P + 2) * 2^{S})$$

Where, M, P, S can be set by PLLmode register. Note that not all the M and P parameter combinations are valid. Make sure to check the stability of the resulting frequency.

The PLL has a standby mode to minimize power consumption. It is controlled by PLL bit of CKCTRL register.

System Clock Control Register (SCLKmode) 0x80000408

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HS	HD	H_PHASE						0		F_PHASE					

It generates FCLK, HCLK for system operation. FCLK is dedicated for the ARM940T processor, HCLK is used as internal AHB bus clock that is fed to almost internal peripherals including ARM940T processor, memory controller, DMA controller, etc. Each clock can be generated either by DCO mode or Divider mode. The 6bit DCO (Digital Controlled Oscillator) can generate a variable frequency as long as its frequency is below about one tenth of divisor clock's frequency. For reliable operation, keep the n power of 2 relationships with divisor clock, so the DCO act like a simple clock divider. (To keep the n power of 2 relationship between f_{SCLK} and f_{DIV} in DCO mode, the phase value must be one of the 0, 32, 16, 8, 4, 2, 1). The target frequency can be acquired by writing the phase value calculated by the following equation to the PHASE register.

For the DCO Mode (when DIVMODE[1] is "0"),

$PHASE = 64 * f_{SCLK} / f_{DIV}$ (PHASE must be less or equal to 32)

For the Divider Mode (when DIVMODE[1] is "1"),

$PHASE = f_{DIV} / f_{SCLK} - 1$

Although the DCO mode can generate flexible frequency outputs, it has irrequlal clock duty and jitter which may cause unexpected timing problem especially with external bus components. Timing parameters programmd in memory control registers should have sufficient margin to compensate the irregularity of the DCO. It is strongly recommended to use Divider mode (refer to DIVMODE register) rather than DCO mode.

Bit	Name	Type	Default	Description
31:16	Reserved	R	0x0008	Reserved
15	HS	R/W	0	HCLK Clock Select 0: Enable XTHCLK bit of PWDCTL register. 1: Disable XTHCLK bit of PWDCTL register. PWDCTL[16] signal, which is shown in Figure 8.1, is replaced with PWDCTL[17].
14	HD	R/W	0	HCLK Clock Disable in IDLE Mode 0: In idle mode, HCLK is enabled 1: In idle mode, HCLK is disabled By using this flag, the power of peripherals driven by HCLK especially for memory controller can save more power in idle mode. This flag must be used carefully because by setting this flag, most of the internal modules including the memory controller are stopped in idle mode. Also note that interrupt request from the internal core modules are not available if HCLK is disabled. The external interrupt pins and the 32-bit counter running with XTIN clock are valid wake up events in this case. If you want to use another interrupt source as an wakeup event, do not disable HCLK with HD bit. Instead, use HCLKSTOP register to disable each peripheral individually.
13:8	H_PHASE	R/W	0x20	HCLK Frequency Select DIVMODE[1] = 0, H_PHASE = 0: $f_{HCLK} = f_{DIV}$ or f_{FCLK} (depends on HS bit) DIVMODE[1] = 0, H_PHASE = 1 ~ 0x20: $f_{HCLK} = f_{DIV} * H\_PHASE / 2^6$ DIVMODE[1] = 0, H_PHASE > 0x20: Undefined. Do not use. DIVMODE[1] = 1, H_PHASE = X: $f_{HCLK} = f_{DIV} / (H\_PHASE + 1)$
7:6	Reserved	R	0	Reserved
5:0	F_PHASE	R/W	0	FCLK Frequency Select DIVMODE[0] = 0, F_PHASE = 0: $f_{FCLK} = f_{DIV}$ DIVMODE[0] = 0, F_PHASE = 1 ~ 0x20: $f_{FCLK} = f_{DIV} * F\_PHASE / 2^6$ DIVMODE[0] = 0, F_PHASE > 0x20: Undefined. Do not use. DIVMODE[0] = 1, F_PHASE = X: $f_{FCLK} = f_{DIV} / (F\_PHASE + 1)$

DCLK (DAI) Control Register (DCLKmode) **0x8000040C**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIVD		D_PHASE[13:0]													

Bit	Name	Type	Default	Description
31:16	Reserved	R	0	Reserved
15:14	DIVD	R/W	0	DCLK Divisor Clock Select DIVD: f_{DIVD} (Divisor Clock Source Selected) 0: XIN input 1: PLL output 2: XTIN input 3: PLLDIVCLK (PLL clock divider output)
13:0	D_PHASE	R/W	0x0800	DCLK Clock Frequency Select

DCLK is also controlled by DAI bit of CKCTRL register that can enable or disable DCLK. If this bit is set to high, DCLK is disabled and if it is low, DCLK is enabled.

DCLK is for DAI which requires 512*fs frequency. To make DCLK of this frequency, first set the frequency of PLL (f_{DIV}) more higher than 512*fs and set D_PHASE according to the above formulae. It is recommended to set the frequency of PLL by the n power of 2, than the duty ratio of DCLK is only dependant of that of PLL clock.

EACLK (External/ADC) Control Register (EACLKmode) 0x80000410

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0								DIVAD		AD_PHASE[5:0]					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DIVX2	EX2_PHASE[13:0]														

Bit	Name	Type	Default	Description
31:24	Reserved	R	0	Reserved
23:22	DIVAD	R/W	0	ADCLK Divisor Clock Select
21:16	AD_PHASE	R/W	0	ADCLK Clock Frequency Select
15:14	DIVX2	R/W	0	EX2CLK / I2C Divisor Clock Select
13:0	EX2_PHASE	R/W	0	EX2CLK / I2C Clock Frequency Select

ADCLK Divisor Clock Select

DIVAD	f_{DIVAD} (Divisor Clock Source Selected)
0	XIN input
1	PLL output
2	XTIN input
3	PLLDIVCLK (PLL clock divider output)

ADCLK Clock Frequency Select

DIVMODE[5]	AD_PHASE	f_{ADCLK} (ADCLK Frequency)
0	0	f_{DIVAD}
0	1 ~ 0x2000	f_{DIVAD}* AD_PHASE / 2^{14}
0	> 0x2000	Undefined. Do not use.
1	X	f_{DIVAD} / (AD_PHASE + 1)

EX2CLK / I2C Divisor Clock Select

DIVX2	f_{DIVX2} (Divisor Clock Source Selected)
0	XIN input
1	PLL output
2	XTIN input
3	PLLDIVCLK (PLL clock divider output)

EX2CLK / I2C Clock Frequency Select

DIVMODE[4]	EX2_PHASE	f_{EX2CLK} (EX2CLK Frequency)
0	0	f_{DIVX2}
0	1 ~ 0x2000	f_{DIVX2} * EX2_PHASE / 2^{14}
0	> 0x2000	Undefined. Do not use.
1	X	f_{DIVX2} / (EX2_PHASE + 1)

ADCLK is also controlled by ADC bit of CKCTRL register that can enable or disable ADCLK. If this bit is set to high, ADCLK is disabled and if it is low, ADCLK is enabled

EX2CLK is also controlled by EX2 bit of CKCTRL register that can enable or disable EX2CLK. If this bit is set to high, EX2CLK is disabled and if it is low, EX2CLK is enabled.

External clock is a user-programmable clock that can be used for various purposes. By setting GPIO registers, GPIO_A10, GPIO_A9 and GPIO_B28 pins can output this clock to user application board. Care must be taken not to use too high frequency that the these pins cannot cope with this signals, or the pins show no clock signal out.

EX2CLK is also a clock source for internal I2C core module. When it is used as an external clock, internal I2C core may not function dependent on the clock frequency.
EX2CLK must be programmed to meet the following equation if I2C core is enabled.

$$f_{EX2CLK} \leq f_{HCLK} / 4.0$$

EX1CLK Control Register (EX1CLKmode) **0x80000414**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIVX1	EX1_PHASE[13:0]														

Bit	Name	Type	Default	Description
31:16	Reserved	R	0	Reserved
15:14	DIVX1	R/W	0	EX1CLK Divisor Clock Select
13:0	EX1_PHASE	R/W	0	EX1CLK Clock Frequency Select

DIVX1	f_{DIVX1} (Divisor Clock Source Selected)
0	XIN input
1	PLL output
2	XTIN input
3	PLLDIVCLK (PLL clock divider output)

DIVMODE[6]	EX1_PHASE	f_{EX1CLK} (EX1CLK Frequency)
0	0	f_{DIVX1}
0	1 ~ 0x2000	f_{DIVX1} * EX1_PHASE / 2^{14}
0	> 0x2000	Undefined. Do not use.
1	X	f_{DIVX1} / (EX1_PHASE + 1)

EX1CLK is also controlled by EX1 bit of CKCTRL register that can enable or disable EX1CLK. If this bit is set to high, EX1CLK is disabled and if it is low, EX1CLK is enabled.

External clock is user-programmable clock that can be used various purposes. It is not used by internal peripherals, and by setting GPIO registers, GPIO_B29, GPIO_B24 and GPIO_B[5:2] pins can output this clock to user application board. Care must be taken not to use too high frequency that these pins cannot cope with.

UTCLK (UART) Control Register (UTCLKmode) **0x80000418**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIVUT	UT_PHASE[13:0]														

Bit	Name	Type	Default	Description
31:16	Reserved	R	0	Reserved
15:14	DIVUT	R/W	0	UTCLK Divisor Clock Select
13:0	UT_PHASE	R/W	0x1BE	UTCLK Clock Frequency Select

DIVUT	f_{DIVUT} (Divisor Clock Source Selected)
0	XIN input
1	PLL output
2	XTIN input
3	PLLDIVCLK (PLL clock divider output)

DIVMODE[7]	UT_PHASE	f_{UTCLK} (UTCLK Frequency)
0	0	f_{DIVUT}
0	1 ~ 0x2000	f_{DIVUT} * UT_PHASE / 2^{14}
0	> 0x2000	Undefined. Do not use.
1	X	f_{DIVUT} / (UT_PHASE + 1)

UTCLK is also controlled by UART bit of CKCTRL register that can enable or disable UTCLK. If this bit is set to high, UTCLK is disabled and if it is low, UTCLK is enabled

This clock is used by UART. For reliable communication with host side, this clock has the frequency of 3.6864MHz or so. The UART clock is then divided by DL register in UART block, it is not so important to maintain the duty ratio of 50%.

UBCLK (USB) Control Register (UBCLKmode) 0x8000041C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0						DIVUB		0		UB_PHASE[5:0]					

UBCLK is used as the main clock of both USB Host and Device block.

Bit	Name	Type	Default	Description
31:10	Reserved	R	0	Reserved
9:8	DIVUB	R/W	0	UBCLK Divisor Clock Select DIVUB: f_{DIVUB} (Divisor Clock Source Selected) 0: XIN input 1: PLL output 2: XTIN input 3: PLLDIVCLK (PLL clock divider output)
7:6	Reserved	R	0	Reserved
5:0	UB_PHASE	R/W	0	UBCLK Clock Frequency Select DIVMODE[8] / UB_PHASE / f_{UBCLK} (UBCLK Frequency) 0 / 0 / f_{DIVUB} 0 / 1 ~ 0x20 / $f_{DIVUB} * UB\_PHASE / 2^6$ 0 / > 0x20 / Undefined. Do not use. 1 / X / $f_{DIVUB} / (UB\_PHASE + 1)$

UBCLK is gated separately by "UBH" bit and "USB" bit of CKCTRL register to generate UHCLK (for Host Controller) and UDCLK (for Device Controller).

LCLK (LCD) Control Register (LCLKmode) 0x80000420

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0						DIVLCD		0		LCD_PHASE[5:0]					

Bit	Name	Type	Default	Description
31:10	Reserved	R	0	Reserved
9:8	DIVLCD	R/W	0	LCLK Divisor Clock Select DIVLCD: f_{DIVLCD} (Divisor Clock Source Selected) 0: XIN input 1: PLL output 2: XTIN input 3: PLLDIVCLK (PLL clock divider output)
7:6	Reserved	R	0	Reserved
5:0	LCD_PHASE	R/W	0	LCLK Clock Frequency Select DIVMODE[9] / LCD_PHASE / f_{LCLK} (LCLK Frequency) 0 / 0 / f_{DIVLCD} 0 / 1 ~ 0x20 / $f_{DIVLCD} * LCD\_PHASE / 2^6$ 0 / > 0x20 / Undefined. Do not use. 1 / X / $f_{DIVLCD} / (LCD\_PHASE + 1)$

LCLK is also controlled by LCK bit of CKCTRL register that can enable or disable LCLK. If this bit is set to high, LCLK is disabled and if it is low, LCLK is enabled.

To avoid LCD FIFO underrun, LCLK frequency must be set below HCLK frequency.

$$f_{LCD} < f_{HCLK}$$

TCLK (Timer) Control Register (TCLKmode) **0x80000424**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0						DIVT		0		TC_PHASE[5:0]					

Bit	Name	Type	Default	Description
31:10	Reserved	R	0	Reserved
9:8	DIVT	R/W	0	TCLK Divisor Clock Select DIVT: f_{DIVT} (Divisor Clock Source Selected) 0: XIN input 1: PLL output 2: XTIN input 3: PLLDIVCLK (PLL clock divider output)
7:6	Reserved	R	0	Reserved
5:0	T_PHASE	R/W	0	TCLK Clock Frequency Select DIVMODE[10] / T_PHASE / f_{TCLK} (TCLK Frequency) 0 / 0 / f_{DIVT} 0 / 1 ~ 0x20 / f_{DIVT} * T_PHASE / 2^6 0 / > 0x20 / Undefined. Do not use. 1 / X / f_{DIVT} / (T_PHASE + 1)

TCLK is also controlled by TCK bit of CKCTRL register that can enable or disable TCLK. If this bit is set to high, TCLK is disabled and if it is low, TCLK is enabled.

GCLK (GSIO) Control Register (GCLKmode) **0x80000428**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0						DIVG		0		GC_PHASE[5:0]					

Bit	Name	Type	Default	Description
31:10	Reserved	R	0	Reserved
9:8	DIVG	R/W	0	GCLK Divisor Clock Select DIVG: f_{DIVG} (Divisor Clock Source Selected) 0: XIN input 1: PLL output 2: XTIN input 3: PLLDIVCLK (PLL clock divider output)
7:6	Reserved	R	0	Reserved
5:0	G_PHASE	R/W	0	GCLK Clock Frequency Select DIVMODE[11] / G_PHASE / f_{GCLK} (GCLK Frequency) 0 / 0 / f_{DIVG} 0 / 1 ~ 0x20 / f_{DIVG} * G_PHASE / 2^6 0 / > 0x20 / Undefined. Do not use. 1 / X / f_{DIVG} / (G_PHASE + 1)

GCLK is also controlled by GCK bit of CKCTRL register that can enable or disable GCLK. If this bit is set to high, GCLK is disabled and if it is low, GCLK is enabled.

CIFCLK Control Register (CIFCLKmode) 0x8000042C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0						DIVCIF		0		CIF_PHASE[5:0]					

Bit	Name	Type	Default	Description
31:10	Reserved	R	0	Reserved
9:8	DIVCIF	R/W	0	CIFCLK Divisor Clock Select DIVCIF: f_{DIVCIF} (Divisor Clock Source Selected) 0: XIN input 1: PLL output 2: XTIN input 3: PLLDIVCLK (PLL clock divider output)
7:6	Reserved	R	0	Reserved
5:0	CIF_PHASE	R/W	0	CIFCLK Clock Frequency Select DIVMODE[12] / CIF_PHASE / f_{CIFCLK} (CIFCLK Frequency) 0 / 0 / f_{DIVCIF} 0 / 1 ~ 0x20 / f_{DIVCIF} * CIF_PHASE / 2^6 0 / > 0x20 / Undefined. Do not use. 1 / X / f_{DIVCIF} / (CIF_PHASE + 1)

CIFCLK is also controlled by CIF bit of CKCTRL register that can enable or disable CIFCLK. If this bit is set to high, CIFCLK is disabled and if it is low, CIFCLK is enabled.

Software Reset Register (SW_nRST) 0x8000043C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	CIF	LCD	DMA	UBH	ETC	ECC	FGP	I2C	GS	UT	UB	GP	TC	IC	DAI

This register can be used to generate a reset signal within a certain peripheral. If one of bits in this register is set to 0, the corresponding peripheral is initialized as like as a system reset has been issued and remained in initialization state until the corresponding bit is released back to 1.

Bit	Name	Type	Default	Description
14	CIF	R/W	1	CIF Block Reset Control
13	LCD	R/W	1	LCD Block Reset Control
12	DMA	R/W	1	DMA Block Reset Control
11	UBH	R/W	1	USB Host Block Reset Control
10	ETC	R/W	1	Miscellaneous Block Reset Control.
9	ECC	R/W	1	ECC Block Reset Control
8	FGP	R/W	0	Fast GPIO Block Reset Control
7	I2C	R/W	1	I2C Block Reset Control
6	GS	R/W	1	GSIO Block Reset Control
5	UT	R/W	1	UART/IrDA Block Reset Control
4	UB	R/W	1	USB Device Block Reset Control
3	GP	R/W	1	GPIO Block Reset Control
2	TC	R/W	1	Timer/Counter Block Reset Control
1	IC	R/W	1	Interrupt Controller Block Reset Control
0	DAI	R/W	1	DAI/CDIF Block Reset Control

Miscellaneous block contains ADC, Leading Zero Counter register, and other system configuration registers. Soft reset for this block is not recommended.

Power Down Mode Control Register (PWDCTL) 0x80000440

Bit	Name	Type	Default	Description
31:18	Reserved	R	0	
17	XTFCLK	R/W	0	Select XTIN for FCLK. If DIV1 bit of PLLmode register is "0" and this bit is set as "1", clock source for FCLK and HCLK is changed to XTIN.
16	XTHCLK	R/W	0	Select XTIN for HCLK. If DIV1 bit of PLLmode register is "0" and this bit is set as "1", clock source for HCLK is changed to XTIN. The functionality of this bit is disabled when HS bit of SCLKmode register is "1".
15:10	Reserved	R/W	0	
9:8	DVPLL	R/W	0	Clock Divisor Value for the PLL Divider described in Figure 8.1. Use the divider when the PLL output frequency is too high. DVPLL: 00 Disabled; 01 PLLOUT / 2; 10 PLLOUT / 3; 11 PLLOUT / 4
7	XTTC32	R/W	0	Clock select for 32-bit counter. Do not change when the counter is enabled. 0: XTIN 1: XIN When this bit 0, XTIN oscillator is always enabled regardless of the other register bits which controls XTIN oscillator.
6	CPUREQ	R/W	0	CPU bus request control in IDLE mode. 0: Disable the bus request signal from the CPU 1: Enable the bus request signal from the CPU
5	PAUSE	R/W	0	PAUSE the arbiter in IDLE mode. 0: Enable the AHB arbiter 1: Pause the AHB arbiter
4	CTLHCKE	R/W	0	HCLK Enable in Power Down Mode. For test purpose only.
3	XTINEN	R/W	0	Force XTIN Oscillator Enabled. For test purpose only.
2	XTINCKE	R/W	0	Force XTIN Clock Enabled. For test purpose only.
1	XINEN	R/W	0	Force XIN Oscillator Enabled. For test purpose only.
0	XINCKE	R/W	0	Force XIN Clock Enabled. For test purpose only.

Note: Except for XTTC32 bit, all the default values were selected to keep the TCC72x compatibility.

Divider Mode Enable Register (DIVMODE) 0x80000444

Bit	Name	Type	Default	Description
31:13	Reserved	R	0	
12	DVMCIF	R/W	0	Divider Mode Enable for CIF Clock (CIFCLK)
11	DVMGSIO	R/W	0	Divider Mode Enable for GSIO Clock (GCLK)
10	DVMTC	R/W	0	Divider Mode Enable for Timer/Counter Clock (TCLK)
9	DVMLCD	R/W	0	Divider Mode Enable for LCD Clock (LCLK)
8	DVMUSB	R/W	0	Divider Mode Enable for USB Clock (UHCLK, UDCLK)
7	DVMUART	R/W	0	Divider Mode Enable for UART/IrDA Clock (UTCLK)
6	DVMEXT	R/W	0	Divider Mode Enable for External Clock (EX1CLK)
5	DVMADC	R/W	0	Divider Mode Enable for ADC Clock (ADCLK)
4	DVMI2C	R/W	0	Divider Mode Enable for I2C Clock (EX2CLK)
3	DVMDAI	R/W	0	Divider Mode Enable for DAI Clock (DCLK)
2	Reserved	R/W	0	
1	DVMAHB	R/W	0	Divider Mode Enable for AHB Clock (HCLK)
0	DVMCPU	R/W	0	Divider Mode Enable for CPU Clock (FCLK)

Each bit selects clock division mode of corresponding clock generator. When set to high, DCO mode is disabled and the clock generator works as a simple divider. The PHASE field of the following registers are used as divisor values;

SCLKmode
DCLKmode
EACLKmode
EX1CLKmode
UTCLKmode
UBCLKmode
LCLKmode
TCLKmode
GCLKmode
CIFCLKmode

The clock generator output frequency is determined by the following equation.

$$f_{OUT} = f_{MUX} / (PHASE + 1)$$

Where, f_{MUX} is the frequency of multiplexer output (refer to Figure 8.1).

As described above, PHASE field has different meaning in the two modes. DIVMODE register should be programmed only when the corresponding clock is disabled or PHASE value is “0” ($f_{OUT} = f_{MUX}$). Otherwise, unexpected clock frequency is fed to core modules until correct PHASE value is written.

HCLK Stop Control Register (HCLKSTOP) **0x80000448**

Bit	Name	Type	Default	Description
31:15	Reserved	R	0	
14	HSTOPCIF	R/W	0	HCLK Stop Control for CIF Block
13	HSTOPLCD	R/W	0	HCLK Stop Control for LCD Block
12	HSTOPDMA	R/W	0	HCLK Stop Control for DMA Block
11	HSTOPUBH	R/W	0	HCLK Stop Control for USB Host Block
10	HSTOPETC	R/W	0	HCLK Stop Control for Miscellaneous Block.
9	HSTOPECC	R/W	0	HCLK Stop Control for ECC Block
8	Reserved	R/W	0	
7	HSTOPI2C	R/W	0	HCLK Stop Control for I2C Block
6	HSTOPGSIO	R/W	0	HCLK Stop Control for GSIO Block
5	HSTOPUART	R/W	0	HCLK Stop Control for UART/IrDA Block
4	HSTOPUSBD	R/W	0	HCLK Stop Control for USB Device Block
3	HSTOPGPIO	R/W	0	HCLK Stop Control for GPIO Block
2	HSTOPTC	R/W	0	HCLK Stop Control for Timer/Counter Block
1	HSTOPIC	R/W	0	HCLK Stop Control for Interrupt Controller Block
0	HSTOPDAI	R/W	0	HCLK Stop Control for DAI/CDIF Block

This register controls HCLK (AMBA System Bus Clock) to each block individually. Writing a non-zero value to this register will stop the corresponding HCLK immediately. Care must be taken to avoid system hang-up when this register is programmed.

9 USB CONTROLLER

9.1 Overview

The TCC76x supports a fully compliant to USB 1.1 specification, full-speed (12 Mbps) functions and suspend/resume signaling. The USB function controller has an endpoint EP0 for control and two in/output endpoints EP1/EP2 for bulk data transaction. The endpoint EP0 has a single 64 byte FIFO; Max packet size is 64 bytes. And the endpoint EP1 and EP2 have a single 128 byte FIFO, respectively. Max packet size of EP1 and EP2 is 64 bytes.

There are 4 types of internal registers;

IN_CSR	IN Control Status Register
OUT_CSR	OUT Control Status Register
IN_MAXP	IN Maximum Packet size Register
OUT WRITE COUNT	OUT Write Count Register

Interrupt (Status) and Interrupt Enable registers are broken down into 2 banks: Endpoint Interrupts, USB Interrupts. The MAXP, ENDPOINT INTERRUPT and ENDPOINT INTERRUPT ENABLE registers are used regardless of the direction of the endpoint. The associated CSR registers correspond to the direction of endpoint.

The TCC76x supports also 1 port of USB host interface that has the following features.

- OHCI Rev. 1.0 compliant
- USB Rev. 1.1 compatible
- 1 down stream port

9.2 Register Description for USB Device Controller

Table 9.1 USB Register Map (Base Address = 0x80000500)

Name	Address	Type	Reset	Description
NON INDEXED REGISTERS				
UBFADR	0x00	R/W	0x00	Function Address Register
UBPWR	0x04	R/W	0x00	Power Management Register
UBEIR	0x08	R/W	0x00	Endpoint Interrupt Flag Register
UBIR	0x18	R/W	0x00	USB Interrupt Flag Register
UBEIEN	0x1C	R/W	0x07	Endpoint Interrupt Enable Register
UBIEN	0x2C	R/W	0x04	Interrupt Enable Register
UBFRM1	0x30	R	0x00	Frame Number 1 Register
UBFRM2	0x34	R	0x00	Frame Number 2 Register
UBIDX	0x38	W	0x00	Index Register
COMMON INDEXED REGISTER				
MAXP	0x40	R/W	0x01	IN Max Packet Register
IN INDEXED REGISTERS				
INCSR1	0x44	R/W	0x00	IN CSR1 Register (EP0 CSR Register)
INCSR2	0x48	R/W	0x20	IN CSR2 Register
OUT INDEXED REGISTERS				
OCSR1	0x50	R	0x00	OUT CSR1 Register
OCSR2	0x54	R/W	0x00	OUT CSR2 Register
OFIFO1	0x58	R	0x00	OUT FIFO Write Count 1 Register
OFIFO2	0x5C	R	0x00	OUT FIFO Write Count 2 Register
FIFO REGISTERS				
EP0FIFO	0x80	R/W	Unknown	EP0 FIFO Register
EP1FIFO	0x84	R/W	Unknown	EP1 FIFO Register
EP2FIFO	0x88	R/W	Unknown	EP2 FIFO Register
DMA REGISTERS				
DMACON	0xC0	R/W	0x00	DMA Control Register
DMAEP1	0xC4	R/W	Unknown	EP1 FIFO Access Register for DMA
DMAEP2	0xC8	R/W	Unknown	EP2 FIFO Access Register for DMA

Function Address Register (UBFADR) **0X80000500**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								UP	FADR						

UP [7]	Function Address Update
UP = 0	Function address doesn't be updated
UP = 1	Function address can be updated with FADR

* The MCU sets this bit whenever it updates the FADR field. This bit is write only register.

FADR [6:0]	Function Address
n	Function address

This register maintains the USB Device Address assigned by the host. The control program should write the value received through a SET_ADDRESS descriptor from host to this register. The address is used for the next token. The UP bit field should be set whenever the FADR field is written. The FADR field is used after the Status phase of a Control transfer, which is signaled by the clearing of the DEND bit in the CSR registers.

Power Management Register (UBPWR) **0x80000504**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								ISOUP	Reserved			URST	RSM	SP	ENSP

ISOUP [7]	Type	ISO Update
1	R/W	Valid in ISO Mode only. If set, IRDY(IN Packet Ready) is set after a SOF token is received. If an IN token is received before a SOF token, then a zero length data packet will be sent to the host.

URST [3]	Type	USB Reset
1	R	Indicates reset signaling is received from the host.

RSM [2]	Type	Resume Signal
1	R/W	Generate a resume signaling (DP is low, DN is high).
0		Stop generating a resume signaling.

SP [1]	Type	Suspend Mode
1	R	Indicates that the USB enters suspend mode

ENSP [0]	Type	Enable Suspend Mode
0	R/W	Disable Suspend Mode
1		Enable Suspend Mode

This register is used for suspend, resume signaling. If ENSP filed is zero, the device will not enter suspend mode. If ENSP is 1 and there are no signals during 3ms, the USB enters suspend mode and the SP bit field is set to 1. It is cleared if USB receives resume or reset signal from host. The USB can also generate a resume signaling by setting RSM bit to 1.

Endpoint Interrupt Flag Register (UBEIR) **0x80000508**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved													EP2	EP1	EP0

EP2 [2]	Type	EP2 Interrupt Flag
1	R	Indicates that the USB EP2 interrupt has been generated
	W	Clear the EP2 interrupt flag.

EP1 [1]	Type	EP1 Interrupt Flag
1	R	Indicates that the USB EP1 interrupt has been generated
	W	Clear the EP1 interrupt flag.

EP0 [0]	Type	EP0 Interrupt Flag
1	R	Indicates that the USB EP0 interrupt has been generated
	W	Clear the EP0 interrupt flag.

USB Interrupt Flag Register (UBIR) **0x80000518**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved													RST	RSM	SP

RST [2]	Type	Reset Interrupt Flag
1	R	Indicates that the USB has received reset signaling (DP, DN is low during more than 10ms)
	W	Clear the Reset interrupt flag.

RSM [1]	Type	Resume Interrupt Flag
1	R	Indicates that the USB has received resume signaling (DP is low, DN is high during 10ms ~ 15ms) in suspend mode
	W	Clear the Resume interrupt flag.

SP [0]	Type	Suspend Interrupt Flag
1	R	Indicates that the USB has received suspend signalizing Suspend signal is implicit signal that is generated if there is no activity for 3ms.
	W	Clear the Suspend interrupt flag.

The suspend interrupt is generated when the USB receives suspend signaling. The SP bit field of the UBIR is set whenever there is no activity for 3ms on the bus. This interrupt is disabled in default. The resume interrupt is generated by a USB when it receives resume signaling in suspend mode. The USB reset interrupt is generated when USB controller receives the reset signaling from the host.

The USB controller has two interrupt registers:

UBEIR Endpoint interrupt register
UBIR USB interrupt register

These registers act as status registers when interrupt is generated. Once interrupt generated, it is needed to read all the interrupt registers and write back to all the registers to clear the interrupt. The endpoint interrupt register UBEIR has three bit fields that correspond to the respective endpoints.

The EP0 interrupt is generated under the following conditions:

- OUT Packet is ready. ORDY field is set in the of EP0 CSR register.
- IN Packet is ready. IRDY field is set in the of EP0 CSR register.
- STST (STALL Handshake Issued) flag is set.
- CEND (Control Transfer End) flag is set.
- DEND (Data Transfer End) is cleared (Indicates End of control transfer).

The EP1/E2 interrupt is generated under the following conditions:

For IN endpoints
- IRDY field is cleared in its CSR register.
- FIFO is flushed
- STST (STALL Handshake Issued) flag is set

- For OUT endpoints
- ORDY field is set in its CSR register.
- STST (STALL Handshake Issued) flag is set

For ISO IN endpoints:
- UNDER_RUN bit is set
- IRDY field is cleared in its CSR register.
- FIFO is flushed

For ISO OUT endpoints:
- ORDY field is set in its CSR register
- OVER RUN bit is set.

Endpoint Interrupt Enable Register (UBEIEN) **0x8000051C**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved													EP2	EP1	EP0

EP2 [2]	Type	EP2 Interrupt Control
0	R/W	Disable EP2 interrupt
1		Enable EP2 interrupt

EP1 [1]	Type	EP1 Interrupt Control
0	R/W	Disable EP1 interrupt
1		Enable EP1 interrupt

EP0 [0]	Type	EP0 Interrupt Control
0	R/W	Disable EP0 interrupt
1		Enable EP0 interrupt

USB Interrupt Enable Register (UBIEN) **0x8000052C**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved													RST	0	SP

RST [2]	Type	Reset Interrupt Control
1	R/W	Enable Reset interrupt.
0		Disable Reset interrupt

SP [0]	Type	Suspend Interrupt Control
1	R/W	Enable Suspend interrupt
0		Disable Suspend interrupt.

*) Once suspend interrupt is generated, this interrupt must be disabled not to generate it continuously. Enable suspend interrupt right after the reset or resume interrupt is detected, and disable suspend interrupt right after that interrupt is detected.

Frame Number 1 Register (UBFRM1) **0x80000530**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								FRM1							

Frame Number 2 Register (UBFRM2) **0x80000534**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								FRM2							

There are two registers, UBFRM1 and UBFRM2, which inform the frame number received from the host. The UBFRM1 denotes the lower byte of frame number. The UBFRM2 denotes the higher byte of frame number.

Frame number = FRM2 * 256 + FRM1

USB Index Register (UBIDX) **0x80000538**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								IDX							

This Index register is used to indicate the endpoint number while accessing the indexed registers: MAXP, INCSR1, INCSR2, OCSR1, OCSR2, OFIFO1, OFIFO2.

Among the following registers, those denoted by suffix letter of 'n' are index register. Index register means that its address is shared by each end point blocks. So if you want to access the indexed registers of EP0, write 0 to the index register ahead, and for EP1 write 1 to the index register, and so on.

Max Packet Register (MAXPn) **0x80000540**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved											MAXP				

MAXP [4:0]	Type	Max Packet Number
00000	R/W	MAXP == 8 bytes (Default)
00001		MAXP == 8 bytes
00010		MAXP == 16 bytes
00100		MAXP == 32 bytes
01000		MAXP == 64 bytes
10000		MAXP == 128 bytes (EP1, EP2 ISO mode only)

EP0 CSR Register (EP0CSR) **0x80000544**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								CLSE	CLOR	ISST	CEND	DEND	STST	IRDY	ORDY

This register has the control and status bits for EP0 endpoint. Since a control transaction involves both IN and OUT tokens, there is only one CSR register, mapped to INCSR1 register. EP0CSR register can access by writing "0" to UBIDX register.

CLSE [7]	Type	Clear Setup End Bit
1	W	The CEND flag is cleared when writing a 1 to this bit.

CLOR [6]	Type	Clear Output Packet Ready Bit
1	W	The ORDY flag is cleared when writing a 1 to this bit.

ISST [5]	Type	Issue STALL Handshake
1	R/W	If USB decodes an invalid token, the CPU writes a 1 to this and CLOR bit concurrently. The USB issues a STALL handshake to the current control transfer.
0		End the STALL condition by writing a 0 to this bit.

CEND [4]	Type	Control Transfer End
1	R	Indicates that the control transfer ends before DEND bit is set. It is cleared by writing a 1 to CLSE bit. When this is set, an interrupt occurs and the USB flushes FIFO and invalidates all access to FIFO.

*) When CEND bit is set, the ORDY bit also may be set. This happens when the current transfer has ended, and a new control transfer is received before the MCU can service the interrupt. In such a case, the CPU should first clear the CEND flag, and then start servicing the new control transfer.

DEND [3]	Type	Data End
1	R/W	CPU write a 1 to this bit: - after loading the last packet of data into the FIFO, at the same time IRDY flag is set. - while it clears ORDY after unloading the last packet of data. - for a zero length data phase, when it clears ORDY flag and sets IRDY flag. In the case of a control transfer where there is no data phase, the CPU (after unloading the setup token) sets DEND at the same time it clears ORDY for the setup token.

STST [2]	Type	STALL Handshake Issued
1	R	Indicates that a control transaction is ended due to a protocol violation. An interrupt is generated when this bit is set.
0	W	Clear STST flag by writing 0.

IRDY [1]	Type	IN Packet Ready
1	W	After writing a packet of data into EP0 FIFO, set this bit to 1.

0	R	Indicates that the packet has been successfully sent to host. An interrupt is generated when the this bit is cleared, so the CPU can load the next packet. For a zero length data phase, the CPU must set IRDY and DEND at the same time.

ORDY [0]	Type	OUT Packet Ready
1	R	Indicates that a valid token is written to the FIFO. An interrupt is generated after this flag is set. The CPU can clear this by writing a 1 to CLOR bit.

IN CSR1 Register (INCSR1n) **0x80000544**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved									CTGL	STST	ISST	FLFF	UNDER	FNE	IRDY

This register maintains the status bits for IN type endpoints in EP1 or EP2.

CTGL [6]	Type	Clear Data Toggle Bit
1	W	The data toggle bit is cleared

STST [5]	Type	STALL Handshake Issued to an IN token
1	R	Indicates that the STALL handshake is issued to an IN token, due to the CPU setting ISST bit. When the USB issues a STALL handshake, IRDY flag is cleared.
0	W	Clear STST flag by writing 0.

ISST [4]	Type	Issue STALL Handshake
1	R/W	Issue a STALL Handshake to the USB.
0		End the STALL condition.

FLFF [3]	Type	Issue FIFO Flush
1	W	IN FIFO is flushed. This bit is cleared by the USB when the FIFO is flushed. The interrupt is generated when this happens. If a token is in progress, the USB waits until the transmission is complete before the FIFO is flushed. If two packets are loaded into the FIFO, only the top-most packet (one that was intended to be sent to the host) is flushed, and the corresponding IRDY bit for that packet is cleared.
0	R	The USB clears this bit after flushing FIFO.

UNDER [2]	Type	Under Run
1	R/W	Valid for Iso mode only. This bit is set when an IN token is received and the IRDY bit is not set. A zero length data packet is sent and the next packet that is loaded into the FIFO is flushed. This bit is cleared by writing 0.

FNE [1]	Type	IN FIFO Not Empty
0	R	Indicates that no packet of data is in IN-FIFO.
1		Indicates that at least one packet of data is in IN-FIFO.

IRDY [0]	Type	IN Packet Ready
1	W	After writing a packet of data into the IN-FIFO, set this bit to 1.
0	R	Indicates that the packet has been successfully sent to host. An interrupt is generated when the USB clears this bit to zero, so the CPU can load the next packet. While this bit is set, the CPU will not be able to write to the FIFO. If the ISST flag is set, IRDY flag cannot be set to 1.

*) FNE == 0 && IRDY == 0 : Indicates that there is no packet in the FIFO.
FNE == 1 && IRDY == 0 : Indicates that there is 1 packet in the FIFO.
FNE == 1 && IRDY == 1 : Indicates that there are 2 packets in the FIFO.

IN CSR2 Register (INCSR2n) **0x80000548**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								ASET	ISO	MDIN	DMA	Reserved			

This register is used to configure IN type endpoints.

ASET [7]	Type	Auto Set
0	R/W	User set IRDY flag manually. (Default)
1		Whenever the CPU writes MAXP data, IRDY will automatically be set by USB. If it writes less data than MAXP, it must set IRDY manually.

ISO [6]	ISO/BULK Mode Select
0	Configures endpoint mode as BULK. (Default)
1	Configures endpoint mode as ISO.

MDIN [5]	IN/OUT Select
0	Configures endpoint direction as OUT type.
1	Configures endpoint direction as IN type. (Default)

DMA [4]	DMA Enable
0	DMA Disable. (Default)
1	DMA Enable.

OUT CSR1 Register (OCSR1n) **0x80000550**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								CTGL	STST	ISST	FLFF	DERR	OVER	FFL	ORDY

This register maintains the status information of endpoints.

CTGL [7]	Type	Data Toggle Bit
1	W	The data toggle sequence bit is reset to DATA0.

STST [6]	Type	STALL Handshake Issued
1	R	Indicates that the OUT token is ended with a STALL handshake. USB issues a stall handshake to the host if host sends more than MAXP data for the OUT token.
0	W	Clear STST flag by writing 0.

ISST [5]	Type	Issue STALL Handshake
1	R/W	Issue a STALL Handshake to the USB.
0		End the STALL condition.

FLFF [4]	Type	Issue FIFO Flush
1	R/W	OUT FIFO is flushed. This bit can be set only when the ORDY flag is set.
0		Stop flushing FIFO.

DERR [3]	Type	Data Error
1	R	Valid only in ISO mode. This bit should be sampled with ORDY (Bit[0]). "1" indicates the data packet due to be unloaded by the CPU has an error (either bit stuffing or CRC). If two packets are loaded into the FIFO, and the second packet has an error, then this bit gets set only after the first packet is unloaded. This bit is automatically cleared when ORDY gets cleared.

OVER [2]	Type	OUT FIFO Over Run
1	R	Valid only in ISO mode. This bit is set if the core is not able to load an OUT ISO token into the FIFO. Cleared by writing 0.

FFL [1]	Type	OUT FIFO Full
1	R	Indicates that no more packets can be accepted

ORDY [0]	Type	OUT Packet Ready
1	R	Indicates the USB has loaded a packet of data into the FIFO.
0	W	Clears ORDY flag by writing 0. Once the CPU reads the FIFO for the entire packet, this bit should be cleared. (refer ACLR bit of OCSR2n register)

*) FFL == 0 && ORDY == 0 : Indicates that there is no packet in the FIFO.
FFL == 0 && ORDY == 1 : Indicates that there is 1 packet in the FIFO.
FFL == 1 && ORDY == 1 : Indicates that there are 2 packets in the FIFO.

OUT CSR2 Register (OCSR2n) **0x80000554**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								ACLR	ISO	Reserved					

This register maintains the configuration of endpoints.

ACLR [7]	Type	Auto Clear
1	R/W	Enable Auto Clear. Whenever the CPU reads data from the OUT FIFO, ORDY will automatically be cleared by the USB.
0		Disable Auto Clear. (Default) Once the CPU reads the FIFO for the entire packet, ORDY should be cleared manually.

ISO [6]	Type	ISO/BULK Mode Select
0	R/W	Configures endpoint mode as BULK. (Default)
1	R/W	Configures endpoint mode as ISO.

OUT FIFO Write Count 1 Register (OFIFO1n) **0x80000558**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								OFIFO1n							

OUT FIFO Write Count 2 Register (OFIFO2n) **0x8000055C**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								OFIFO2n							

There are two registers, OFIFO1n and OFIFO2n, which maintain the write count. OFIFO1n maintains the lower bytes, while OFIFO2n maintains the higher byte.

Write count = OFIFO2n * 256 + OFIFO1n

When ORDY bit of OCSR1n is set for OUT endpoints, these registers maintain the number of bytes in the packet due to be read by the CPU.

EP0 FIFO Register (EP0FIFO) **0x80000580**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								FIFO							

EP1 FIFO Register (EP1FIFO) **0x80000584**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								FIFO							

EP2 FIFO Register (EP2FIFO) **0x80000588**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								FIFO							

USB DMA Control Register (DMACON) **0x800005C0**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved									EOT		Reserved		RUN		CKSEL

Bit	Name	Type	Reset	Description
6:5	EOT	R/W	00	Force EOT. For test purpose only. Do not write in normal operation.
2:1	RUN	R/W	00	Start DMA Command for EP1 and EP0 respectively. DREQ/DACK signaling between the USB core and the central AHB DMA controller is enabled only when one/all of these bits are set. Once set, these bits are kept asserted until cleared by corresponding EOT(End of Transfer) signal from the central AHB DMA controller. Writing a "0" has no effect on these bits. These bits are forced to "0" when the corresponding "DMA" bit of IN CSR2 Register is disabled.
0	CKSEL	R/W	0	Clock Select for System Bus interface. By default (0), divided HCLK clock is used for the system bus interface logic of USB core. When this bit is set as "1", the clock divider is bypassed and HCLK is directly used. Do not enable this bit if HCLK frequency is above 60MHz.

USB DMA EP1 FIFO Register (DMAEP1) **0x800005C4**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								EP1 FIFO Data Port for DMA Controller							

USB DMA EP2 FIFO Register (DMAEP2) **0x800005C8**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								EP2 FIFO Data Port for DMA Controller							

*) Do not access FIFO registers during DMA operation.

9.3 USB Device DMA Operation

DMA operations can be started by setting the "DMA" bit (Bit[4]) of IN CSR2 Register and "RUN" bits (Bit[2:1]) of "USB DMA Control Register" described above. Before enable these bits, the USB core and the central AHB DMA controller must be programmed correctly. Be careful about the endpoint directions programmed in the USB core and Source/Destination addresses programmed in central AHB DMA controller.
Source or Destination address must be one of DMAEP1(0x800005C4) and DMAEP2(0x800005C8). Do not use EP1FIFO and EP2FIFO register address.

9.3.1 OUT Endpoint DMA Operation

After the USB core receives OUT data (≤ maximum packet size) from HOST, the endpoint which took the data will generate DREQ strobe to AHB DMA Controller as far as the FIFO isn't empty. Consequently, the number of DREQs will be equal to the number of data bytes from Host. The DMA controller can read data from the FIFO in the specific endpoint by issuing the DACK input to the core. Whenever one packet is transferred successfully from HOST to USB, the process described above shall be performed for the OUT endpoint DMA operation. This operation is repeated until EOT signal is asserted from the DMA Controller.

9.3.2 IN Endpoint DMA Operation

As long as the FIFO isn't full, DREQ signal is asserted to the DMA Controller. Then, DMA controller may write one packet of data (≤ maximum packet size) or multiple packets of data to a specific IN endpoint FIFO with DACK until EOT is asserted.

9.4 Register Description for USB Host Controller

The USB host controller complies with OHCI Rev 1.0. Refer to the specification of OHCI (Open Host Controller Interface) Rev 1.0 for more detailed information.

The following figure illustrates a block diagram of USB host controller.

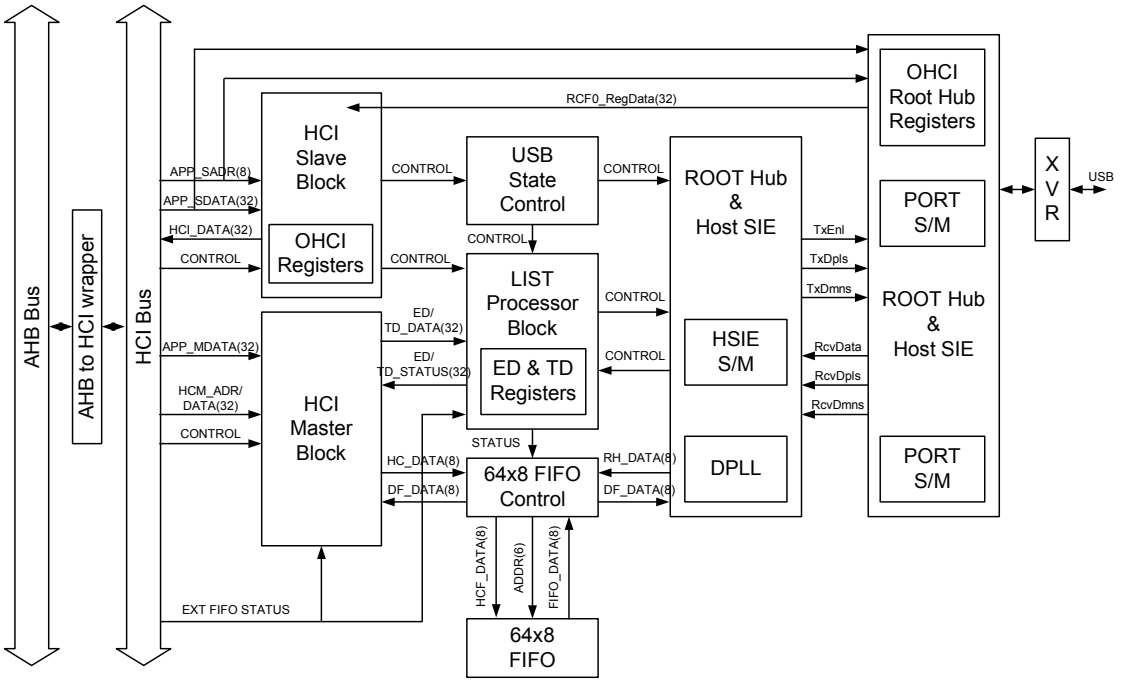


Figure 9.1 USB Host Controller Block Diagram

The following table describes the address mapping of OHCI Rev1.0 registers.

Table 9.2 USB Host Register Map (Base Address = 0x80000D00)

Name	Address	Type	Reset	Description
HcRevision	0x00	R	0x00000010	Control and status registers
HcControl	0x04	R/W	0x00000000	
HcCommandStatus	0x08	R	0x00000000	
HcInterruptStatus	0x0C	R	0x00000000	
HcInterruptEnable	0x10	R/W	0x00000000	
HcInterruptDisable	0x14	W	0x00000000	
HcHCCA	0x18	R/W	0x00000000	Memory pointer registers
HcPeriodCurrentED	0x1C	R	0x00000000	
HcControlHeadED	0x20	R/W	0x00000000	
HcControlCurrentED	0x24	R/W	0x00000000	
HcBulkHeadED	0x28	R/W	0x00000000	
HcBulkCurrentED	0x2C	R/W	0x00000000	
HcDoneHead	0x30	R	0x00000000	
HcRmInterval	0x34	R/W	0x00002EDF	Frame counter registers
HcFmRemaining	0x38	R/W	0x00000000	
HcFmNumber	0x3C	R/W	0x00000000	
HcPeriodStart	0x40	R/W	0x00000000	
HcLSThreshold	0x44	R/W	0x00000628	
HcRhDescriptorA	0x48	R/W	0x02001202	Root hub registers
HcRhDescriptorB	0x4C	R/W	0x00000000	
HcRhStatus	0x50	R/W	0x00000000	
HcRhPortStatus1	0x54	R/W	0x00000100	
HcRhPortStatus2	0x58	R/W	0x00000100	

10 UART/IrDA

10.1 Overview

The TCC76x has 1 simple UART module that can be used in programming the system software or IrDA interfacing. The block diagram of UART is in the following figure.

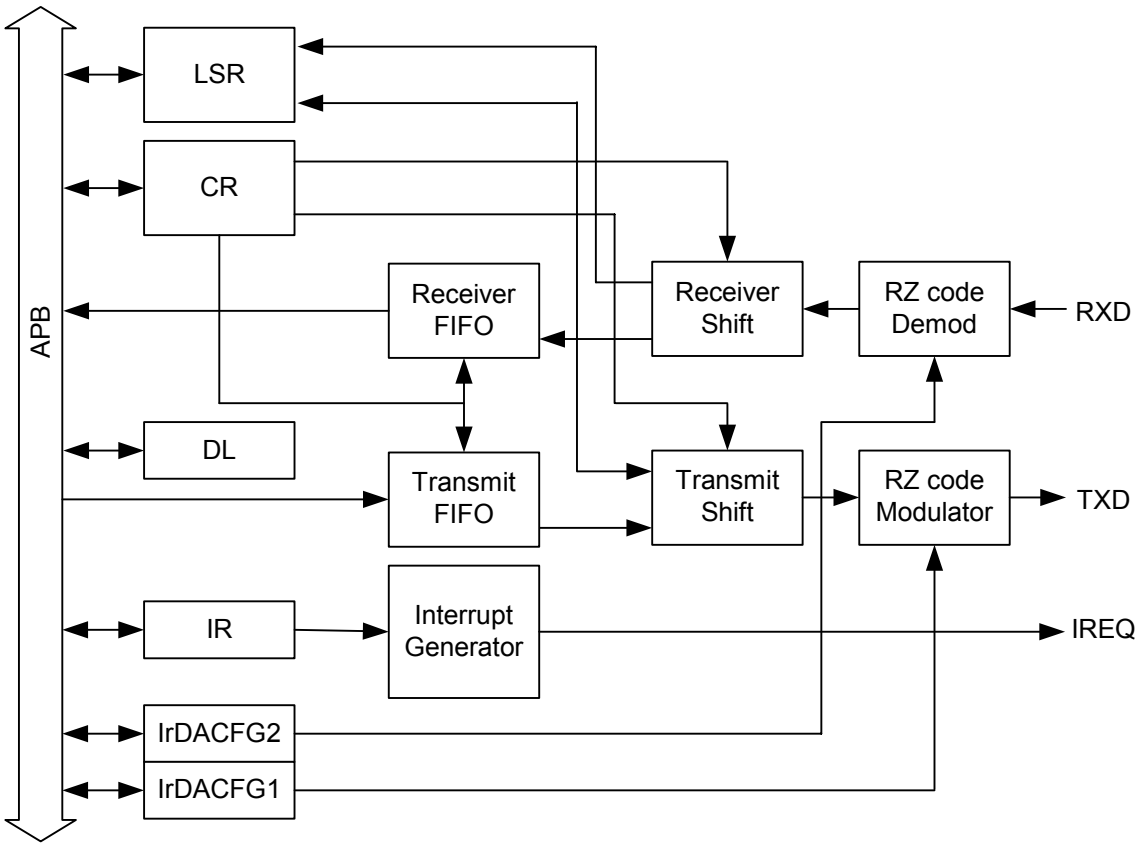


Figure 10.1 UART Block Diagram

This UART is simplified version of UART16550, it provides only a simple interface (TXD, RXD) between host system and TCC76x system.
In the UART, there are two FIFO blocks each for transmission and reception link. Transmission FIFO has 4 bytes depth, receiving FIFO has 8 bytes depth.

UART can also be used as IrDA interfacing. There is a signal transformer between IrDA signal and UART signal.
The basic timing diagram of UART and IrDA data transmission is illustrated in Figure 10.2.

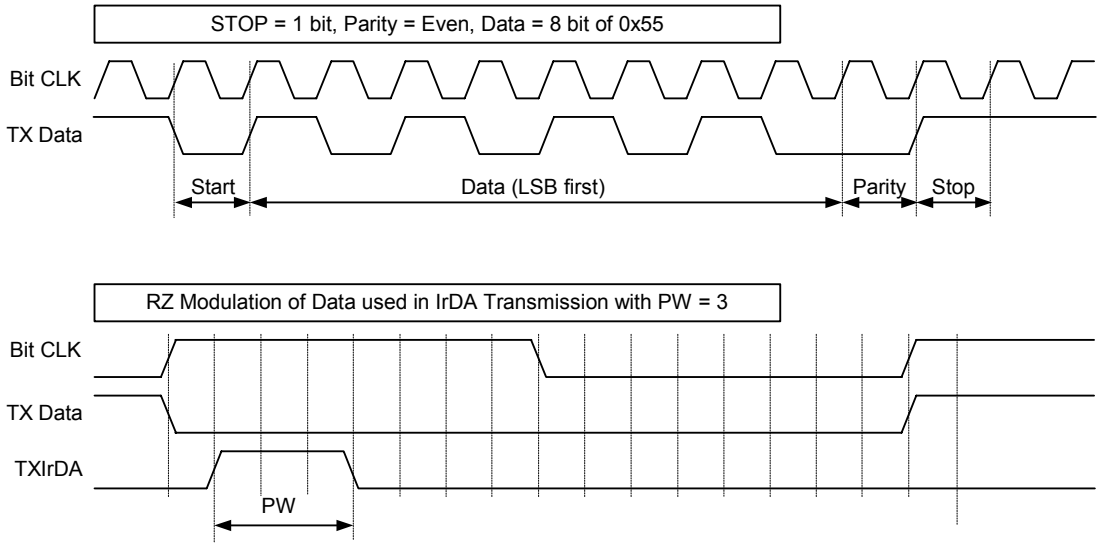


Figure 10.2 Timing Diagram of UART Transmission

10.2 Register Description

Table 10.1 UART/IrDA Register Map (Base Address = 0x80000600)

Name	Address	Type	Reset	Description
UTRXD	0x00	R	Unknown	Receiver Buffer Register
UTTXD	0x00	W	Unknown	Transmitter Holding Register
UTDL	0x04	W	0x0000	Divisor Latch Register
UTIR	0x08	R/W	0x000	Interrupt Register
UTCR	0x0C	R/W	0x000	UART Control Register
UTLSR	0x10	R	0x0101	Status Register
IrDACFG1	0x14	R/W	0x0003	IrDA Configuration Register 1
IrDACFG2	0x18	R/W	0x4da1	IrDA Configuration Register 2

Receiver Buffer Register (UTRXD) **0x80000600**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0								Received Data (when reading)							

Whenever FRX flag of IR register is set, or RA flag of LSR register is set, reading of this register gets the 1 byte of received data.

Transmitter Holding Register (UTTXD) **0x80000600**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0								Transmitting Data (when writing)							

When the transmission FIFO is not full, writing of this register fills that data to transmission FIFO. Checking TF flag of LSR register can monitor the status of a transmission FIFO.

Divisor Latch Register (UTDL) **0x80000604**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Divisor Latch Value															

This is for generation of the desired baud rate clock. This register is set to 0 at reset, UART is disabled until this register is set by non-zero value. The value can be calculated as follows.

UTDL = f_{UART} / (16 * desired baud rate)

The UART clock is generated by clock generator block. It is recommended that the frequency of UART clock is set to 3.6864MHz, so the desired baud rate can be acquired by writing a value to UTDL register as follows.

UTDL = 230400 / (desired baud rate)

Interrupt Register (UTIR) **0x80000608**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0					ERS	ETX	ERX	0	FRS	FTX	FRX	0	QRS	QTX	QRX

ERS [10]	Type	Interrupt Control
0	R/W	Receiver Line Status interrupt is disabled
1	R/W	Receiver Line Status interrupt is enabled

ETX [9]	Type	Interrupt Control
0	R/W	Transmitter Holding Register Empty interrupt is disabled
1	R/W	Transmitter Holding Register Empty interrupt is enabled

ERX [8]	Type	Interrupt Control
0	R/W	Receiver Data Available interrupt is disabled
1	R/W	Receiver Data Available interrupt is enabled

FRS [6]	Type	Receiver Line Status Flag
0	R	Indicate that Receiver Line Status has not changed
1	R	Indicate that Receiver Line Status has changed

FTX [5]	Type	Transmitter Holding Register Empty Flag
0	R	Interrupt has not generated
1	R	Interrupt has generated, but not cleared

FRX [4]	Type	Receiver Data Available Flag
0	R	Interrupt has not generated
1	R	Interrupt has generated, but not cleared

FRS, FTX, FRX is set or cleared regardless of each enable bit (ERS, ETX, ERX) settings. It can be used to follow polling method instead of interrupt method.

QRS [2]	Type	Interrupt Flag
0	R	Indicate that Receiver Line Status interrupt has not generated
1	R	Indicate that Receiver Line Status interrupt has generated

QTX [1]	Type	Interrupt Flag
0	R	Transmitter Holding Register Empty interrupt has not generated
1	R	Transmitter Holding Register Empty interrupt has generated

QRX [0]	Type	Interrupt Flag
0	R	Indicate that Receiver Data Available interrupt has not generated
1	R	Indicate that Receiver Data Available interrupt has generated

QRS, QTX, QRX is only set when each enable bit is set to 1. This flags is used to distinguish which interrupt has generated the UART flag of IREQ and MREQ register in interrupt controller.

UART/IrDA Control Register (UTCR) **0x8000060C**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0						NO	BK	TF	RF	FIFO		PR		ST	0

NO [9]	Type	Start Bit Width Check
0	R/W	Check if the pulse width of start bit is more than 0.5 bit duration of baud rate
1		Don't check the pulse width of start bit (test or boot mode only)

BK [8]	Type	Break Control Bit
0	R/W	Normal operation
1		Bit '0' is transmitted regardless of THR

TF [7]	Type	Reset Transmitter FIFO
1	R/W	The transmitter FIFO is cleared

RF [6]	Type	Reset Receiver FIFO
1	R/W	The receiver FIFO is cleared

FIFO [5:4]	Type	RX FIFO Level Select
n	R/W	0 = 1byte FIFO, 1 = 2 byte FIFO 2 = 4 byte FIFO, 3 = 7 byte FIFO

If this field is set to 1, it means that the RDA flag or interrupt is influenced when the number of received data in the RX FIFO is 2. It is recommended that this field is set to 0, so right after reception of some data, the RDA flag or interrupt can be generated.

PR [3:2]	Type	Parity Bit Select
0	R/W	Even parity
1		Odd parity
2, 3		Parity is disabled

ST [1]	Type	Stop Bit
0	R/W	1 Stop bit
1		2 Stop bit

Line Status Register (UTLSR) **0x80000610**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0											TE	TF	FE	PE	RA

TE [4]	Type	Transmitter FIFO Status
0	R	At least 1 byte is stored in transmitter FIFO.
1		No data is stored in transmitter FIFO

TF [3]	Type	Transmitter FIFO Status
0	R	At least 1 byte can be stored in transmitter FIFO.
1		No data can be stored in transmitter FIFO

Transmitter FIFO depth is fixed to 4.

FE [2]	Type	Framing Status
0	R	Stop bit is received and correct
1		The received data in the FIFO don't have valid stop bit

PE [1]	Type	Parity Status
0	R	Parity bit is received and correct
1		The received data in the FIFO don't have valid parity bit

RA [0]	Type	Received FIFO Status
0	R	No data has been received
1		At least 1 received data is stored in the FIFO

IrDA Configuration Register 1 (IrDACFG1) **0x80000614**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EN	P1	POL	LB	0								PW			

EN [15]	Type	IrDA TX Enable
0	R/W	IrDA TX is disabled, UART mode is used
1		IrDA TX is enabled

P1 [14]	Type	Transmit Pulse Type
0	R/W	Pulse width is proportional to selected baud speed
1		Pulse width is proportional to UART base clock speed

POL [13]	Type	Transmit Pulse Polarity
0	R/W	TX '0' data is converted to level high pulse
1		TX '0' data is converted to level low pulse

LB [12]	Type	Loopback
0	R/W	Normal operation
1		Transmitted data is fed back to RX port.

PW [3:0]	Type	IrDA RZ Pulse Width
PW	R/W	Controls pulse width of TX '0' data. If PW = 3, the high pulse has duration of 3/16 of it's a bit period or 3 * 3686400^{-1} sec.

The IrDA shares data path with UART. So all of UART registers such as baud rate, interrupt en/disable, communication control, line status also influence to IrDA mode.

IrDA Configuration Register 2 (IrDACFG2) **0x80000618**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EN	P1	POL	0	DEC				MAX1				MIN1			

EN [15]	Type	IrDA RX Enable
0	R/W	IrDA RX is disabled, UART mode is used
1		IrDA RX is enabled

P1 [14]	Type	Receiver Pulse Type
0	R/W	Received pulse width is proportional to selected baud speed
1		Received pulse width is proportional to UART base clock speed

POL [13]	Type	Receive Pulse Polarity
0	R/W	The polarity of received data is not inverted
1		The polarity of received data is inverted

DEC [11:8]	Type	RX Data Decision Time
n	R/W	The decision point for receiving data, its unit has 1/16 of baud rate.

MAX1 [7:4]	Type	Maximum number of "1"s
n	R/W	The maximum number of "1"s to decide the received IrDA (RZ) signal as 0. If P1 is set to 1, MAX1 has the unit of 1/1843200 sec, or if P1 is set to 0, the unit of MAX1 has 1/16 of baud rate.

MIN1 [3:0]	Type	Minimum number of "1"s
n	R/W	The minimum number of "1"s to decide the received IrDA (RZ) signal as 0. If P1 is set to 1, MIN1 has the unit of 1/1843200 sec, or if P1 is set to 0, the unit of MIN1 has 1/16 of baud rate.

11 GSIO PORT

11.1 Overview

The TCC76x has four GSIOs (General Purpose Serial Input/Output) for communication between the TCC76x and other devices that have serial interface. All the pins in the GSIOs are multiplexed with GPIOs. Refer the chapter of GPIO for more information about these multiplexing. User can program what these multiplexed pins are used for.

The GSIO block has 4 pins.

SDO	the serial data output pin
SDI	the serial data input pin
SCK	the serial clock pin
FRM	the frame pin

The base clock is generated dividing the GCLK by programming the GSIO control register GSCR. The SCK is generated from the basic clock in every data transfers. Using GSIO control field in the GSCR can program various types of serial interface.

There are 5 control registers for GSIOs; GSCR0, GSCR1, GSCR2, GSCR3, and GSICR. The start time of transfer can be controlled with programming the delay counter field in the GSCRn. The base counter increments at every base clock right after writing the data into the GSDRn. The serial data starts to come out when delay counter value are same to base counter value. The word size of transfer can be programmed from 1 bit to 16 bits. The frame1 and the frame2 fields specify the start and end point of transition based on base counter. The frame polarity defines whether the frame signal is low active or high active signal. The Last Clock mask filed is for special serial interface, which makes the last clock pulse masked.

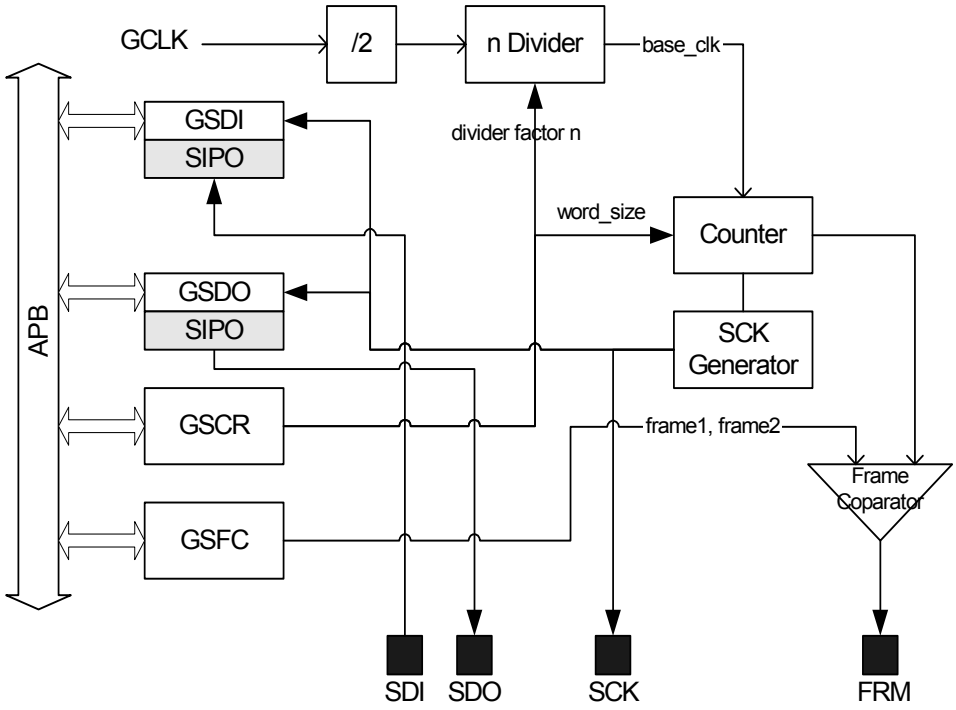


Figure 11.1 GSIO Block Diagram

11.2 Register Description

Table 11.1 GSIO Register Map (Base Address = 0x80000700)

Name	Address	Type	Reset	Description
GSDO0	0x00	R/W	Unknown	GSIO0 Output Data Register
GSDI0	0x04	R/W	Unknown	GSIO0 Input Data Register
GSCR0	0x08	R/W	0x0000	GSIO0 Control Register
GSGCR	0x0C	R/W	0x0000	GSIO Global Control Register
GSDO1	0x10	R/W	Unknown	GSIO1 Output Data Register
GSDI1	0x14	R/W	Unknown	GSIO1 Input Data Register
GSCR1	0x18	R/W	0x0000	GSIO1 Control Register
GSDO2	0x20	R/W	Unknown	GSIO2 Output Data Register
GSDI2	0x24	R/W	Unknown	GSIO2 Input Data Register
GSCR2	0x28	R/W	0x0000	GSIO2 Control Register
GSDO3	0x30	R/W	Unknown	GSIO3 Output Data Register
GSDI3	0x34	R/W	Unknown	GSIO3 Input Data Register
GSCR3	0x38	R/W	0x0000	GSIO3 Control Register

GSIOn Output Data Register (GSDO0 ~ GSDO3) 0x80000700 + (0x10 * n)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0												WORD[3:0]			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
GSDO[15:0]															

WORD [19:16]	GSIO word size
N	GSIO data has (N+1) bit unit, N = 0 ~ 15

*) This field is valid only if WS of GSCRn register is set to 1.

GSDO [15:0]	Type	GSIO Output Data
GSDO	R	The value that have been written through register is read
	W	The value is transmitted by LSB or MSB order that is controlled by MS field of GSCRn register.

GSIOn Input Data Register (GSDI0 ~ GSDI3) 0x80000704 + (0x10 * n)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Data from GSIO Input Pin															

By writing to GSDOn register, the corresponding GSIO block start to transmit and at the same time it starts to receive data through the SDI pin. At the end of transmission, the received data can be read through this GSDIn register. The bit order of receiving conforms to that of transmission.

GSIOn Control Register (GSCR0 ~ GSCR3) 0x80000708 + (0x10 * n)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EN	MS	WORD				WS	DIV							CP	CM
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	DELAY		FP	FRM1						FRM2					

EN [31]	GSIO Enable
0	Disable the corresponding GSIO block
1	Enable the corresponding GSIO block

MS [30]	First Bit Select
0	Data is transmitted or received by LSB first order
1	Data is transmitted or received by MSB first order

WORD [29:26]	GSIO word size
n	GSIO data transaction has (n+1) bit unit, n = 0 ~ 15

*) This is valid only when the WS bit of GSCRn register is 0.

WS [25]	Word Size Select
0	GSIO word size is determined by WORD of GSCRn register
1	GSIO word size is determined by BW of GSDO register

DIV [24:18]	GSIO base clock speed control
0	Reserved.
1 ≤ n ≤ 127	GSIO base clock has 1/(2n+2) of GCLK frequency.

CP [17]	GSIO clock polarity
0	SDO changes or SDI is sampled at SCK falling
1	SDO changes or SDI is sampled at SCK rising

CM [16]	Last clock mask
0	No mask. GSIO clock is generated for every SDO.
1	GSIO clock is masked at the last SDO period.

DELAY [14:13]	Initial delay for serial transmission
0	Reserved. *DELAY should not be set to 0.*
1 ≤ n ≤ 3	GSIO transmission starts after n base clock has generated.

FP [12]	Frame pulse polarity
0	FRM has low active pulse
1	FRM has high active pulse

FRM1 [11:6]	Frame pulse start position
n	Frame pulse starts after n base clock has generated

FRM2 [5:0]	Frame pulse end position
n	Frame pulse ends after n base clock has generated

Refer to the figure for a basic wave form of GSIO operation.

GSIO Global Control Register (GSGCR) 0x8000070C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
G3	G2	G1	G0	IEN3	IEN2	IEN1	IEN0	FLG3	FLG2	FLG1	FLG0	Busy3	Busy2	Busy1	Busy0

G[3:0] [15:12]	GPIO_B[23:21] Other Function Signal Select
if bit n is 1 (n=0~3)	FRM, SCK, SDO of GSIOn can be come out from GPIO_B[23:21]

*) If multiple bit of G[3:0] is set to 1, the output of each GSIO is ORed and come out from GPIO_B[23:21]. It is needed to configure the GPIO_B[23:21] as GSIO port to use these output.

IEN[3:0] [11:8]	GSIO Interrupt Enable
if bit n is 1 (n=0~3)	Enable GSIOn Interrupt
0	Disable GSIOn Interrupt

*) The master flag to enable GSIO interrupt is GS bit of IEN register in interrupt controller. User must set that flag ahead as well as these fields.

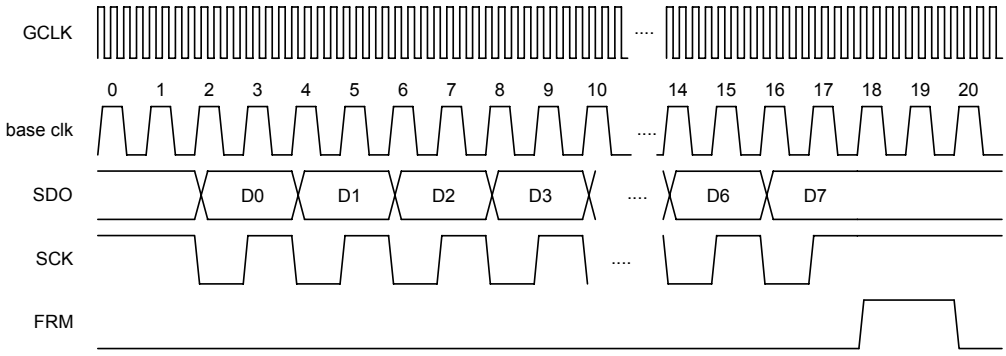
FLG[3:0] [7:4]	Type	GSIO Interrupt Flag
if bit n is 1 (n=0~3)	R	Indicates that GSIOn operation (read/write) has been completed.
	W	Clear FLG[n] field

*) If an interrupt of a GSIO is enabled, GSIO interrupt is generated when the GSIO operation is completed.
These FLGn can be used to distinguish which GSIO has generated the interrupt. These flags are cleared by writing "1" at the corresponding flag.

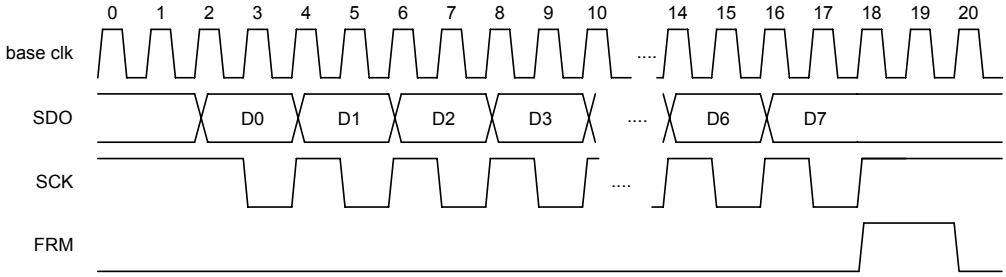
Busy[3:0] [3:0]	GSIO Cycle Busy Flag
if bit n is 0	Indicates that the transmission and reception of GSIOn have finished, and can process another serial data.
if bit n is 1	Indicates that the transmission and reception of GSIOn is in operation, so it cannot process another serial data.

The following figures illustrate the representative waveforms about the various GSIO operations.

div_factor = 1 ; div4 = 2*(1+1)
word_size = 7 ; 8bits = 7+1
init_delay = 2, clk_pol = 0
frame_pol = 1
frame1 = 18, frame2 = 20
last_clk_mask = 0



clk_pol = 1



frame1 = 17, frame2 = 19
last_clk_mask = 1, clk_pol = 1

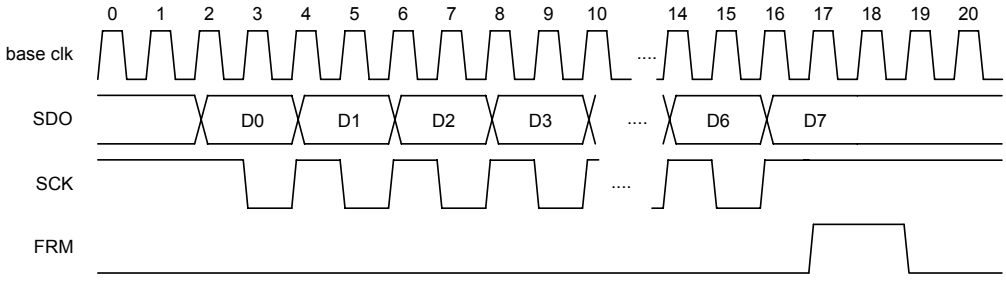


Figure 11.2 GSIO operation

12 MISCELLANEOUS PERIPHERALS

12.1 ADC

12.1.1 Overview

The TCC76x has multiple-input general purpose low-power ADC for battery level detection, remote control interface, touch screen interface, etc. It is a CMOS type 10bit A/D converter with 8-channel analog input multiplexer. The TCC761 can support up to 8 inputs for ADC, and the other derivatives can support up to 3 inputs.

- Resolution : 10-bit
- Maximum Conversion Rate : 500KSPS
- Main Clock : 2.5MHz (Max.)
- Standby Mode
- Input Range : 0.0V ~ VDDA_ADC

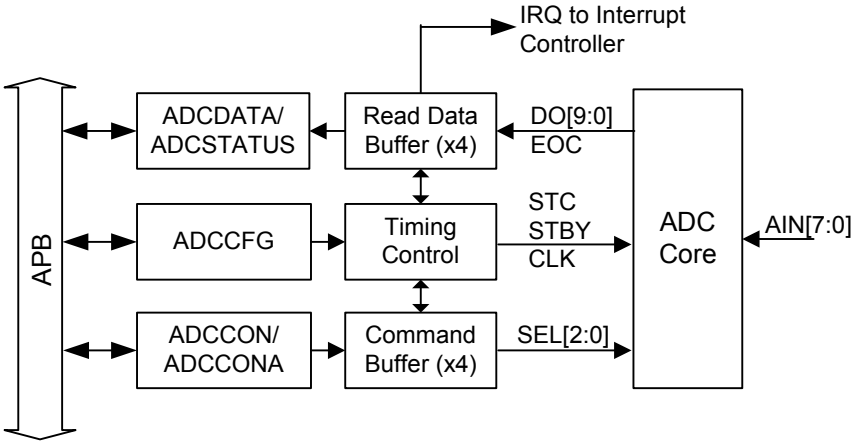


Figure 12.1 ADC Controller Block Diagram

Except for the APB interface, the ADC controller module runs with ADCLK from the Clock Generator module. The clock input is always divided before sent to the ADC core. The EACLKmode register of Clock Generator and CLKDIV bits of ADCCFG register must be programmed to get desired frequency. The maximum frequency of CLK signal in Figure 12.1 must not exceed 2.5MHz.

When one of the ADCCON or ADCCONA register is written with a channel number (SEL[2:0]), the SEL value is posted to the Command Buffer. The ADC Core starts conversion cycle as long as the Comand Buffer is not empty. After the conversion cycle is completed, the result is written in Read Data Buffer. The data can be read from either ADCDATA or ADCSTATUS register. Up to four different SEL values can be posted to the Command Buffer. When the buffer is full, data written to ADCCON/ADCCONA registers are ignored. Various operating options can be set by using ADCCFG register.

12.1.2 ADC Controller Register Description

Table 12.1 ADC Controller Register Map (Base Address = 0x80000A00)

Name	Address	Type	Reset	Description
ADCCON	0x00	R/W	0x00000018	ADC Control Register
ADCDATA	0x04	R	Unknown	ADC Data Register
ADCCONA	0x80	R/W	0x00000018	ADC Control Register A
ADCSTATUS	0x84	R/W	Unknown	ADC Status Register
ADCCFG	0x88	R/W	0x00002400	ADC Configuration Register

- ADCCON and ADCDATA registers are preserved for the TCC72x compatibility. For the new features in the TCC76x, ADCCONA and ADCSTATUS registers should be accessed.

ADC Control Register (ADCCON) **0x80000A00**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved											STB	X	ASEL		

STB [4]	Type	ADC Standby Select
1	R/W	ADC goes to standby mode
0		ADC starts operating

ASEL [2:0]	ADC Input Select
n	ADINn pin is selected as ADC input signal n = 0 ~ 7 in TCC761. n = 0, 2, 4 in other derivatives. Refer to Pin Description

ADC Data Register (ADCDATA) **0x80000A04**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0					ADATA										FLG

ADATA [10:1]	ADC Data
adc	ADC data = adc

*) All the AD input levels must be within the operable range that is from 0 V to VDDADC(the main power level of ADC). Do not exceed the limit.

FLG [0]	ADC Status Flag
1	Indicate that A/D conversion has finished, data is stable.
0	A/D conversion is on processing, data is unstable

ADC Control Register A (ADCCONA) 0x80000A80

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved											STB	X	ASEL		

*) This register has the same functionality as that of ADCCON register. Only the register address is different.

ADC Status Register (ADCSTATUS) 0x80000A84

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	WBVCNT			R	RBVCNT			Reserved					RSELV		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved						RBDATA									

Bit	Name	R/W	Reset	Description
31	Reserved	R	0	
30:28	WBVCNT	R	0	Command Write Buffer Valid entry count. Up to 4 entries with different ASEL values can be posted to command buffer.
27	Reserved	R	0	
26:24	RBVCNT	R	0	Read Data Buffer Valid entry count. Up to 4 entries.
23:19	Reserved	R	0	
18:16	RSEL	R	X	Input channel number for current read data. Valid only if RBCNT is not zero.
15:10	Reserved	R	0	
9:0	RBDATA	R	X	Read Buffer Data.

ADC Configuration Register (ADCCFG) 0x80000A88

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLKDIV				DLYSTC				NEOC	0	FIFOTH		IRQE	R8	APD	SM

Bit	Name	R/W	Reset	Description
15:12	CLKDIV	R/W	0x2	Clock Divisor Value. ADCLK is divided by ((CLKDIV + 1) * 2).
11:8	DLYSTC	R/W	0x4	Delay from SEL to STC (Start of Conversion) in ADC core CLK count. Whenever SEL value changes, delay is inserted.
7	NEOC	R/W	0	For test purpose only. Must be written as "0"
6	Reserved	R/W	0	
5:4	FIFOTH	R/W	0	FIFO Threshold for interrupt assertion. Interrupt will be asserted only if FIFOTH < (# of Valid Entry).
3	IRQE	R/W	0	Interrupt Enable.
2	R8	R/W	0	When this bit is "1", two LSBs are truncated. (shift right). Only "ADCSTATUS" register is affected by this bit.
1	APD	R/W	0	Auto Power Down Enable. This bit is effective only if SM bit (described below) is "1". After conversion cycle is done, the ADC core is forced to power down mode.
0	SM	R/W	0	Single Mode Enable. When disabled (0), ADC conversion cycle is repeated forever with the input selected by ASEL bits. When enabled (1), only one cycle is executed.

12.2 Miscellaneous Register Description

Table 12.2 Miscellaneous Register Map (Base Address = 0x80000A00)

Name	Address	Type	Reset	Description
USBCTR	0x14	R/W	0x00000004	USB Port Control Register
TSTSEL	0x18	R/W	0x00000000	Test Mode Control Register
MISCCFG	0x1C	R/W	0x00000000	Miscellaneous Configuration Register
CFGPUA	0x20	R/W	0x00000000	Pull-up Enable for GPIO_A
CFGPUB	0x24	R/W	0x00000000	Pull-up Enable for GPIO_B
CFGPUC	0x28	R/W	0x00000000	Pull-up Enable for GPIO_C
CFGPUD	0x2C	R/W	0x003C0000	Pull-up Enable for GPIO_D
CFGDRVAL	0x30	R/W	0x00000000	Buffer Drive Strength Select AL
CFGDRVAH	0x34	R/W	0x00000000	Buffer Drive Strength Select AH
CFGDRVBL	0x38	R/W	0x00000000	Buffer Drive Strength Select BL
CFGDRVBH	0x3C	R/W	0x00000000	Buffer Drive Strength Select BH
CFGDRVCL	0x40	R/W	0x00000000	Buffer Drive Strength Select CL
CFGDRVCH	0x44	R/W	0x00000000	Buffer Drive Strength Select CH
CFGDRVDL	0x48	R/W	0x00000000	Buffer Drive Strength Select DL
CFGDRVDH	0x4C	R/W	0x00000000	Buffer Drive Strength Select DH
CFGDRVXL	0x50	R/W	0x03FFFFFF	Buffer Drive Strength Select XL
CFGDRVXH	0x54	R/W	0x04000000	Buffer Drive Strength Select XH
CFGSYS	0x60	R/W	0x00000000	System Configuration

- The base address is the same for the ADC controller.

USB Port Control Register (USBCTR) **0x80000A14**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0												PSL	CNT	OVR	OVC

- USBCTR register is for test mode only, and must be set to 0x02 prior to use USB module.

TEST Mode Register (TSTSEL) **0x80000A18**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0								Reserved							

- TSTSEL register is for test mode only, must be remained as 0x00. Preserved for the TCC72x compatibility.

Miscellaneous Configuration Register (MISCFG) 0x80000A1C

<table>
<tr><th>Bit</th><th>Name</th><th>R/W</th><th>Reset</th><th>Description</th></tr>
<tr><td>31:16</td><td>Reserved</td><td>R</td><td>0</td><td></td></tr>
<tr><td>15</td><td>RDYIRQEN</td><td>R/W</td><td>0</td><td>READY Interrupt Request Enable. When enabled, input from READY pin can generate interrupt to the CPU via channel [15] of Interrupt Controller. MEN bit of Interrupt Enable Register is used for interrupt enable bit for READY pin only. Refer to RDY bits in Section 5.2 Interrupt Controller Register Description.</td></tr>
<tr><td>14</td><td>RDYIRQPOL</td><td>R/W</td><td>0</td><td>READY Interrupt Request Polarity Control. (1 = inverted)</td></tr>
<tr><td>13:5</td><td>Reserved</td><td>R</td><td>0</td><td></td></tr>
<tr><td>4</td><td>CIFEN</td><td>R/W</td><td>0</td><td>Camera Interface Enable on to GPIO pins. CIFEN has a precedence over CFGI2C bit and GPIO control bits.
<table>
<tr><th>Camera Interface Signals</th><th>GPIO Pins</th></tr>
<tr><td>HS</td><td>GPIO_D[17]</td></tr>
<tr><td>VS</td><td>GPIO_D[16]</td></tr>
<tr><td>CLK</td><td>GPIO_D[15]</td></tr>
<tr><td>Data[7:4]</td><td>GPIO_D[21:18]</td></tr>
<tr><td>Data[3:0]</td><td>GPIO_A[3:0]</td></tr>
</table></td></tr>
<tr><td>3:2</td><td>Reserved</td><td>R</td><td>0</td><td></td></tr>
<tr><td>1:0</td><td>CFGI2C</td><td>R/W</td><td>0</td><td>These bits selects GPIO pins for I2C signals.
<table>
<tr><th>CIFEN</th><th>CFGI2C[1:0]</th><th>SCL</th><th>SDA</th></tr>
<tr><td>X</td><td>00</td><td>Disabled</td><td>Disabled</td></tr>
<tr><td>X</td><td>01</td><td>GPIO_A[9]</td><td>GPIO_A[8]</td></tr>
<tr><td>X</td><td>10</td><td>GPIO_A[11]</td><td>GPIO_A[10]</td></tr>
<tr><td>0</td><td>11</td><td>GPIO_D[17]</td><td>GPIO_D[16]</td></tr>
<tr><td>1</td><td>11</td><td>Disabled</td><td>Disabled</td></tr>
</table></td></tr>
</table>

The TCC76x supports programmable output drive strength and controllable pull-up resistor for the GPIO pins. For the external bus address and command signals, only the drive strength control is supported.

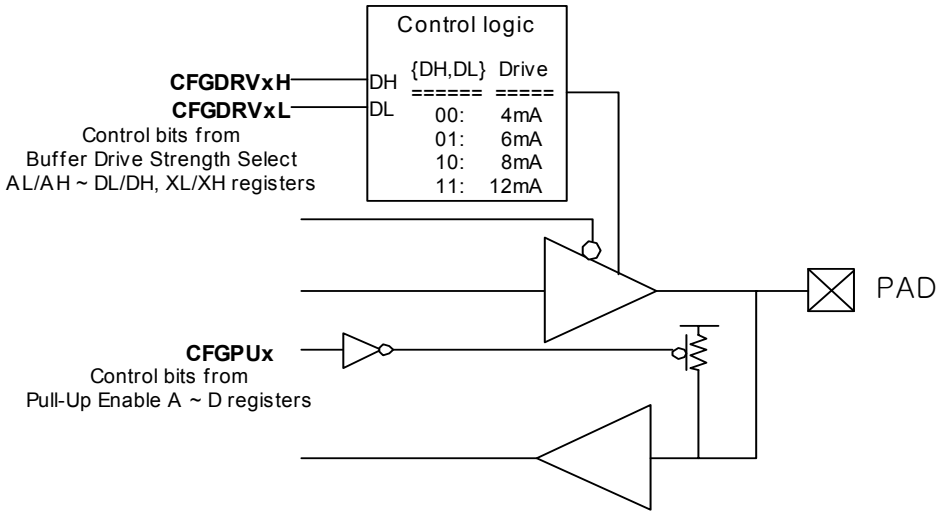


Figure 12.2 Pull-Up and Drive Strength Control

Note that pull-up and drive strength control is not applicable to GPIO_B[29:26] which are USB transceiver I/O pins.

Pull-Up Enable A (CFGPUA) 0x80000A20

Bit	Name	R/W	Reset	Description
31:0	CFGPUA	R/W	0x00000000	Pull-Up Enables for GPIO_A pins.

Pull-Up Enable B (CFGPUB) 0x80000A24

Bit	Name	R/W	Reset	Description
31:0	CFGPUB	R/W	0x00000000	Pull-Up Enables for GPIO_B pins.

Pull-Up Enable C (CFGPUC) 0x80000A28

Bit	Name	R/W	Reset	Description
31:0	CFGPUC	R/W	0x00000000	Pull-Up Enables for GPIO_C pins.

Pull-Up Enable D (CFGPUD) 0x80000A2C

Bit	Name	R/W	Reset	Description
31	CFGPUXD	R/W	0	Pull-Up Enable for XD[15:0] pins.
30:0	CFGPUD	R/W	0x003C0000	Pull-Up Enables for GPIO_D pins.

Buffer Drive Strength Select AL (CFGDRVAL) 0x80000A30

Bit	Name	R/W	Reset	Description
31:0	CFGDRVAL	R/W	0x00000000	Buffer Drive Strength Select for GPIO_A pins.

Buffer Drive Strength Select AH (CFGDRVAH) 0x80000A34

Bit	Name	R/W	Reset	Description
31:0	CFGDRVAH	R/W	0x00000000	Buffer Drive Strength Select for GPIO_A pins.

Buffer Drive Strength Select BL (CFGDRVBL) 0x80000A38

Bit	Name	R/W	Reset	Description
31:0	CFGDRVBL	R/W	0x00000000	Buffer Drive Strength Select for GPIO_B pins.

Buffer Drive Strength Select BH (CFGDRVBH) 0x80000A3C

Bit	Name	R/W	Reset	Description
31:0	CFGDRVBH	R/W	0x00000000	Buffer Drive Strength Select for GPIO_B pins.

Buffer Drive Strength Select CL (CFGDRVCL) 0x80000A40

Bit	Name	R/W	Reset	Description
31:0	CFGDRVCL	R/W	0x00000000	Buffer Drive Strength Select for GPIO_C pins.

Buffer Drive Strength Select CH (CFGDRVCH) 0x80000A44

Bit	Name	R/W	Reset	Description
31:0	CFGDRVCH	R/W	0x00000000	Buffer Drive Strength Select for GPIO_C pins.

Buffer Drive Strength Select DL (CFGDRVDL) 0x80000A48

Bit	Name	R/W	Reset	Description
31:0	CFGDRVDL	R/W	0x00000000	Buffer Drive Strength Select for GPIO_D pins.

Buffer Drive Strength Select DH (CFGDRVDH) 0x80000A4C

Bit	Name	R/W	Reset	Description
31:0	CFGDRVDH	R/W	0x00000000	Buffer Drive Strength Select for GPIO_D pins.

Buffer Drive Strength Select XL (CFGDRVXL) 0x80000A50

Bit	Name	R/W	Reset	Description
31:28	Reserved	R/W	0x0	Reserved
27	XDL	R/W	0	Buffer Drive Strength Select for XD[15:0] pins
26	CLKL	R/W	0	Buffer Drive Strength Select for SD_CLK pin
25	OEL	R/W	1	Buffer Drive Strength Select for nOE pin
24	WEL	R/W	1	Buffer Drive Strength Select for nWE pin
23:0	XAL	R/W	0xFFFFFF	Buffer Drive Strength Select for XA[23:0] pins.

Buffer Drive Strength Select XH (CFGDRVXH) 0x80000A54

Bit	Name	R/W	Reset	Description
31:28	Reserved	R/W	0x0	
27	XDH	R/W	0	Buffer Drive Strength Select for XD[15:0] pins
26	CLKH	R/W	1	Buffer Drive Strength Select for SD_CLK pin
25	OEH	R/W	0	Buffer Drive Strength Select for nOE pin
24	WEH	R/W	0	Buffer Drive Strength Select for nWE pin
23:0	XAH	R/W	0x000000	Buffer Drive Strength Select for XA[23:0] pins.

System Configuration (CFGSYS) 0x80000A60

Bit	Name	R/W	Reset	Description
31:17	Reserved	R/W	0x00000000	
16	CFGRSPERR	R/W	0	Error Response Enable. When enabled, ABORT is asserted to the CPU if undefined addresses are accessed.
15:0	Reserved	R/W	0x0000	Reserved for test. Must be written as zero.

13 DMA CONTROLLER

13.1 Overview

The TCC76x has 2-channel DMA controller for data transfer. The DMA can be used to perform high-speed transfers between external memory, on-chip memory, memory-mapped external devices, and on-chip peripheral module. It's possible to select channel priority levels with fixed priority or round-robin priority.
The block diagram of DMA controller is in the following figure.

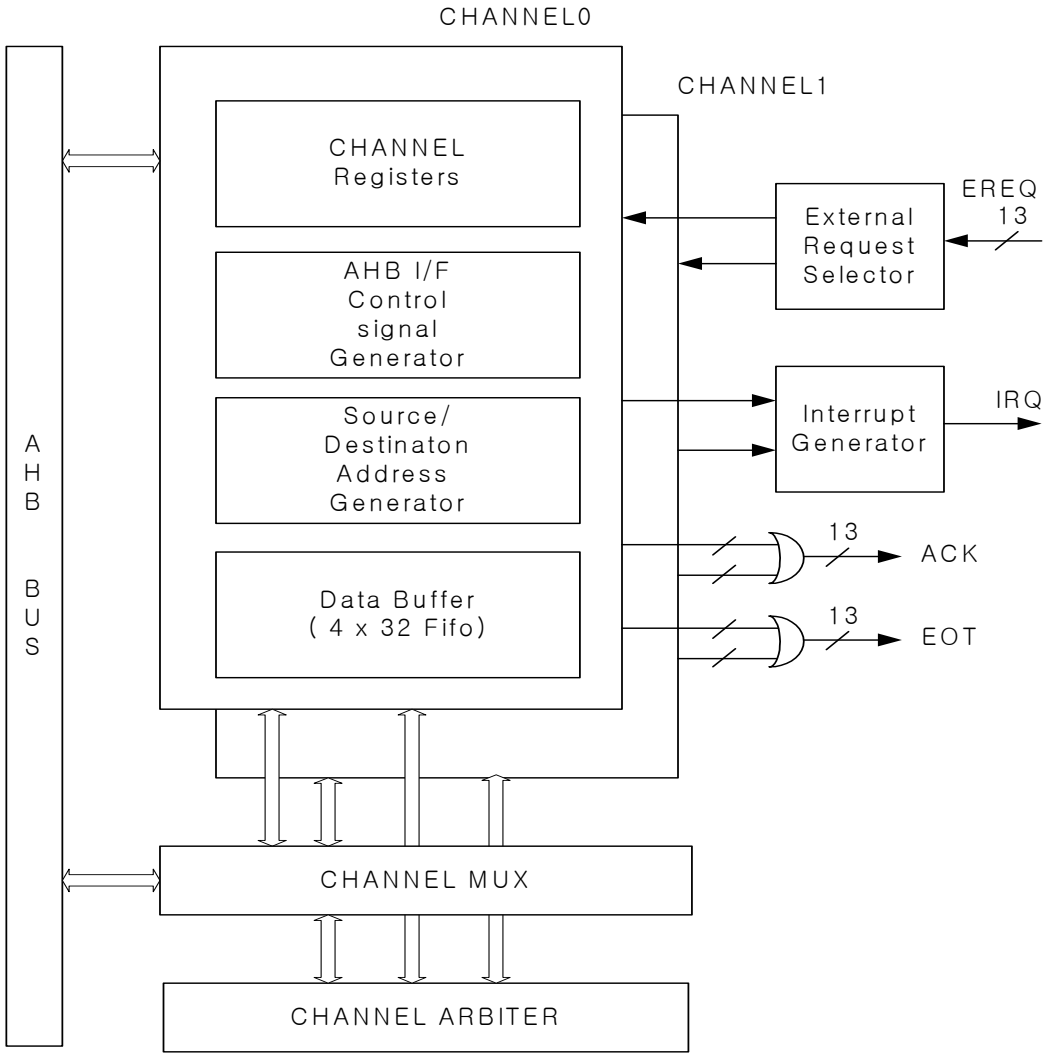


Figure 13.1 DMA Controller Block Diagram

13.2 Register Description

Table 13.1 DMA Controller Register Map (Base Address = 0x80000E00)

Name		Address	Type	Reset	Description
CHANNEL0	ST_SADR0	0x00	R/W	-	Start Address of Source Block
	SPARAM0	0x04/0x08	R/W	-	Parameter of Source Block
	C_SADR0	0x0C	R	-	Current Address of Source Block
	ST_DADR0	0x10	R/W	-	Start Address of Destination Block
	DPARAM0	0x14/0x18	R/W	-	Parameter of Destination Block
	C_DADR0	0x1C	R	-	Current Address of Destination Block
	HCOUNT0	0x20	R/W	0x00000000	Initial and Current Hop count
	CHCTRL0	0x24	R/W	0x00000000	Channel Control Register
CHCONFIG		0x2C	R/W	-	Channel Configuration Register
CHANNEL1	ST_SADR1	0x30	R/W	-	Start Address of Source Block
	SPARAM1	0x34/0x38	R/W	-	Parameter of Source Block
	C_SADR1	0x3C	R	-	Current Address of Source Block
	ST_DADR1	0x40	R/W	-	Start Address of Destination Block
	DPARAM1	0x44/0x48	R/W	-	Parameter of Destination Block
	C_DADR1	0x4C	R	-	Current Address of Destination Block
	HCOUNT1	0x50	R/W	0x00000000	Initial and Current Hop count
	CHCTRL1	0x54	R/W	0x00000000	Channel Control Register

Start Source Address Register (ST_SADR) **0x80000E00**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ST_SADR[31:16]															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ST_SADR[15:0]															

This register contains the start address of source memory block for DMA transfer. The transfer begins reading data from this address.

Start Destination Address Register (ST_DADR) **0x80000E10**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ST_DADR[31:16]															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ST_DADR[15:0]															

This register contains the start address of destination memory block for DMA transfer.

Source Block Parameter Register (SPARAM) **0x80000E04 / 0x80000E08**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SMASK[23:8]															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SMASK[7:0]								SINC[7:0]							

SMASK [31:8]	Source Address Mask Register
0	non-masked
1	Masked so that source address bit doesn't be changed during DMA transfer

Each bit field controls the dedicated bit of source address field. That is, if SMASK[23] is set to 1, the 28th bit of source address is masked, and if SMASK[22] is set to 1, the 27th bit of source

address is masked, and so on. If a bit is masked, a corresponding bit of address bus is not changed during DMA transfer. This function can be used to generate circular buffer address.

SINC [7:0]	Source Address Increment Register
sinc	Source address is added by amount of sinc at every write cycles. sinc is represented as 2's complement, so if SINC[7] is 1, the source address is decremented.

The addresses of DMA transfer have 32bit wide, but the upper 4bit of them are not affected during DMA transfer. If the source or destination address reaches its maximum address space like 0x7FFFFFFF or 0x2FFFFFFF, the next transfer is starting from 0x70000000 or 0x20000000 not from 0x80000000 or 0x30000000.

Destination Block Parameter Register (DPARAM) 0x80000E14 / 0x80000E18

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DMASK[23:8]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMASK[7:0]								DINC[7:0]							

DMASK [23:8]	Destination Address Mask Register
0	non-masked
1	Masked so that destination address bit doesn't be changed during DMA transfer

Each bit field controls the corresponding bit of source address field. That is, if DMASK[23] is set to 1, the 28th bit of source address is masked, and if DMASK[22] is set to 1, the 27th bit of source address is masked, and so on. If a bit is masked, a corresponding bit of address bus is not changed during DMA transfer. This function can be used to generate circular buffer address.

DINC [7:0]	Destination Address Increment Register
dinc	Destination address is added by amount of dinc at every write cycles. dinc is represented as 2's complement, so if DINC[7] is 1, the destination address is decremented.

The addresses of DMA transfer have 32bit wide, but the upper 4bit of them are not affected during DMA transfer. If the source or destination address reaches its maximum address space like 0x7FFFFFFF or 0x2FFFFFFF, the next transfer is starting from 0x70000000 or 0x20000000 not from 0x80000000 or 0x30000000.

Current Source Address Register (C_SADR) 0x80000E0C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C_SADR[31:16]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C_SADR[15:0]															

This register contains the current source address of DMA transfer. It represents that the current transfer read data from this address. This is read only register.

Current Destination Address Register (C_DADR) 0x80000E1C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C_DADR[31:16]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C_DADR[15:0]															

This register contains current destination address of DMA transfer. It represents that the current transfer write data to this address. This is read only register.

HOP Count Register (HCOUNT) 0x80000E20

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C_HCOUNT[15:0]															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ST_HCOUNT[15:0]															

C_HCNT [31:16]	Type	Current Hop Count
cn	R	Represent cn number of Hop transfer remains

ST_HCNT [15:0]	Type	Start Hop Count
sn	R/W	DMA transfers data by amount of sn Hop transfers

At the beginning of transfer, the C_HCNT is updated by ST_HCNT register. At the end of every hop transfer, this is decremented by 1 until it reaches to zero. When this reaches to zero, the DMA finishes its transfer and may or may not generate its interrupt according to IEN flag of CHCTRL register.

Channel Control Register (CHCTRL) 0x80000E24

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0			DMASEL[12:0]												
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CONT	0	SYNc	HRD	LOCK	BST	TYPE		BSIZE		WSIZE		FLAG	IEN	REP	EN

DMASEL [28:16]	Select Source of DMA Request
non-zero	Each bit field selects corresponding signal as a source for DMA request. The bit-map of this register is identical with the IEN of interrupt controller. So if you want to use EXINT0 pin as a source of DMA request, set DMASEL[0] as 1 and select transfer type of HW_ARBIT or HW_BURST. If multiple bits of this field are set, all the corresponding signal can generate DMA request for this channel.

CONT [15]	Issue Continuous Transfer
0	DMA transfer begins from ST_SADR / ST_DADR address
1	DMA transfer begins from C_SADR / C_DADR address It must be used after the former transfer has been executed, so that C_SADR and C_DADR contain a meaningful value.

SYNC [13]	Hardware Request Synchronization
0	Do not Synchronize Hardware Request.
1	Synchronize Hardware Request.

HRD [12]	Hardware Request Direction
0	ACK/EOT signals are issued when DMA-Read Operation.
1	ACK/EOT signals are issued When DMA-Write Operation.

LOCK [11]	Issue Locked Transfer
1	DMA transfer executed with lock transfer

Lock field controls the LOCK signal (refer to AHB specification). When the LOCK is set to 1, the DMA transfer doesn't be bothered by other AHB masters like LCD controller, ARM etc. This field is only meaningful in case of non-burst type transfers.

BST[10]	BURST Transfer
0	DMA transfer executed with arbitration.
1	DMA transfer executed with no arbitration. (burst operation)

Arbitration means that at the end of every HOP transfer, the AHB bus is released from DMA channel so other master can occupy the bus when that master has requested the bus.

Burst means that once the DMA request occurs, all of transfers are executed without further DMA requests.

TYPE [9:8]	Transfer Type
00	SINGLE transfer with edge-triggered detection
11	SINGLE transfer with level-sensitive detection
01	HW transfer
10	SW transfer

In SINGLE Type, After one Hop data transferring DMA checks External DMA Request (DREQ) and then if its bit is active , DMA transfers next hop data . DREQ is detected level-sensitive or edge-triggered by SINGLE transfer TYPE.
The 1 Hop of transfer means 1 burst of read followed by 1 burst of write. 1 burst means 1, 2 or 4 consecutive read or write cycles defined by BSIZE field of CHCTRL register. The Figure 13.2 illustrates the relation among the above transfers.

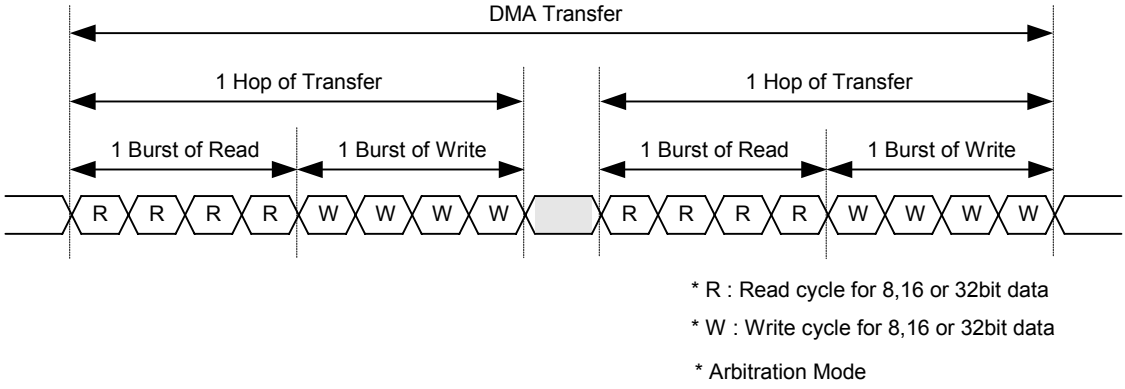


Figure 13.2 Relation between Hop and Burst Transfers (If burst size is 4.)

Hardware type transfer means that the DMA transfer triggered by external or internal hardware blocks selected by DMASEL field in CHCTRL register. This field has same mapping with interrupt enable flag of interrupt controller, so the DMA transfer can be occurred as like as interrupt is generated.

Software type transfer means that the DMA transfer triggered by EN bit of CHCTRL Register . When this is set to 1, transfer request signal is generated internally and then the transfer begins immediately.

Hardware demand type transfer (HW_DEMAND) means that once the DMA request occurs, DMA checks request signal each hop transfer, and if request signal is set, DMA transfer one hope's data. After transferring all hope's data, DMA operation will be finished.

Figure 13.3 is the example of various types of transfer.

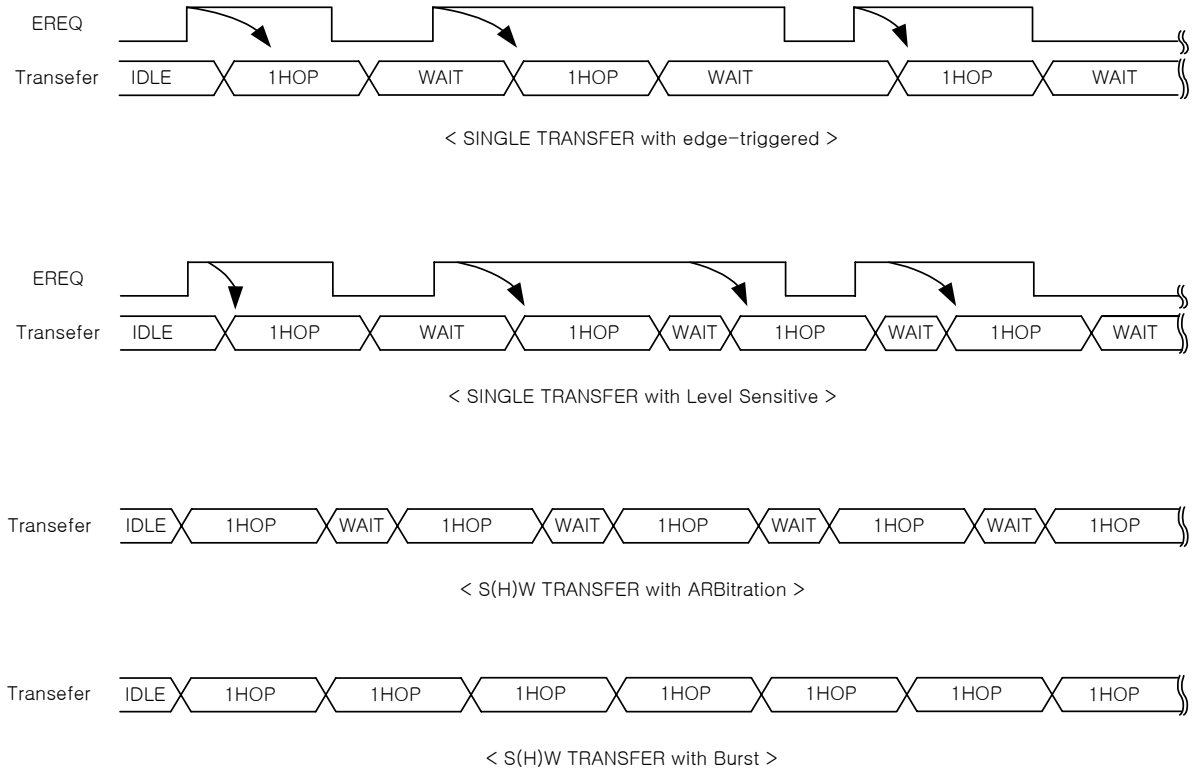


Figure 13.3 The Example Of Various Types of Transfer.

BSIZE [7:6]	Burst Size
0	1 Burst transfer consists of 1 read or write cycle.
1	1 Burst transfer consists of 2 read or write cycles
2, 3	1 Burst transfer consists of 4 read or write cycles

WSIZE [5:4]	Word Size
0	Each cycle read or write 8bit data
1	Each cycle read or write 16bit data
2, 3	Each cycle read or write 32bit data

FLAG [3]	Type	DMA Done Flag
1	R	Represents that all hop of transfers are fulfilled.
1	W	Clears FLAG to 0

It does not automatically cleared by another transfer starts, so before starting any other DMA transfer, user must clear this flag to 0 for checking DMA status correctly.

IEN [2]	Interrupt Enable
1	At the same time the FLAG goes to 1, DMA interrupt request is generated.

To generate IRQ or FIQ interrupt, the DMA flag of IEN register in the interrupt controller must be set to 1 ahead.

REP [1]	Repeat Mode Control
0	After all of hop transfer has executed, the DMA channel is disabled
1	The DMA channel remains enabled. When another DMA request has occurred, the DMA channel start transfer data again with the same manner (type, address, increment, mask) as the latest transfer of that channel.

EN [0]	DMA Channel Enable
0	DMA channel is terminated and disabled. It does not affect the HCOUNT register, so if the current hop counter is not zero when channel is disabled, it is possible that the transfer illegally starts right after channel is re-enabled. Make sure that HCOUNT is zero not to continue transfer after channel is re-enabled.
1	DMA channel is enabled. If software type transfer is selected, this bit generates DMA request directly, or if hardware type transfer is used, the selected interrupt request flag generate DMA request.

Channel Configuration Register(CHCONFIG) **0x80000E2C**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
									IS1	IS0				MIS1	MIS0
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
						SWP1	SWP0				PRI				FIX

IS1 [22]	Channel 1 Alternate interrupt status
0	No interrupt in channel 1
1	Channel1 Interrupt is occurred

Without regard to Interrupt enable bit(IEN) of channel1, this bit indicates the channel1 interrupt status.
This bit is automatically cleared when FLAG bit of channel1 is cleared. This bit is read only.

IS0 [21]	Channel 0 Alternate interrupt status
0	No interrupt in channel 0
1	Channel1 Interrupt is occurred

Except for channel difference, This bit is the same as IS1 bit.

MIS1[17]	Channel1 Masked Interrupt Status
0	Masked interrupt is not occurred in channel 1
1	Channel1 Masked Interrupt is occurred

This bit is set when channel1 interrupt occurs and interrupt enable bit (IEN) of channel1 is set.
This bit is automatically cleared when FLAG bit of channel1 is cleared. This bit is read only.

MIS0[16]	Channel0 Masked Interrupt Status
0	Masked interrupt is not occurred in channel 0
1	Channel0 Masked Interrupt is occurred

Except for channel difference, This bit is the same as MIS1 bit.

SWP1 [9]	Channel1 SWAP Enable bit
0	Do not Swap Channel1 Data.
1	Swap Channel1 Data.

When this bit is set, data to be written to destination address will be swapped.
For example, the 32bit source data which consists of 4bytes {D3,D2,D1,D0} will be stored {D0,D1,D2,D3} in destination address. The 16bit source data which consists of 2bytes {D1,D0} will be stored {D0,D1} in destination address.

SWP0[8]	Channel0 SWAP Enable bit
0	Do not Swap Channel0 Data.
1	Swap Channel0 Data.

Except for channel difference, the function controlled by this bit is the same as its SWP1 bit.

PRI[4]	PRIORITY
0	CHANNEL0 is the Highest Priority in FIXed mode.
1	CHANNEL1 is the Highest Priority in FIXed mode.

FIX [0]	Fixed Priority Operation
0	Round-Robin (Cyclic) Mode.
1	Fixed Priority Mode.

In round-robin mode, Each channel is enabled one by one every one hop transferring.
In Fixed mode, according to PRI bit, the highest channel is serviced first and lower priority channel is serviced after higher priority channel operation is finished. See Figure 13.4 for more information.

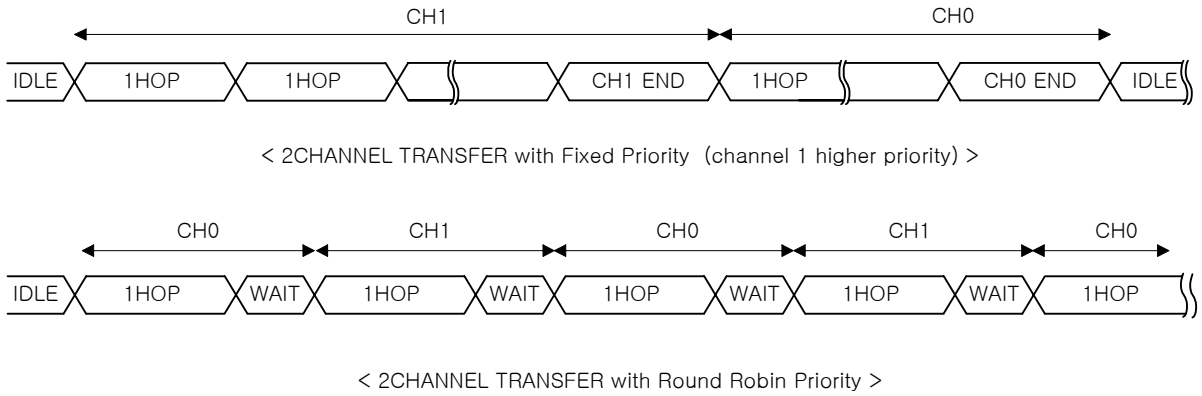


Figure 13.4 Enabled 2Channel Transfer.

The CHANNEL1 Registers are not described in detail in this data sheet.
The function of CHANNEL1 Registers are the same as CHANNEL0 Register except for channel difference and assigned address.

14 LCD CONTROLLER

14.1 Overview

The LCD controller (LCDC) is used to send out the image data from system memory to a LCD panel or NTSC/PAL encoder by properly formatting the raw image data stored in the memory. This LCDC provides all the necessary control signals to interface directly to mono STN, color STN, TFT panels, and NTSC/PAL encoders. Figure 14.1 shows LCDC block diagram and Figure 14.2 shows LCDC pin mappings.

The features of the LCDC are:

- supports Thin Film Transistor(TFT) color displays with 16-bit interface
- supports Super Twisted Nematic(STN) displays with 4 or 8-bit interfaces
- 1, 2 or 4 bits per pixel(bpp) displays for mono STN
- 8 /16 bpp color displays for color STN
- 16 bpp true-color non-palletized color displays for color TFT
- resolution programmable up to 1024 * 1024
- programmable timing for different display panels
- NTSC/PAL digital video encoder interface

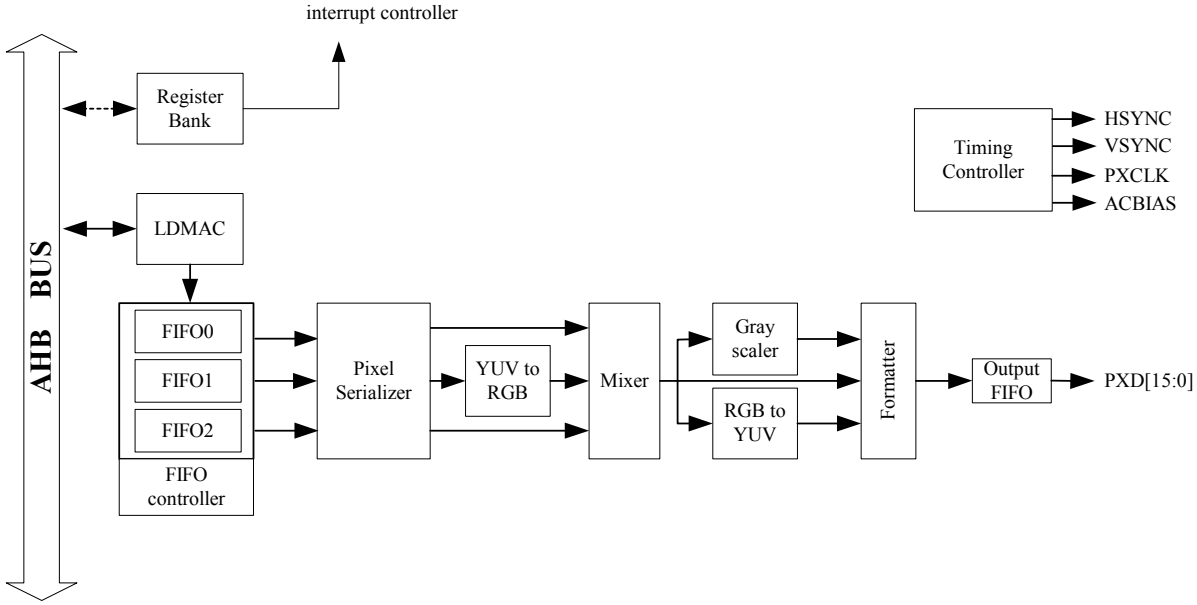


Figure 14.1 LCD controller Block Diagram

Signal name	GPIO
HSYNC	GPIO_B17
VSYNC	GPIO_B18
PXCLK	GPIO_B19
ACBIAS	GPIO_B20
PXDATA[15:0]	GPIO_A[31:16]

Figure 14.2 PIN mapping

The following key parameters can be programmed:

- horizontal front and back porch
- horizontal synchronization pulse width
- number of panel clocks per line
- vertical front and back porch
- vertical synchronization pulse width
- number of lines per panel
- signal polarity
- panel clock frequency
- AC panel bias
- STN mono 1, 2, 4bpp
- STN color 8bpp(palletized, 256colors from 3375), 16bpp(direct 4:4:4RGB)
- STN 4 or 8-bit interface mode
- TFT LCD
- NTSC/PAL, Interlace/Non-interlace mode
- YUV2RGB, RGB2YUV

Encoded pixel data are stored in off-chip memory in the frame buffer and are transferred to the LCDC's input FIFO, on a demand basis, using the AMBA AHB master interface.

The LCDC issues a service request to the DMA after it has been initialized and enabled. The DMA automatically performs burst word transfers, filling empty entries of the FIFO. Values are fetched from the bottom of the FIFO, one entry at a time, and each 32-bit value is unpacked into individual pixel encodings, of 1, 2, 4, 8 or 16 bits each. After value is removed from the FIFO, the entries are invalidated.

The frame buffer is in an off-chip memory area used to supply enough encoded pixel values to fill the entire screen one or more times. The pixel data buffer contains one encoded pixel values for each of the pixels present on the screen. The number of pixel data values depends on the size of the screen. Figure 14.4 shows the memory organization within the frame buffer for each size pixel encoding.

14.2 Related Blocks

Before using LCDC, it needs to configure blocks which are related to LCDC.

First, timing control signals and pixel data signals of LCDC use GPIO_B[20:17] and GPIO_A[31:16]. Figure 14.2 shows GPIO mapping. Therefore, these GPIO ports must be configured to LCD function and output mode. *GPIO* part explains these configurations in detail. Figure 14.3 shows output pixel data organization on GPIO[31:16].

Second, LCLK, which is the main clock of LCDC, must be enabled and configured to the proper frequency. HCLK frequency must be higher than LCLK frequency. Otherwise, FIFO underrun is occurred. In case of FIFO underrun, HCLK frequency must be set to faster value and/or LCLK frequency must be set to slower value.

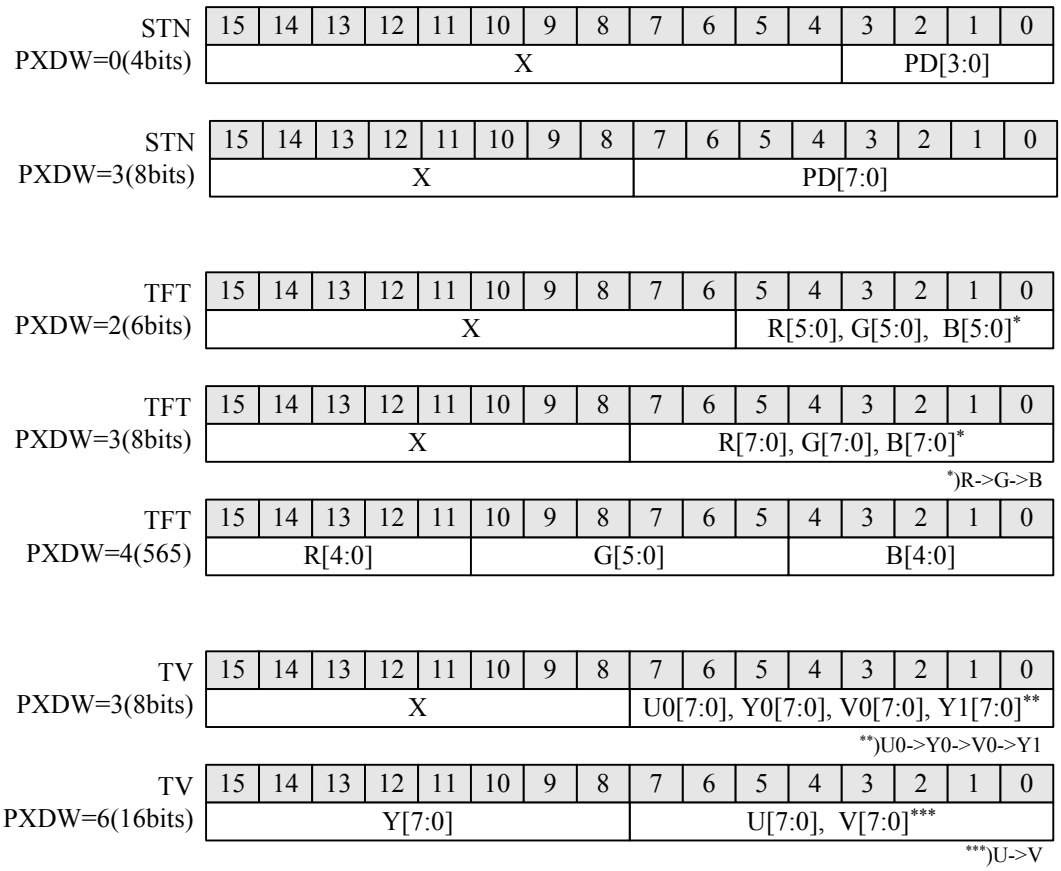


Figure 14.3 Output Pixel Data Organization(GPIO_A[31:16] = PXDATA[15:0])

14.3 Interrupt configuration

LCDC has three maskable interrupt sources; Disable Done(DD), Register Update(RU), and FIFO underrun interrupt(FU). Each interrupt source can be masked as corresponding bit of LIM is set to 1. DD interrupt is generated when LEN bit is cleared and current frame is completed. RU interrupt is generated after all of control registers are updated. So, control registers which was programmed are applied to displaying a frame after displaying the current frame is completed. FU interrupt is generated when FIFO underrun is occurred. HCLK frequency is always faster than LCLK frequency to prevent FIFO underrun from taking place.

For using LCDC interrupt, all of LCDC interrupt source must be cleared before enabling interrupt. The corresponding bits of LSTATUS are written to 1 to clear it. And CREQ register of interrupt controller must be also cleared.

1. clear LSTATUS register of LCDC
2. clear CREQ of interrupt controller
3. set LIM register of LCDC to unmask the corresponding LCDC interrupt.
4. set IEN register of interrupt controller to enable the LCDC interrupt

Whenever LCDC interrupt is generated, the corresponding bits of LSTATUS register must be cleared. Otherwise, LCDC interrupt is not generated any more.

14.4 STN LCD

The LCDC generates VSYNC, HSYNC, PXCLK, ACBIAS, and PXDATA signals for STN LCD driver.

Figure 14.4 shows 1bpp, 2bpp, 4bpp, 8bpp, and 16bpp of PXDATA memory organization. BR of LCTRL register indicates whether pixel data in frame memory is big-endian for 1bpp, 2bpp, or 4bpp mode. Figure 14.5 shows RGB configuration for color STN LCD.

The timing diagram for STN mode is shown in Figure 14.7. VSYNC and HSYNC pulse are controlled by the configurations of the LPC field of LHTIME and FLC field of LVTIME1 and LVTIME2. Each field is related to the LCD size and display mode.

In 1bpp, 2bpp, 4bpp:

LPC *=(Horizontal display size / pixel data width) – 1*

In 8pp and 16bpp (RGB):

LPC *= {3 * Horizontal display size / (pixel data width) – 1}*

Pixel data width is determined by PXDW of LCTRL register. In the case of STN LCD mode, it must be 4 or 8-bit width.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
1BPP	p31	p30	p29	p28	p27	p26	p25	p24	p23	p22	p21	p20	p19	p18	p17	p16
2BPP	p15		p14		p13		p12		p11		p10		p9		p8	
4BPP	p7				p6				p5				p4			
8BPP	p3								p2							
16BPP	p1															

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1BPP	p15	p14	p13	p12	p11	p10	p9	p8	p7	p6	p5	p4	p3	p2	p1	p0
2BPP	p7		p6		p5		p4		p3		p2		p1		p0	
4BPP	p3				p2				p1				p0			
8BPP	p1								p0							
16BPP	p0															

a) BR=0

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
1BPP	p24		p25		p26		p27		p28		p29		p30		p31	
2BPP	p12				p13				p14				p15			
4BPP	p6								p7							
8BPP	p3															
16BPP	p1															

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1BPP	p8		p9		p10		p11		p12		p13		p14		p15	
2BPP	p4				p5				p6				p7			
4BPP	p2								p3							
8BPP	p1															
16BPP	p0															

b) BR=1

Figure 14.4 STN LCD pixel data organization

	7	6	5	4	3	2	1	0
STN 8BPP	R[1:0]		G[2:0]			B[2:0]		

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STN 16BPP	X				R[3:0]				G[3:0]				B[3:0]			

Figure 14.5 Color STN Pixel Data

ACBIAS signal is used by the LCD driver to alternate the polarity of the row and column voltage used to turn the pixel on and off. It is controlled by the ACDIV field of LCLKDIV register. This value must be (lpw+1) times.

$$ACDIV = \{(lpw+1) * n\} - 1$$

n = number of HSYNC(CL1)

PXCLK frequency is determined by the CLKDIV field of LCLKDIV register as follows. The minimum value of CLKDIV is 3 in STN mode.

$$f_{PXCLK} = f_{LCLK} / (2 * CLKDIV) \quad (1)$$

VSYNC frequency is related to the field of FEWC, LSWC, LEWC, LPC, and FLC as well as LCLK and PXCLK.

$$f_{VSYNC} = f_{PXCLK} / [\{(LPW+1) + (LPC+1) + (LSWC+1) + (LEWC+1)\} * \{(FLC + 1) + (FPW+1)\}]$$

Therefore, if FR is the required refresh rate, f_{PXCLK_REQ}, which is the required PXCLK, is the flowing.

$$f_{PXCLK\_REQ} = FR \times [\{(LPW+1) + (LPC+1) + (LSWC+1) + (LEWC+1)\} * \{(FLC + 1) + (FEWC+1)\}] \quad (2)$$

The LCDC contains dithering pattern registers for STN LCD: a 48-bit modulo 7 dithering pattern register (LDP7L and LDP7H), a 32-bit modulo 5 dithering pattern register (LDP5), a 16-bit modulo 4 dithering pattern register (LDP4), and a 16-bit modulo 3(LDP3) dithering pattern register. These dithering pattern registers can contain the programmable

pre-dithered pattern values for each duty cycle ratio. Bits per pixel of image determines pre-dithered value.

If BPP is 4 or 16, pre-dithered value is non-palettized value, which is pixel data in the frame memory. If BPP is 2, a nibble of LUTBL that is indexed by 2-bit pixel data is pre-dithered value. If BPP is 8, each nibble of LUTRD, LUTGR, and LUTBL that is indexed by pixel data, which consist of 3-bit R, 3-bit G, and 2-bit B, is pre-dithered value. Figure 14.6 shows the relationship between pre-dithered values and dithering pattern registers.

The LDP7H and LDP7L contain 5 pre-dithered patterns for 1/7, 3/7, 4/7, 5/7, and 6/7 duty cycle rate. Each field of LDP7H and LDP7L is 7-bit long. The LDP5 has 4 pre-dithered pattern fields for 1/5, 2/5, 3/5, and 4/5 duty cycle rate. Each field of LDP5 is 5-bit long. The LDP4 has 3 pre-dithered pattern fields for 1/4, 1/2(=2/4), and 3/4 duty cycle rate, and each field is 4-bit long. Likewise, the LDP3 has 2 fields for 1/3 and 2/3 duty cycle rate with 3-bit length.

Note that the pre-dithered data for 1 and 0 is not defined in the dithering pattern register, because these values are implemented with VDD and VSS condition.

Pre-dithered value	Dithering register	Duty cycle ratio
0	0	0
1	DP1_7	1/7
2	DP1_5	1/5
3	DP1_4	1/4
4	DP1_3	1/3
5	DP2_5	2/5
6	DP3_7	3/7
7	DP2_4	1/2
8	DP4_7	4/7
9	DP3_5	3/5
10	DP2_3	2/3
11	DP5_7	5/7
12	DP3_4	3/4
13	DP4_5	4/5
14	DP6_7	6/7
15	1	1

Figure 14.6 Dithering operation

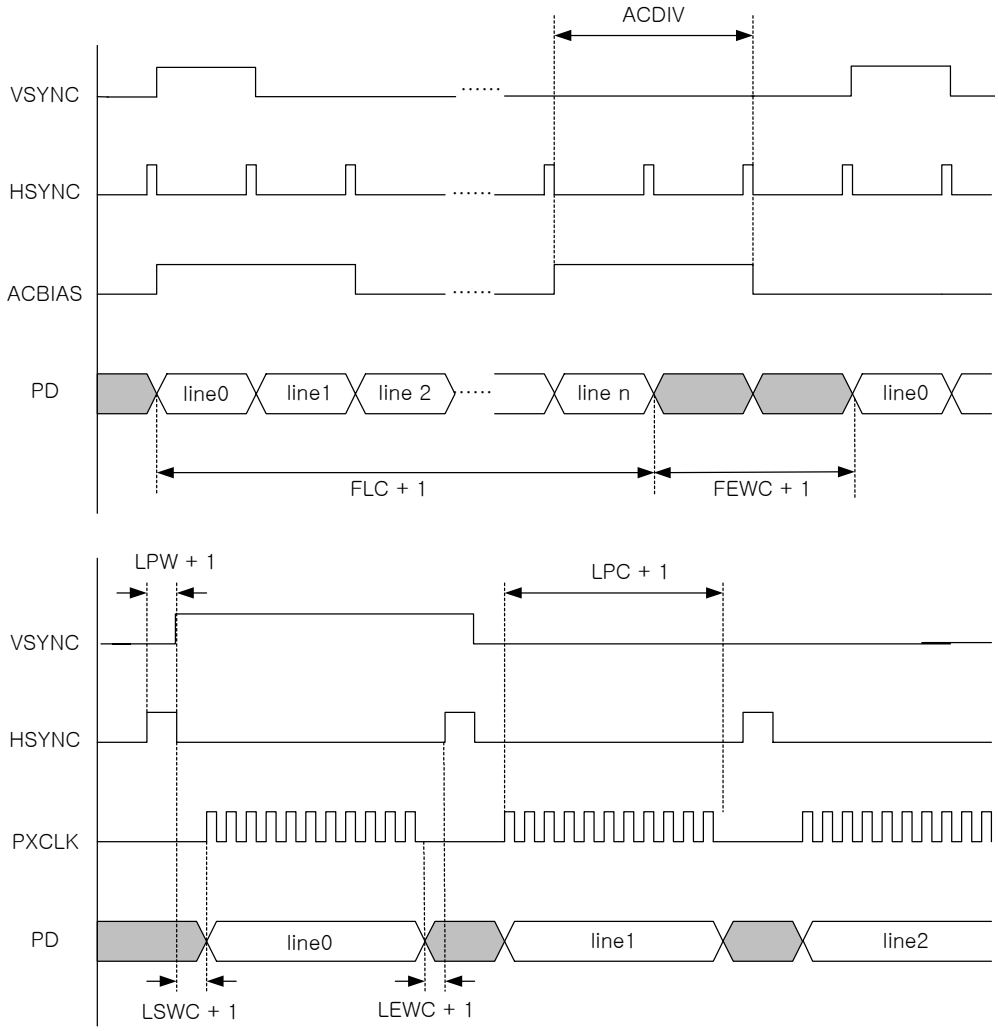


Figure 14.7 STN mode timing

Example

For a monochrome STN LCD, 4-bit interface panel, 4 pixels are captured by the panel in every panel clock cycle. Figure 14.8 gives the major registers to be programmed for supporting 4-bit interface STN LCD. LCLK and Refresh rate are examples only. And LSWC, LEWC, LPW, and FEWC are STN LCD panel dependent.

LCLK = 20 MHz, Refresh rate = 60 Hz
PXDW* = 0 (4bits)
VD* = 1
BPP* = 2 (4bpp)
DP* = 0 (one pixel data per pixel clock cycle)
NI = 1
TV* = 0, TFT* = 0, STN* = 1
LSWC* = LEWC* = LPW* = FEWC* = 1 (STN LCD dependent)

Width (pixel)	Height (pixel)	LPC*	FLC*	DHSIZE*	DVSIZE*	$F^{**}_{PXCLK\_REQ}$	CLKDIV*	f_{PXCLK}***
160	160	39	159	160	160	0.393	25	0.4
160	200	39	199	160	200	0.491	20	0.5
320	200	79	199	320	200	0.973	10	1

.*) control registers to be programmed. **) Refer to expression (2). ***) Refer to expression (1).

Figure 14.8 Monochrome STN LCD(4bits, 1BPP) example

14.5 TFT LCD

The LCDC supports 16bpp true-color non-palletized color displays for color TFT LCD. Figure 14.9 show frame memory organization. If image source is YUV420 or YUV422, YUV2RGB converer can be used as Y2R of LCTRL is set. And each YUV channel is indicated by LIBA0, LIBA1, and LIBA2 register.
It generates the control signals for LCD driver such as, VSYNC, HSYNC, PXCLK, PXDEN(ACBIAS) and PXDATA. Figure 14.10 shows PXDATA format in TFT mode. The timing diagram of TFT mode is shown in Figure 14.12.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RGB555	I*	R1[4:0]					G1[4:0]					B1[4:0]				
RGB565	R1[4:0]						G1[5:0]					B1[4:0]				
8BPP(U or V)	U6 or V6								U4 or V4							
8BPP(Y)	Y3								Y2							

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RGB555	I*	R0[4:0]					G0[4:0]					B0[4:0]				
RGB565	R0[4:0]						G0[5:0]					B0[4:0]				
8BPP(U or V)	U2 or V2								U0 or V0							
8BPP(Y)	Y1								Y0							

Figure 14.9 TFT LCD pixel data memory organization

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PXDW 565	R[4:0]					G[5:0]						B[4:0]				
PXDW 555	I*	R[4:0]					G[4:0]					B[4:0]				

*) intensity bit

Figure 14.10 TFT LCD output pixel data

The VSYNC and HSYNC frequency is controlled by the LPC and FLC field.

LPC = (Horizontal display size) – 1
FLC = (Vertical display size) – 1

And PXCLK frequency is determined by the CLKDIV value.

$$f_{PXCLK} = f_{LCLK} / (2 \times CLKDIV) \quad (3)$$

The frequency of VSYNC signal is the frame rate. So the frame rate can be calculated as follows:

$$f_{VSYNC} = f_{PXCLK} / [\ (FSWC + FPW + FLC + FEWC) \times \{(LSWC+1) + (LPC+1) + (LEWC+1) + (LPW+1)\}]$$

Therefore, if FR is the required refresh rate in TFT mode, f_{PXCLK_REQ}, which is the required PXCLK, is the flowing.

$$f_{PXCLK\_REQ} = FR \times \{(LPW+1) + (LPC+1) + (LSWC+1) + (LEWC+1)\} \times \{(FSWC+1) + (FPW+1) + (FLC+1) + (FEWC+1)\} \quad (4)$$

Example

TFT LCD(RGB565), LCLK = 80MHz and Refresh rate = 60Hz,

PXDW* = 0x4, YUV* = 0, BPP* = 0x4, DP* = 0, NI* = 1
TV* = 0, TFT* = 1, STN* = 0
LSWC* = LEWC* = LPW* = 3 (TFT LCD dependent)
FSWC* = FEWC* = FPW* = 1 (TFT LCD dependent)

Width (pixel)	Height (pixel)	LPC*	FLC*	DHSIZE*	DVSIZE*	F_{PXCLK_REQ}**	CLKDIV*	f_{PXCLK}***
176	220	175	219	176	220	2.55	15	2.67
240	320	239	319	240	320	4.93	8	5
640	480	639	479	640	480	19.01	2	20

.*) control registers to be programmed. **) Refer to expression (4). ***) Refer to expression (3).

Figure 14.11 TFT LCD(RGB565) example

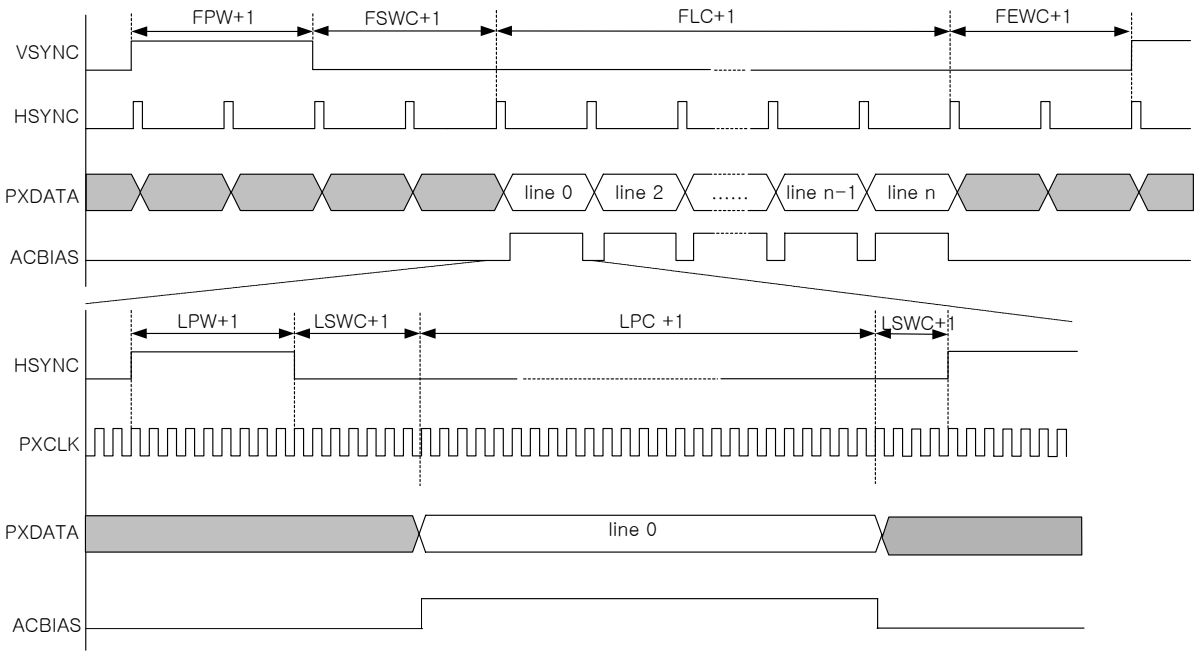


Figure 14.12 TFT mode timing

14.6 NTSC/PAL interface

The LCDC can generate the control signals for 8-bit or 16-bit NTSC/PAL encoder. The pixel color mapping of NTSC/PAL mode is identical to that of 8-bit or 16-bit LCD interfacing.

For NTSC/PAL interface, TV field of LCTRL register must be set. Registers used in this mode are similar to those in TFT mode except for LVTIME1 and LVTIME2 registers.; LVTIME1 is for odd field and LVTIME2 is for Even field. And these registers value is not based on HSYNC, but based on half of HSYNC. For example, if FPW of LVTIME1 is 3, pulse width of VSYNC on odd field is not 4 HSYNC cycles, but 2 HSYNC cycles. And if FPW of LVTIME1 is 4, it represents to 2.5 HSYNC cycles.

Interlace/Non-interlace mode can be configured by NI field of LCTRL register. Figure 14.13 and Figure 14.14 each show the timing diagram of NTSC and PAL interlace mode. In non-interlace mode, odd field sync signals are repeated instead.

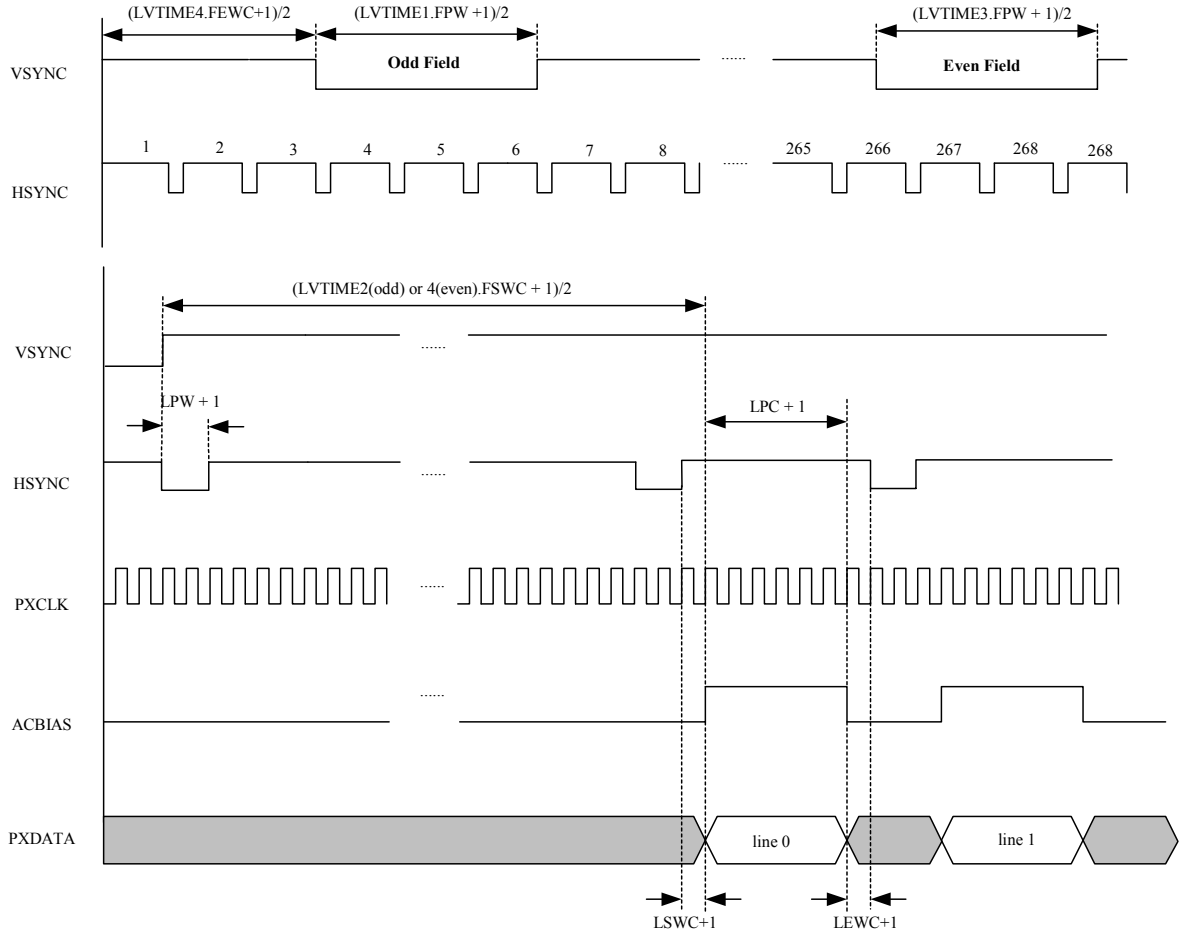


Figure 14.13 NTSC interlace mode timing

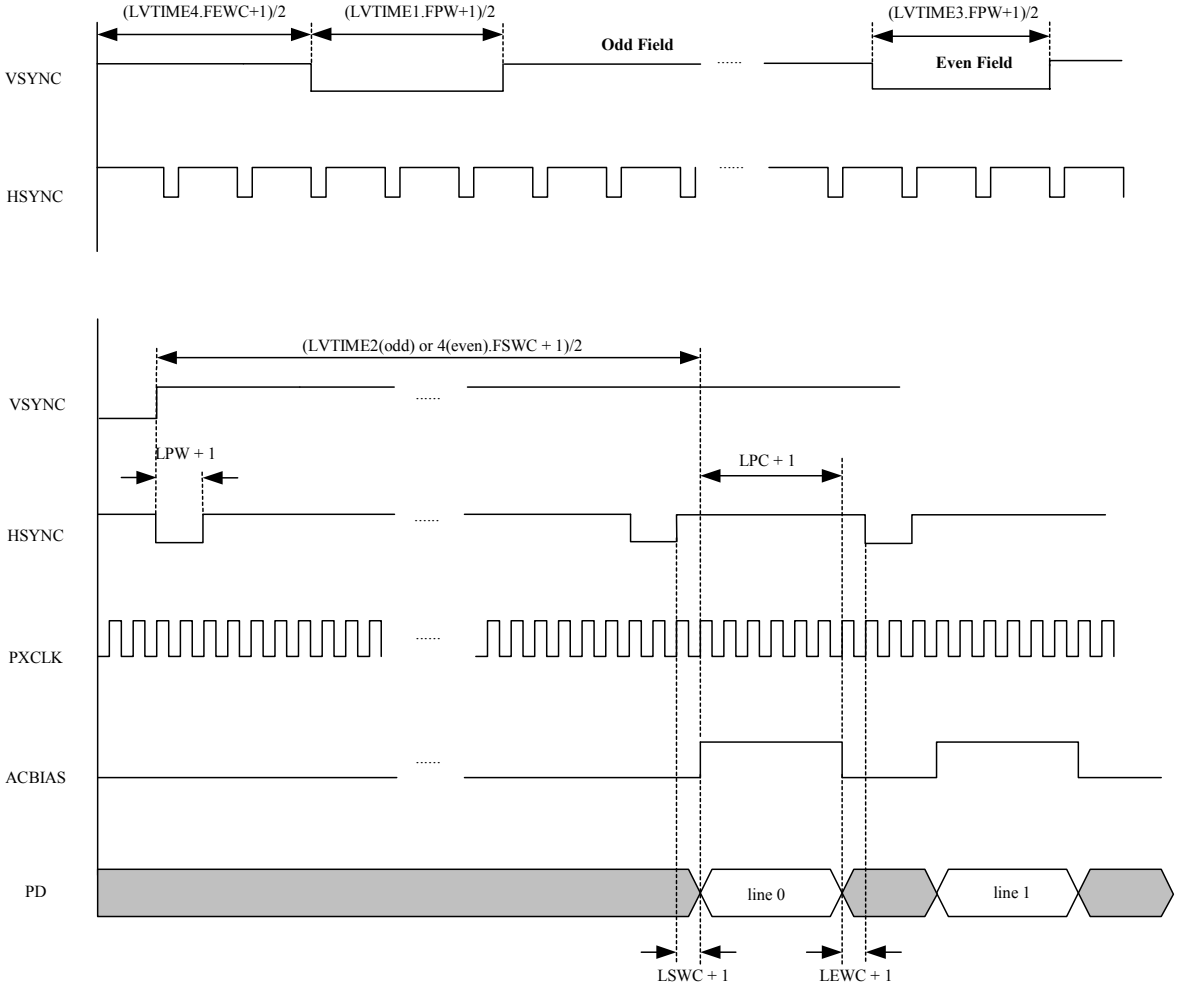


Figure 14.14 PAL interlace mode timing

Example

The frame memory has RGB565 type image source. The following code fragment gives the major registers to be programmed for NTSC encoder interface.
HCLK = 72MHz, LCLK = 54MHz, PXCLK=27MHz

LCTRL = 0x041E8E03
LCTRL.YUV = 0 (RGB)
LCTRL.BPP = 0x4 (RGB565)
LCTRL.R2Y = 0x1
LCTRL.DP = 0x1
LCTRL.PXDW = 0x6 (16bits)
LCTRL.TV = 0x1
LCTRL.IAC = 0x0
LCTRL.IVS = 0x1
LCTRL.IHS = 0x1
LCTRL.IPX = 0x1
LCTRL.NI = 0x0
LCTRL.DEN = 0x1

LCTRL.LEN = 0x1

LCLKDIV = 1
LHTIME1.LPW = 128-1
LHTIME1.LPC = 1440-1
LHTIME2.LSWC = 116-1
LHTIME2.LEWC = 32-1
LVTIME1.FPW = 3*2 –1
LVTIME1.FLC = 240*2 – 1
LVTIME2.FSWC = 15*2 –1
LVTIME2.FEWC = 4*2+1 –1
LVTIME3.FPW = 3*2-1
LVTIME3.FLC = 240*2 –1
LVTIME4.FSWC=15*2+1-1
LVTIME4.FEWC=4*2-1

LIP.X = 0
LIP.Y = 0
LIS.WIDTH = LDS.VSIZE = 720
LIS.HEIGHT = LDS.HSIZE = 480

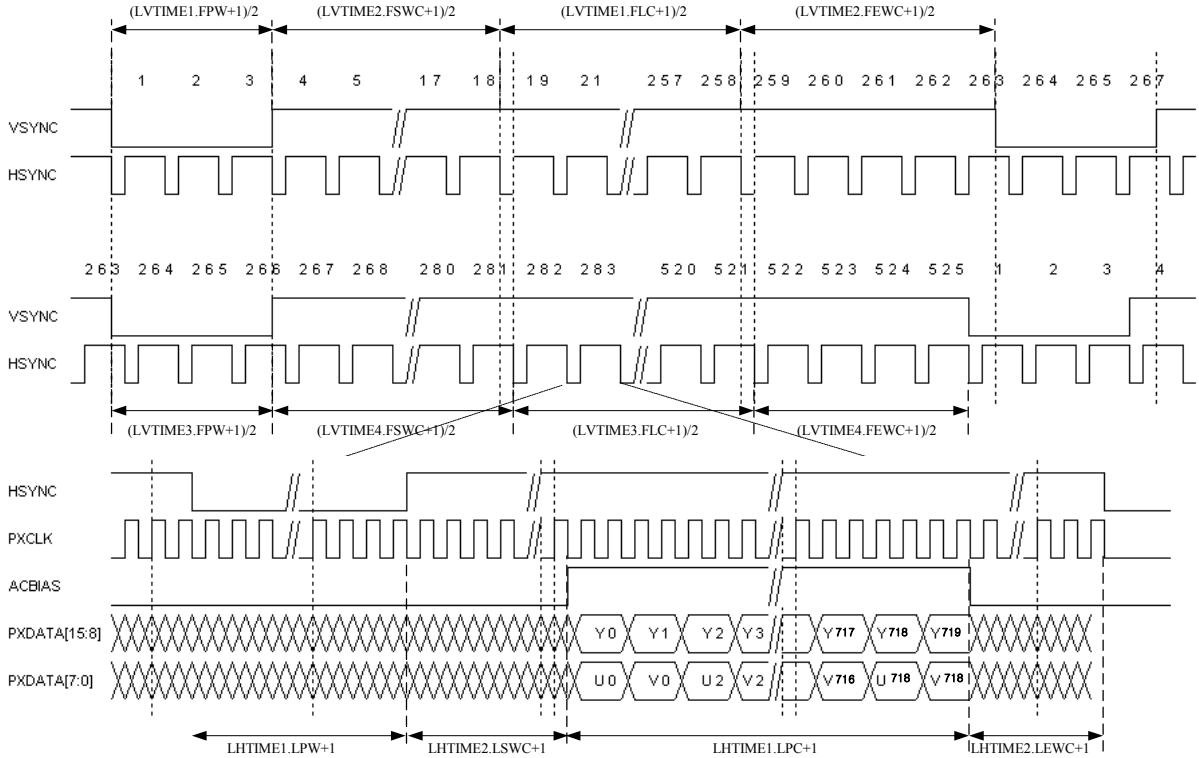


Figure 14.15 Example: NTSC interlace mode timing diagram

14.7 Register Description

Table 14.1 LCD Controller Register Map (Base Address = 0x80000F00)

Name	Address	Type	Reset	Description
LCTRL	0x00	R/W	0x00000006	control register
LCLKDIV	0x04	R/W	0x00000000	ac-bias clock and pixel clock divisor
LHTIME1	0x08	R/W	0x00000000	Horizontal axis timing control register1
LHTIME2	0x0C	R/W	0x00000000	Horizontal axis timing control register2
LVTIME1	0x10	R/W	0x00000000	Vertical axis timing control register1
LVTIME2	0x14	R/W	0x00000000	Vertical axis timing control register2
LVTIME3	0x18	R/W	0x00000000	Vertical axis timing control register3
LVTIME4	0x1C	R/W	0x00000000	Vertical axis timing control register4
LLUTRD	0x20	R/W	0x00000000	Lookup table for red color
LLUTGR	0x24	R/W	0x00000000	Lookup table for green color
LLUTBL	0x28	R/W	0x00000000	Lookup table for blue color
LDP7L	0x2C	R/W	0x4D2B3401	modulo 7 dithering pattern low register
LDP7H	0x30	R/W	0x0000003F	modulo 7 dithering pattern high register
LDP5	0x34	R/W	0x1D0B0610	modulo 5 dithering patterns
LDP4	0x38	R/W	0x00000768	modulo 4 dithering patterns
LDP3	0x3C	R/W	0x00000034	Modulo 3 dithering patterns
LDS	0x40	R/W	0x00000000	Display size register
LSTATUS	0x44	R/Clear	0x00000000	Status register
LIM	0x48	R/W	0x00000007	Interrupt mask register
LIP	0x4C	R/W	0x00000000	Image position register
LIS	0x50	R/W	0x00000000	Image size register
LIBA0	0x54	R/W	0x00000000	Image base address register 0
LICA0	0x58	R	0x00000000	Image current address register
LIBA1	0x5C	R/W	0x00000000-	Image base address register 1
LIBA2	0x60	R/W	0x00000000	Image base address register 2

LCD Control Register (LCTRL) **0x80000F00**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
		YUV[1:0]		BPP[3:0]					BR	Y2R	R2Y	DP	PXDW[2:0]		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TV			IAC	IVS	IHS	IPX		NI			TFT	STN		DEN	LEN

YUV [29:28]*	YUV data type
00	RGB
01	YUV 4:2:0
11	YUV 4:2:2

*) When it is YUV 4:2:0 or YUV 4:2:2, BPP must be 8bpp.

BPP [27:24]	Bits Per Pixel
0000	1 bpp
0001	2 bpp
0010	4 bpp
0011	8 bpp*
0100	RGB565
0101	RGB555
0111	RGB444 (STN only)

*) When it is YUV 4:2:0 or YUV 4:2:2, BPP must be 8bpp.

BR[22]*	Bit-Reverse
0	Little-endian pixel data
1	Big-endian pixel data

*) It is only used when BPP is 1, 2, or 4bpp.

Y2R[21]	YUV to RGB converter
0	Disable
1	Enable

R2Y[20]	RGB to YUV converter
0	Disable
1	Enable

DP[19]	Double Pixel Data
0	One pixel data every one PXCLK cycle is output.
1	One pixel data every two PXCLK cycle is output. It is for 16-bit TV mode.

PXDW [18:16]	Pixel Data Width
000	4 bits
010	6 bits
011	8bits
100	16bits(RGB565)
101	16bits(RGB555)
110	16bits(YUV)

IAC [12]	Inverted ACBIAS signal
0	Normal
1	Inverted

IVS [11]	Inverted VSYNC signal
0	Normal
1	Inverted

IHS[10]	Inverted HSYNC signal
0	Normal
1	Inverted

IPX [9]	Inverted Pixel Clock
0	Data is driven onto the LCD's data pins on the rising edge of pixel clock pin
1	Data is driven onto the LCD's data pins on the falling edge of pixel clock pin

NI [7]	Non-interlace
0	Interface mode. Odd field timing control: LVTIME1, LVTIME2 Even field timing control: LVTIME3, LVTIME4
1	Non-interlace mode LVTIME1 and LVTIME3 must be same, and LVTIME2 and LVTIME4 must be same.

TV[15]	TFT [4]	STN [3]	Description
0	0	1	Select STN-LCD mode
0	1	0	Select TFT-LCD mode
1	0	0	Select TV mode In this mode, all values of LVTIMEn registers are divided by 2. Therefore, if LVTIME1.FPW is set to 5 HSYNC cycles, LVTIME1.FPW is programmed to 9(= 5*2 – 1).

Other combinations are undefined and should not be used.

DEN [1]	Pixel Data Transfer Enable
0	Disable If LEN is enabled, LCD controller only generates timing control signals.
1	Enable

Normally, DEN must be always enabled to operate LCD controller and display pixel data on LCD. Some LCD modules, however, have their own frame memory. In this case, if the current frame is the same with previous frame, it needs not to be transferred to LCD module for reducing power-consumption and bus-bandwidth.

LEN [0]	LCD controller Enable
0	Disable
1	Enable

LCD Clock Divider Register (LCLKDIV) **0x80000F04**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ACDIV								CLKDIV							

FIELD	Description
ACDIV [15:8]	AC Bias clock divisor(STN only). The number of clock cycles to count between each toggle of AC_BIAS pin.. ACBIAS is toggled every n HSYNC cycles if ACDIV is {(lpw+1) *n – 1}.
CLKDIV [7:0]	Pixel clock divisor Note that programming CLKDIV less than 3 is illegal for STN LCD. *PXCLK = LCLK / (2*CLKDIV)* *(if CLKDIV = 0, PXCLK = LCLK)*

LCD Horizontal Timing Register1 (LHTIME1) **0x80000F08**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0								LPW							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0					LPC										

FIELD	Description
LPW [23:16]	Line Pulse Width is the number of pixel clock cycles.
LPC [10:0]	Line Pulse Count is the number of pixel clock cycles in each line minus 1 on the screen TFT /NTSC(16bit)/PAL(16bit) : active horizontal pixels - 1 Color STN : (3 * Horizontal display size / pixel width) -1 Mono STN: (Horizontal display size / pixel width)- 1

LCD Horizontal Timing Register2 (LHTIME2) **0x80000F0C**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0							LSWC								
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0							LEWC								

FIELD	Description
LSWC [24:16]	Line Start Wait Cycle is the number of dummy pixel-clock cycles minus 1 to insert from the start of each horizontal line of pixels.
LEWC [8:0]	Line End Wait Cycle is the number of dummy pixel-clock cycles minus 1 to insert before the end of each horizontal line of pixels.

LCD Vertical Timing Register1 (LVTIME1) **0x80000F10**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0										FPW					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0					FLC										

FIELD	Description
FPW [21:16]	TFT/TV : Frame Pulse Width is the pulse width of frame clock (VSYNC). STN: N/A
FLC [10:0]	Frame Line Count is the number of lines in each frame on the screen.

LCD Vertical Timing Register2 (LVTIME2) **0x80000F14**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0							FSWC[8:1]								VD
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0							FEWC								

FIELD	Description
FSWC [8:1] VD	TFT/TV: Frame Start Wait Cycle is the number of lines to insert at the end of each frame. VD is FSWC[0]. STN: FSWC[8:1] is N/A. If VD is set, VSYNC signal starts on negative falling edge of HSYNC.
FEWC [7:0]	TFT/TV: Frame End Wait Cycle is the number of lines to insert at the beginning of each frame. STN: extra dummy lines between the end and beginning of frame

LCD Vertical Timing Register3 (LVTIME3) **0x80000F18**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0										FPW					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0					FLC										

If NI of LCTRL is 0, LVTIME3 and LVTIME4 is for even-field. Otherwise, LVTIME3 and LVTIME4 must be the same with LVTIME1 and LVTIME2.

LCD Vertical Timing Register4 (LVTIME4) **0x80000F1C**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0							FSWC								
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0							FEWC								

LCD Lookup Register for RED (LLUTRD) 0x80000F20

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LLUTRD[31:16]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LLUTRD[15:0]															

This register is used for supporting palletized color STN-LCD. It is divided into 8 nibbles. The passive color mode uses a lookup table register, which allows any 8 red levels to be selected out of the 16 possible red levels. The most significant 3-bit of 8-bit encoded pixel addresses 8 red palette locations. Note that LLUTRD register is only used in STN-LCD mode

LCD Lookup Register for GREEN (LLUTGR) 0x80000F24

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LLUTGR[31:16]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LLUTGR[15:0]															

This register is used for supporting palletized color STN-LCD. It is divided into 8 nibbles. The passive color mode uses a lookup table register, which allows any 8 green levels to be selected out of the 16 possible green levels. The next most significant 3-bit of 8-bit encoded pixel addresses 8 green palette locations. Note that LLUTGR register is only used in STN-LCD mode

LCD Lookup Register for BLUE (LLUTBL) 0x80000F28

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LLUTBL[15:0]															

This register is used for supporting palletized color STN-LCD. It is divided into 4 nibbles. The passive color mode uses a lookup table register, which allows any 4 blue levels to be selected out of the 16 possible blue levels. The least significant 2-bit of 8-bit encoded pixel addresses 4 green palette locations. Note that LLUTBL register is only used in STN-LCD mode.

LCD Dithering Pattern Register (LDP7L) **0x80000F2C**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	DP5_7							0	DP4_7						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	DP3_7							0	DP1_7						

LCD Dithering Pattern Register (LDP7H) **0x80000F30**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0								DP6_7							

LCD Dithering Pattern Register (LDP5) **0x80000F34**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0			DP4_5					0			DP3_5				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0			DP2_5					0			DP1_5				

LCD Dithering Pattern Register (LDP4) **0x80000F38**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0				DP3_4				DP2_4				DP1_4			

LCD Dithering Pattern Register (LDP3) **0x80000F3C**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0									DP2_3			0	DP1_3		

LCD Display Size (LDS) **0x80000F40**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
					VSIZE										
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
					HSIZE										

FIELD	Description
VSIZE [26:16]	Vertical size: number of active lines
HSIZE [10:0]	Horizontal size: number of active pixels in a line.

LCD Status Register (LSTATUS) 0x80000F44

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0												EF	DD	RU	FU

FIELD	Description
EF [3]	Even-Field(Read-Only) 0: odd field or frame 1: even field or frame
DD* [2]	Disable Done(Read/Clear). If LEN is disabled, DD will be 1 after current frame has been displayed.. As MDD of LIM register is cleared, it can be LCD interrupt source
RU*[1]	Register Update(Read/Clear) It indicates that all registers programmed are applied to current frame data. As MRU of LIM register is cleared, it can be LCD interrupt source.
FU*[0]	FIFO underrun(Read/Clear) It indicates that FIFO underrun has been occurred. In this case, LCLK frequency must be lower. As MFU of LIM register is cleared, it can be LCD interrupt source.

For clearing a specified bit, it must be written to 1. If a interrupt is generated, LSTATUS bits, which correspond to the interrupt sources, must be cleared. Otherwise, the uncleared interrupt will be not generated any more.

LCD Interrupt Masking Registers (LIM) 0x80000F48

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0													MDD	MRU	MFU

FIELD	Description
MDD[2]	Mask “Disable Done Interrupt”.
MRU[1]	Mask “Register Update Interrupt”.
MFU[0]	Mask “FIFO underrun(Read/Clear)”.

LCD Image Position(LIP) 0x80000F4C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
					Y[10:0]										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
					X[10:0]										

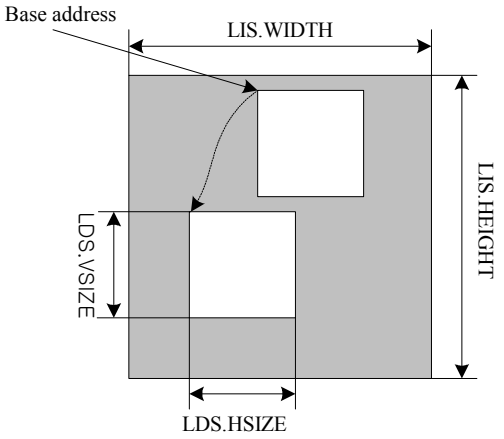
FIELD	Description
Y [10:0]	Y position to display
X [10:0]	X position to display

LCD Image Size(LIS) **0x80000F50**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
				HEIGHT[11:0]											
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
				WIDTH[11:0]											

FIELD	Description
HEIGHT [11:0]	Image height
WIDTH [11:0]	Image width

If image size is larger than display size, the image is clipped automatically. Therefore, as image base address is changed, the panning operation can be implemented.



LCD Image Base Address0(LIBA0) **0x80000F54**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LIBA0[31:16]															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LIBA0[15:2]														0	

FIELD	Description
LIBA0 [31:2]	Image base address. If a image is YUV format, it is Y base address.

LCD Image Base Address1(LIBA1) **0x80000F5C**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LIBA1 [31:16]															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LIBA1 [15:2]														0	

FIELD	Description
LIBA1 [31:2]	If a image is YUV format, it is U base address. Otherwise, it is not used.

LCD Image Base Address2(LIBA2) **0x80000F60**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LIBA2 [31:16]															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LIBA2 [15:2]														0	

FIELD	Description
LIBA2 [31:2]	If a image is YUV data, it is V base address. Otherwise, it is not used.

15 MEMORY CONTROLLER

15.1 Overview

The TCC76x has a memory controller for various kind of memory for digital media en-decoding system. It can manipulate SDRAM, Flash (NAND, NOR type), ROM, SRAM type memories, and also support the IDE interface for HDD or USB2.0 device. It has configurable data bus width through the GPIO pin or each configuration register. The data bus width can be configured for each chip select separately

The memory controller provide the power saving function for SDRAM (self refresh).

The following figure represents the block diagram of memory control unit.

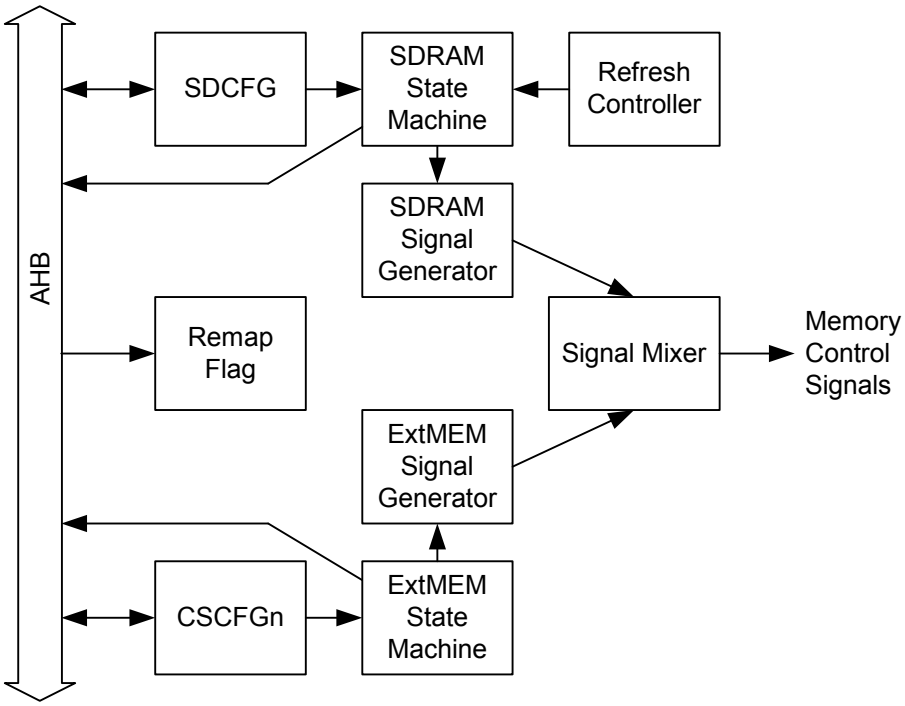


Figure 15.1 Memory Controller Block Diagram

The registers for memory controller block have the base address of 0xF0000000.

Table 15.1 Memory Controller Register Map (Base Address = 0xF0000000)

Name	Address	Type	Reset	Description
SDCFG	0x00	R/W	0x62E97010	SDRAM Configuration Register
SDFSM	0x04	R	-	SDRAM FSM Status Register
MCFG	0x08	R/W	0xZZZZ_02	Miscellaneous Configuration Register
TST	0x0C	W	0x00000000	Test mode register (must be remained zero)
CSCFG0	0x10	R/W	0x0B405649	Configuration Register for External Chip Select 0 (nCS0 pin)
CSCFG1	0x14	R/W	0x0150569A	Configuration Register for External Chip Select 1 (nCS1 pin)
CSCFG2	0x18	R/W	0x006056BA	Configuration Register for External Chip Select 2 (nCS2 pin)
CSCFG3	0x1C	R/W	0x0A70569A	Configuration Register for External Chip Select 3 (nCS3 pin)
CLKCFG	0x20	R/W	0xXXXXXX00	Memory Controller Clock Count Register
SDCMD	0x24	W	-	SDRAM Command Register

Table 15.2 NAND flash Register Map (Base Address = N * 0x10000000)

Name	Address	Type	Reset	Description
NDCMD	0x00	R/W	-	Command Cycle Register
NDLADR	0x04	W	-	Linear Address Cycle Register
NDRADR	0x08	W	-	Row Address Cycle Register
NDIADR	0x0C	W	-	Single Address Cycle Register
NDDATA	0x10	R/W	-	Data Access Cycle Register

*) N represents BASE field of configuration register (CSCFGx) for each chip select.

15.2 SDRAM Controller

The SDRAM controller supports from 16Mbit up to 512Mbit SDRAM.
The SDRAM parameter such as size, refresh period, RAS to CAS delay, refresh to idle delay can be programmed by internal register. Refer to SDRAM cycle diagram in Figure 15.2

SDRAM Configuration Register (SDCFG) **0xF0000000**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CL	BW	CW		SDBASE				RC			RCD			RD[2:1]	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RD[0]	RP			RW		Refresh						AM	APD	PPD	SR

*) The reset value means the following configuration.
CAS Latency = 2 cycles, CAS Width = 9bit, RAS Width = 12bit,
Bus Width = 16bit, SDBASE = 0x20000000
tRC = 7 cycles, tRCD = 2 cycles, tRD = 2 cycles, tRP = 7 cycles, Refresh = (512 + 15) cycles

Except for Bit 0 (SR), the sequence below must be followed whenever this register is written.

1. Clear SDEN bit of MCFG register (SDRAM controller is disabled)
2. Update SDCFG register value
3. Set SDEN bit of MCFG register (SDRAM controller is enabled and MRS cycle is issued to the SDRAM).

Although the reset value of SDEN bit is "0", the boot ROM enables the SDEN bit in JTAG debug mode,. Thus, do not rely on the default value of SDEN bit. Always follow the sequence above if JTAG debugging is required.

CL [31]	CAS Latency (tCL)
0	CAS latency is 2 cycle
1	CAS latency is 3 cycle

*) Do not change this bit when SDEN bit of MCFG register is "1". Disable SDEN first. After this bit is written, SDEN bit must be re-enabled for SDRAM MRS cycle.

BW [30]	Bus Width Select
0	Bus width for SDRAM is 32 bit (valid only in TCC761)
1	Bus width for SDRAM is 16 bit

CW [29:28]	CAS Width
0, 1	8 bit is used for CAS address
2	9 bit is used for CAS address
3	10 bit is used for CAS address

*) 16Mbit : CAS = 8 bit, RAS = 11 bit
64Mbit : CAS = 8 bit, RAS = 12 bit
128Mbit : CAS = 9 bit, RAS = 12 bit
256Mbit : CAS = 9 bit, RAS = 13 bit
512Mbit : CAS =10bit, RAS = 13 bit

SDBASE [27:24]	SDRAM Base Address
N	Indicates the MSB 4bit of SDRAM area. That is SDRAM base = 0x**N**0000000

RC [23:21]	Delay of Refresh to Idle (tRC)
n	n number of HCLK cycle is used to meet the refresh to idle delay time

RCD [20:18]	Delay of RAS to CAS (tRCD)
n	(n+1) number of HCLK cycle is used to meet the RAS to CAS delay time

RD [17:15]	Delay of Read to Precharge (tRD)
n	n number of HCLK cycle is used to meet the read to precharge time

RP [14:12]	Delay of Precharge to Refresh (tRP)
n	(n+1) number of HCLK cycle is used to meet the precharge to refresh time

RW [11:10]	RAS Width
{x,1}	11bit is used for RAS address bus
{0,0}	12bit is used for RAS address bus
{1,0}	13bit is used for RAS address bus

*) 16Mbit : CAS = 8 bit, RAS = 11 bit
64Mbit : CAS = 8 bit, RAS = 12 bit
128Mbit : CAS = 9 bit, RAS = 12 bit
256Mbit : CAS = 9 bit, RAS = 13 bit
512Mbit : CAS =10bit, RAS = 13 bit

Refresh [9:4]	Refresh Cycle
n	Every (n * 512 + 15) number of HCLK cycle has passed, the SDRAM refresh request is generated. If on going cycle has finished, the refresh cycle starts. Real refresh period depends on the period of HCLK.

AM	Address Matching Configuration Bit
0	BA-RAS-CAS
1	RAS-BA-CAS

APD	Reserved
0	Reserved for ChipTest. Must be written as "0"

PPD	Precharge Power-Down Mode
0	Disable precharge power-down mode
1	Enable precharge power-down mode When sdram in precharge-idle state, CKE signal would be zero for power-down. In this case, the redundant 1 cycle is needed to enter the active state.

SR	Self-Refresh Mode
0	Exit from the self-refresh mode
1	Enter the self-refresh mode

SDRAM FSM Status Register (SDFSM) **0xF0000004**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0				SDFSM											

This register is read only and represents current status of finite state machine in the SDRAM controller. This can be used for test purpose only.

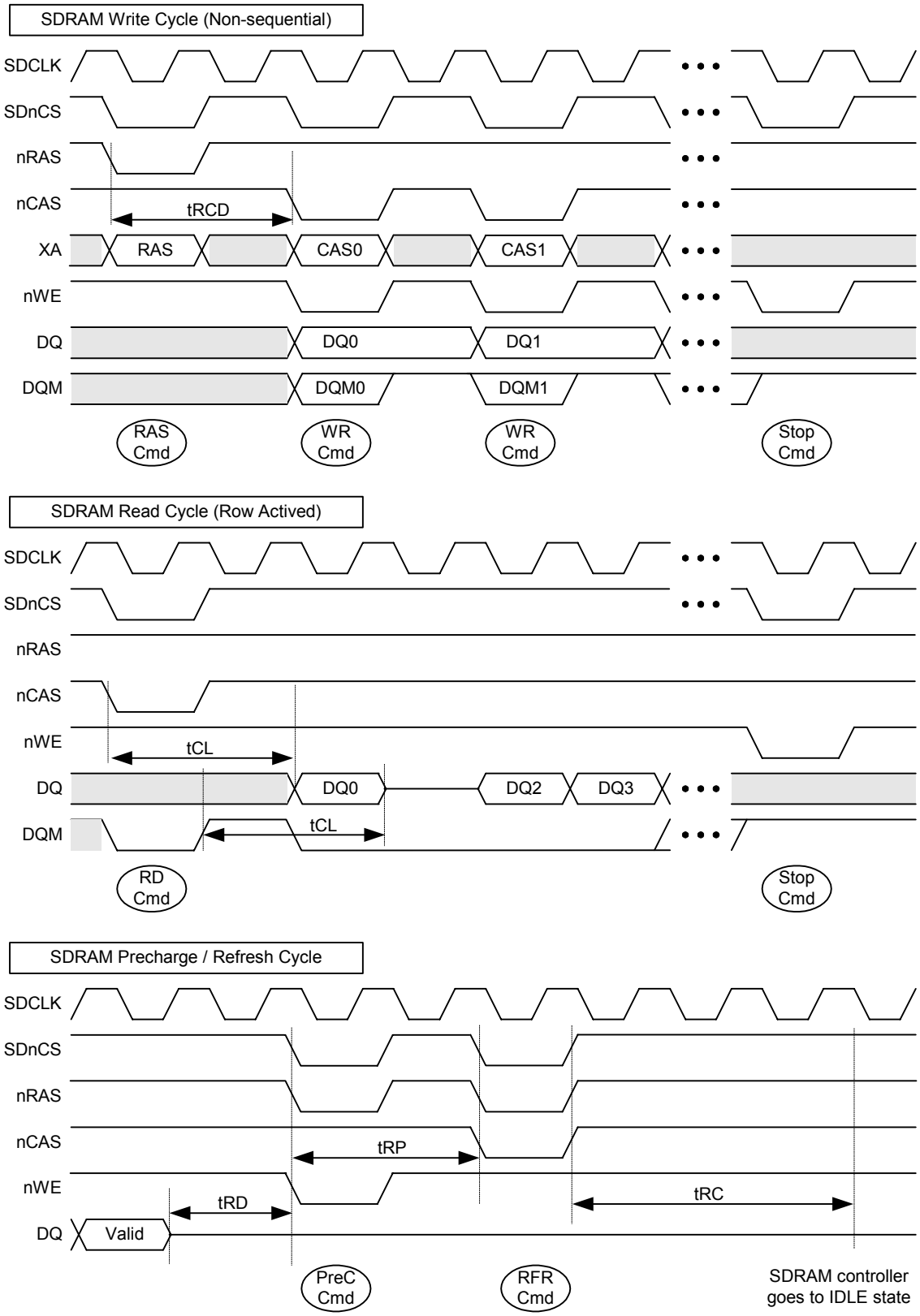


Figure 15.2 SDRAM Cycle Diagram

15.3 Miscellaneous Configuration

In this register, there are various special flags for the TCC76x system.

One of them is for supporting boot PROM. At initialization, the lower address space (0x00000000 ~ 0x0FFFFFFF) is mapped to internal or external boot ROM. But after initialization, these space must be mapped to a RAM as the system program including interrupt vector table is located in this area. To satisfy this requirement, the TCC76x provide RM(Remap) flag.

BM flag is used to select one of the boot procedures. Refer to Section "BOOTING PROCEDURE" for details. BM flag contains the state of GPIO_B[24,22,21] pins at the rising edge of the nRESET pin.

BW flag is used to detect the initial system bus width configuration. This flag is read-only, and contains the state of GPIO_A[9:8] pin at the rising edge of nRESET pin. So user can control the bus width by pulling up or down the GPIO_A[9:8] pin.

Miscellaneous Configuration Register (MCFG) **0xF0000008**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
XXXX															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RDY	XDM	X	BW		BM			SDW	SDT	JTEN	SDEN	SDS	SRF	GPO	RM

RDY [15]	Type	Bus Ready Flag
0	R	Represent that READY pin is low.
1		Represent that READY pin is high.

*) This flag reflects READY pin's state. READY pin is used to extend the access cycle for the external memories. It can control directly the cycle of external memory access by setting the URDY bit of each configuration register and also can be used as a ready flag by polling the state of this bit, especially for NAND flash interfacing.

XDM [14]	Type	Data-Bus Output Mode
0	R/W	In idle state, the data bus would be in input-mode. (Default)
1		In idle state, the data bus would be in output mode.

BW [12:11]	Type	Bus Width Flag
00, 01	R	The corresponding memory is configured by 32bit data bus. The 32bit bus width is valid only in TCC761.
10		The corresponding memory is configured by 16bit data bus.
11		The corresponding memory is configured by 8bit data bus.

BW is the status of GPIO_A[9:8] at the rising edge of nRESET signal. The bus-width of memory attached at nCSx register is determined as follows.

BW (of CSCFGx) = BW (of MCFG) ^ BW (that user want)

BM [10:8]	Type	Boot Mode
n	R	The state of GPIO_B[24,22,21] pins at reset. Refer to Chapter "BOOTING PROCEDURE" for boot mode.

SDW [7]	Type	SDRAM High-Frequency Wait
0	R/W	No additive wait cycle
1		Additive wait cycle

SDT [6]	Type	Type of SDRAM
0	R/W	Single-Data-Rate SDRAM
1		Double-Data-Rate SDRAM

JTEN [5]	Type	JTAG Enable
0	R/W	JTAG port is disabled
1		JTAG port is enabled

SDEN [4]	Type	SDRAM Controller Enable
0	R/W	SDRAM controller is disabled
1		SDRAM controller is enabled

*) When this bit goes from low to high, SDRAM MRS cycle is generated.
This bit must be cleared before CL bit of SDCFG register is changed.

SDS [3]	Type	SD_CLK output select
0	R/W	SDRAM Clock is out from SD_CLK pin
1		GPO bit is out from SD_CLK pin

SRF [2]	Type	Self Refresh Cycle Generation
0	R/W	If SDRAM is in standby mode, the refresh cycle is generated a few times automatically, and SDRAM exits from standby state and goes back into idle state.
1		If SDRAM is not in standby mode, the self-refresh cycle is generated, and the SDRAM enters into standby mode and stay this mode until this flag goes back to low.

*) Do not set while program is executing in SDRAM. SR bit of SDCFG register has the same function.. Either one can be used for self-refresh mode control.

It is recommended to use the following example sequence to control self-refresh mode.

To enable self-refresh mode,

1. Manipulate cache coherency if necessary.
2. Set SR bit of SDCFG register
3. Set SDS bit of MCFG register

To exit from self-refresh mode,

1. Clear SDS bit of MCFG register
2. Clear SR bit of SDCFG register

The above sequences must be executed in the non-SDRAM area, like internal SRAM or NOR flash and while the SDRAM is in self-refresh mode, code should not access the SDRAM area.

GPO [1]	Type	SD_CLK output
0 / 1	R/W	When SDS bit is high, this bit is out through SD_CLK pin

RM [0]	Type	Remap Flag
0	R/W	The area 0 (0x00000000 ~ 0x0FFFFFFF) space is mapped to internal / external boot ROM
1		The area 0 space is released from boot ROM

In initialization, RM flag direct that the lower address space is mapped to internal or external boot ROM. The boot program in internal or external ROM set RM flag high after going to address space that is not in lower address space(0x00000000~0x0FFFFFFF). After RM flag is set to 1, the lower address space is released from internal or external boot ROM, so the lower address space can be mapped to other memories including SDRAM or internal SRAM by changing the base address of that memories. The RM flag can be restored to 0 by user request, but because the lower address space is remapped to boot ROM again, care must be taken not to illegally change the RM flag.

15.4 External Memory Controller

External memory controller can control external memories such as NAND or NOR type flash memory and ROM, SRAM type memory. These memories are selected by nCS3 ~ nCS0 pins. The cycle parameter for accessing external memory can be configured by internal registers. In case of NAND flash, additional parameters for address, command and data cycles can be provided.

External Chip Select n Configuration Register (CSCFGx) 0xF0000010 + (x * 4)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OD	WD	PW[7:6]		BW		MTYPE		CSBASE				URDY	RDY	PW[5:4]	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PW[3]	AMSK	PSIZE		CADR		STP		PW[2:0]				HLD			

*) The reset value of each CSCFGx register means the following configuration for each chip select.
Chip Select 0 : 16bit, SRAM, Base = 0x40000000, tSTP=1, tPW=2, tHLD=1
Chip Select 1 : 32bit, IDE, Base = 0x50000000, not use Ready, tSTP=2, tPW=4, tHLD=2
Chip Select 2 : 32bit, NAND, Base = 0x60000000, AMSK=1, PSIZE=1, CADR=3, tSTP=2, tPW=8, tHLD=2
Chip Select 3 : 16bit, NOR, Base = 0x70000000, tSTP=2, tPW=4, tHLD=2

OD	Delayed 'OE' Signal
0	Normal STP and HLD timing would be applied.
1	When STP and HLD are zero, 1 cycle would be added for delayed by half-pulse for OE signal

WD	Delayed 'WE' Signal
0	Normal STP and HLD timing would be applied.
1	When STP and HLD are zero, 1 cycle would be added for delayed by half-pulse for WE signal

*bw [27:26]	Bus Width Select
0, 1	Bus width = 32 bit (valid only in TCC761)
2	Bus width = 16 bit
3	Bus width = 8 bit

*) bw is calculated by xoring the BW field of MCFG register and BW field of CSCFGx register, that is bw = BW(of MCFG) ^ BW(of CSCFGx). BW(of MCFG) is acquired by the status of GPIO_A[9:8] at the rising edge of nRESET signal. So, if user want to set bus-width independently to the BW of MCFG, you must set the BW of CSCFGx as like as the follows.

BW (of CSCFGx) = BW (of MCFG) ^ BW (that user want)

MTYPE [25:24]	Type of External Memory
0	NAND type
1	IDE type
2	SMEM_0 type (Ex : ROM, NOR flash) Byte write control signal (DQM) is not needed.
3	SMEM_1 type (Ex : SRAM) Byte write control signal (DQM) is needed.

CSBASE [23:20]	Chip Select n Base Address
M	Indicates the MSB 4bit of nCS[n] area. The base address of nCS[n] is set to M * 0x10000000.

URDY [19]	Use Ready
1	Ready / Busy signal monitoring is enabled The memory controller extends access cycle until the state of READY pin indicates that the access request has accomplished.

*) Refer to Figure 15.3 for ready(busy) cycle extension. Don't use this feature when access NAND flash. NAND flash's READY signal is for waiting from end of command cycle to start of data cycle so it is not adequate for extension of each cycle.

RDY [18]	Ready / Busy Select
0	The READY(MODE0) pin indicate the READY signal. The memory controller extends access cycle until this pin goes to high state.
1	The READY(MODE0) pin indicate the BUSY signal. The memory controller extends access cycle until this pin goes to low state.

*) Refer to Figure 15.3 for ready/busy cycle extension.

AMSK [14]	Address Mask Bit
0	Upper half of data bus is masked to zero.

*) In case of 16bit width NAND flash, the upper half byte must be held low, during address cycles. This bit must be set to zero. But if the system uses multiple NAND flashes by sharing a chip select but separating each data to 16 or 32bit data bus of the TCC76x, the AMSK must be set to 1, so the address can be fed to each NAND flashes.

PSIZE [13:12]	Page size of NAND Flash
psize	The size of one page for NAND type flash. It represents byte per page calculated by the following equation. 1 Page = $256 * 2^{psize}$

*) Refer to Table 15.3 about the relationship between the address generation and each page size configuration.

CADR [11:9]	Number of Address Cycles
N	The number of address command cycle for NAND type flash. (N+1) cycle is used for generating address cycle command.

*) Refer to sub-register of NAND type memory for more information of PSIZE and CADR field.

STP [8:6]	Number of Cycle for Setup Time (tSH)
N	N cycle is issued between the falling edge of nCS[n] and nOE / nWE.

PW[7:0] [29:28,17:15,5:3]	Number of Cycle for Pulse Width (tPW)
N (= 0~255)	(N+1) cycle is issued between the falling and rising edge of nOE / nWE.

HLD [2:0]	Number of Cycle for Hold Time (tHLD)
N	N cycle is issued between the rising edge of nOE / nWE and nCS[n].

The following figure displays the element cycle diagram for external memories.

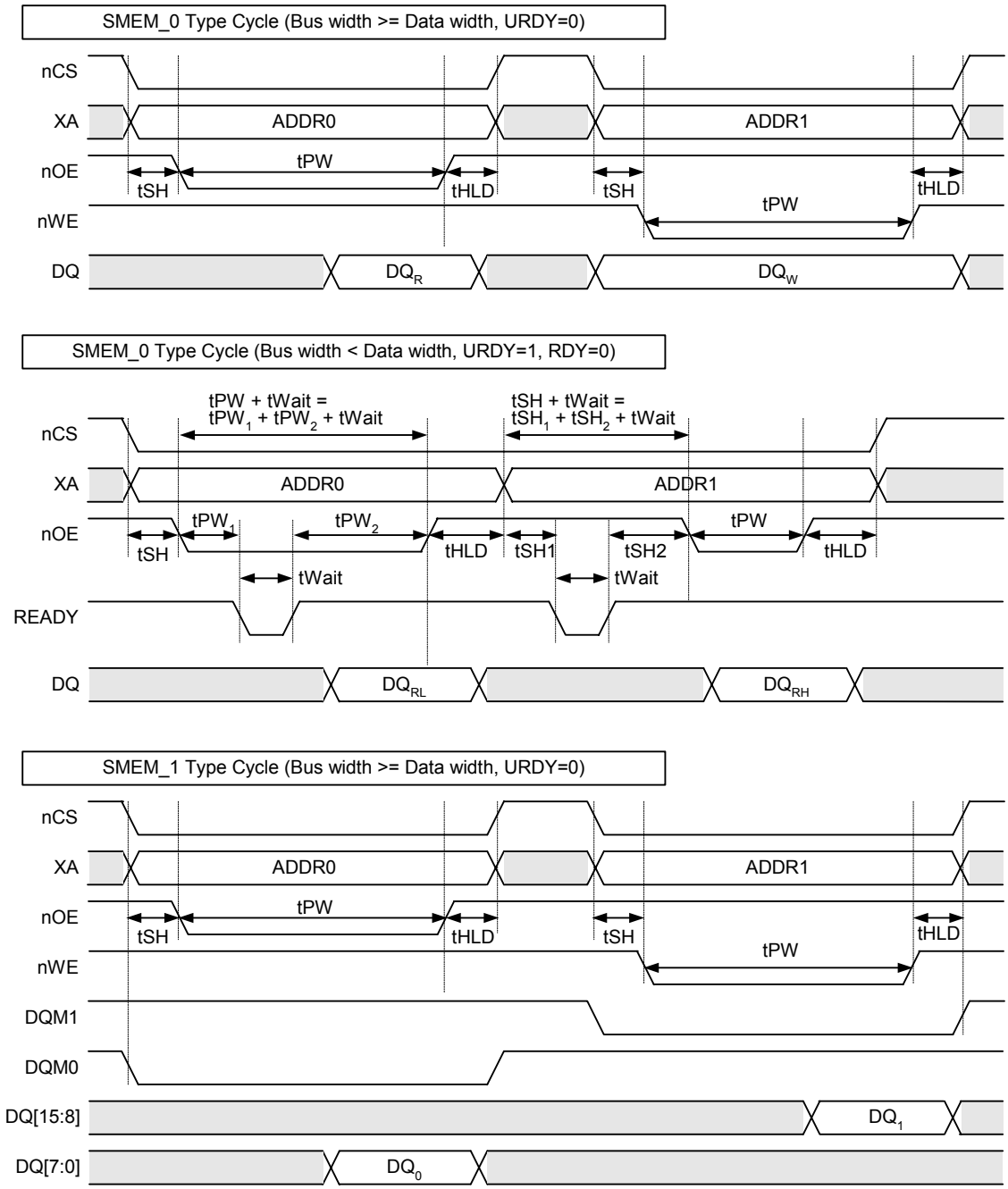


Figure 15.3 Basic Timing Diagram for External Memories

In case of IDE type memories, there are two chip-enable signals for it. In the TCC76x, each enable signal can be controlled by offset address space. ‘nCS0’ reflects that the offset address range of 0 ~ 0x1F is accessed, ‘nCS1’ reflects that 0x20 ~ 0x3F is accessed. For larger address than 0x3F, if bit5 of address value means which enable signal is activated. (0 to ‘nCS0’, 1 to ‘nCS1’)

Memory Controller Clock Count Register (CLKCFG) **0xF0000020**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved													CNT[2:0]		

CNT [2:0]	Count Select for Clock Gating
N	The internal clock of the Memory Controller can be gated to save power. These bits selects the clock gating ratio. The timing parameters of CSCFGx registers should be re-written with appropriate values. These bits also affect the SD_CLK output. Do not enable this feature when DDR SDRAM is used.

SEL[2:0]	SD_CLK and Internal Clock
1	HCLK / 2
2	HCLK / 4
3	HCLK / 6

SDRAM Command Register (SDCMD) **0xF0000024**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															A10
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
nCS	nRAS	nCAS	nWE	BA[1:0]		A[9:0]									

When this register is written, corresponding SDRAM signal is output to the SDRAM. This is a write only register and read data is undefined. Any value written to this register must be a valid SDRAM command (MRS or EMRS, etc).

Sub-registers of NAND type memory

In case of NAND flash type memories, there are several sub-registers for generating command, address, and data cycles.
Followings are these sub-registers. (M is base field of CSCFGx register)
Except the data register (NDDATA), the sub-register has implicit size of 32bit, so the bus-width of CSCFGx register does not affect the cycle of command and address registers. It only affects the cycle of data register.

Command Cycle Register (NDCMD) **0x10000000 * M**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NDCMD3								NDCMD2							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NDCMD1								NDCMD0							

*) If bus width of NAND flash is more than 8bit, the NDCMD1 ~ 3 may be used as command register, otherwise only NDCMD0 is used as command register. The following values are an example commands for NAND flash of SAMSUNG. Refer to corresponding datasheet of NAND flash chip for more detailed list of command s.

0x00/0x01 : Page Read Command
0x80 : Page Program Command
0x60 : Block Erase Command
0x70 : Status Read Command (generated by reading from 0xM0000700 address)

Linear Address Cycle Register (NDLADR) **0x10000000 * M + 0x04**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NDLADR[31:16]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NDLADR[15:0]															

*) By writing to this register, memory controller generates linear address cycle for NAND flash.

Row Address Cycle Register (NDRADR) **0x10000000 * M + 0x08**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NDRADR[31:16]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NDRADR[15:0]															

*) By writing to this register, memory controller generates row address cycle for NAND flash.

Table 15.3 represents the relation between each cycle and address generation.
User must set this information appropriately to PSIZE and CADR field of CSCFGx register ahead of accessing NAND data.

Table 15.3 Page size of NAND Flash

# of Cycle	Address Generation			
	PSIZE = 0	PSIZE = 1	PSIZE = 2	PSIZE = 3
1st	ADR[7:0]	ADR[7:0]	ADR[7:0]	ADR[7:0]
2nd	ADR[15:8]	ADR[16:9]	ADR[10:8]	ADR[11:8]
3rd	ADR[23:16]	ADR[24:17]	ADR[18:11]	ADR[19:12]
4th	ADR[31:24]	ADR[31:25]	ADR[26:19]	ADR[27:20]
5th	-	-	ADR[31:27]	ADR[31:28]

*) ADR means address value that is written to NDLADR or NDRADR register. The shaded cycles represent row address cycles. That is, NAND address cycles start from there when NDRADR register is accessed.

Single Address Cycle Register (NDIADR) **0x10000000 * M + 0x0C**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								NDIADR							

*) When CPU writes to this register, one cycle of address cycle is generated.

Data Register (NDDATA) **0x10000000 * M + 0x10**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NDDATA3								NDDATA2							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NDDATA1								NDDATA0							

*) NDDATA3~1 may be used as the value of data register, otherwise only NDDATA0 is used as data register. It is dependant on the bus-width of CSCFGx register of NAND flash.

15.5 Internal Memory

In the TCC76x, there is 64Kbytes of SRAM for general purposes and 4Kbytes of ROM for system initialization. SRAM area is dedicated to area 3 (0x30000000 ~ 0x3FFFFFFF), and also accessed by area 0 (0x00000000 ~ 0x0FFFFFFF) when there are no devices assigned to area 0. ROM area is dedicated to area E (0xE0000000 ~ 0xEFFFFFFF), and also accessed by area 0 (0x00000000 ~ 0x0FFFFFFF) when RM flag of MCFG register is cleared to 0.

In case of internal ROM, access cycle can be extended by inserting 1 wait cycle. This wait cycle is determined by writing any value to ROM area.

When writing to address of which the bit 2 is 1 (such as 0xE0000004, 0xE000000C, 0xE0000014, …) , the wait cycle is to be inserted from the next ROM access cycle. On the other hand writing to address of which the bit 2 is 0 (such as 0xE0000000, 0xE0000008, 0xE0000010, …), the wait cycle is to be removed from the next ROM access cycle.

In the TCC76x, zero wait access is guaranteed for the internal ROM and SRAM up to 100MHz AHB clock. The wait cycle insertion feature was preserved for the TCC72x. There is no need to enable wait cycle.

16 ECC (Error Correction Code)

16.1 Functional Description

The ECC (Error Correction Code) is used to correct data error in storage device or various kind of communicating system. The TCC76x has a simple ECC generation module that calculate these ECC for this purpose. By enable ECC module, it consistently monitors internal bus activity and calculate ECC whenever there is read or write cycle from/to a predefined memory area. The area can be determined by special register so this module can be used ECC calculation itself not only for specific storage device such as NAND flash.

The following figure represents block diagram including internal bus connection for ECC module.

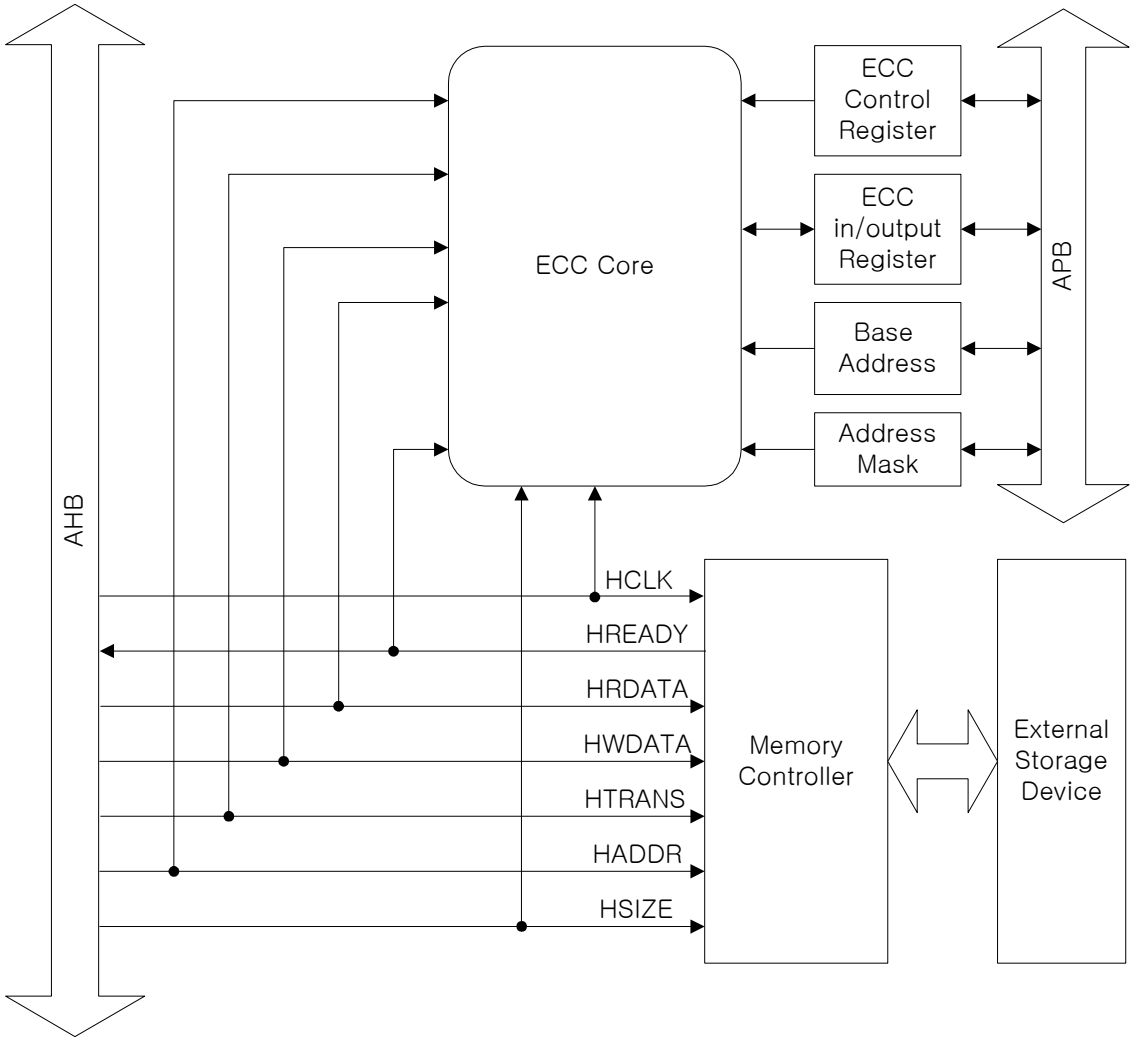


Figure 16.1 ECC Block Diagram

16.2 Register Description

Table 16.1 ECC Register Map (Base Address = 0x80000900)

Name	Address	Type	Reset	Description
ECC_CTRL	0x00	R/W	0x00000000	ECC Control Register
ECC_BASE	0x04	R/W	0x00000000	Base Address for ECC Calculation
ECC_MASK	0x08	R/W	0x00000000	Address mask for ECC area.
ECC_CLR	0x0C	W	-	Clear ECC output register
SLC_ECC0	0x10	R	0x00000000	1st Block ECC output for SLC NAND
SLC_ECC1	0x14	R	0x00000000	2nd Block ECC output for SLC NAND
SLC_ECC2	0x18	R	0x00000000	3rd Block ECC output for SLC NAND
SLC_ECC3	0x1C	R	0x00000000	4th Block ECC output for SLC NAND
SLC_ECC4	0x20	R	0x00000000	5th Block ECC output for SLC NAND
SLC_ECC5	0x24	R	0x00000000	6th Block ECC output for SLC NAND
SLC_ECC6	0x28	R	0x00000000	7th Block ECC output for SLC NAND
SLC_ECC7	0x2C	R	0x00000000	8th Block ECC output for SLC NAND
MLC_ECC0W	0x40	W	-	MLC NAND ECC calculation register 0
MLC_ECC1W	0x44	W	-	MLC NAND ECC calculation register 1
MLC_ECC0R	0x48	R/W	0x00000000	Calculated ECC output 0 for MLC NAND
MLC_ECC1R	0x4C	R/W	0x00000000	Calculated ECC output 1 for MLC NAND

ECC Control Register (ECC_CTRL) **0x80000900**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0											ECC_CNT[8:4]				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ECC_CNT[3:0]				MLC_STAT[3:0]				HLD	0	EC0	ME	SLC_CNT[2:0]			SE

ECC_CNT [20:12]	ECC Word Counter
N	Means that N number of words are calculated

MLC_STAT [11:8]	Represent Internal State for MLC
1000	ST_ECC : Compare state. It compares two ECC for error-checking.
0100	ST_WR : Write state. It calculates ECC for write cycle.
0010	ST_RD : Read state. It calculates ECC for read cycle.
0001	ST_IDLE : Idle state. It waits until there is access for MLC device.

HLD [7]	ECC Hold
1	Hold Enabled. ECC output register is not changed.

EC0 [5]	ECC Zero
1	Means that ECC output register (MLC_ECC0R & MLC_ECC1R for MLC, SLC_ECC0 & SLC_ECC1 for SLC) contains 0.

ME [4]	MLC ECC Enable
1	Enable ECC for MLC
0	Disable ECC of MLC

SLC_CNT [3:1]	ECC Block Count
N (0 ~ 7)	Means that N number of ECC block (256 bytes) are calculated. This is useful to determine how many ECC output registers are valid. That is, N number of ECC output register counting from SLC_ECC0 are valid.

SE [0]	SLC ECC Enable
1	Enable ECC for SLC
0	Disable ECC of SLC

ECC Base Address Register (ECC_BASE) **0x80000904**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ECC_BASE[31:16]															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ECC_BASE[15:0]															

ECC Address Mask Register (ECC_MASK) **0x80000908**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0				ECC_MASK[9:0]										0	

The ECC is calculated whenever the specified region of memory is accessed. The region for ECC calculating is determined by ECC_BASE & ECC_MASK register. The real base address is determined by following formula.

Real base address = ECC_BASE(0x80000904) & ~(ECC_MASK[9:0] << 2)
(The real base address is assumed to be word aligned, so the least 2 bits are always 0.)

The size of region is also determined by ECC_MASK register. If ECC_MASK register have N concatenated 0 from LSB, the region size is set to 2^N bytes.

ECC Clear Register (ECC_CLR) **0x8000090C**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Don't care															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Don't care															

Whenever this register is written by any value, all ECC output registers are cleared to 0.

ECC Output Register for SLC (SLC_ECCx) **0x80000910 + x*4**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0								SLC_ECCx_0							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SLC_ECCx_1								SLC_ECCx_2							

These registers contain ECC output for SLC. It calculates ECC of SSFDC standard, and can contain up to 8 block of data. Every time it finishes calculating ECC for each block, it shifts the ECC values for previous block from SLC_ECC0 upward to SLC_ECC7 register. So the ECC for last block is always stored at SLC_ECC0 register.

For each output register, there are a total of 22 bits of parity data (6 bits for column parity

and 16 bits for line parity) as follows:
P1, P1', P2, P2', P4, P4', P8, P8', P16, P16', ……, P1024, P1024'

The parity data that have been generated are stored as follows.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SLC_ECCx_0	P64	P64'	P32	P32'	P16	P16'	P8	P8'
SLC_ECCx_1	P1024	P1024'	P512	P512'	P256	P256'	P128	P128'
SLC_ECCx_2	P4	P4'	P2	P2'	P1	P1'	1	1

ECC Evaluation Register for MLC (MLC_ECC0W) **0x80000940**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MLC_ECC0W[31:16]															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MLC_ECC0W[15:0]															

ECC Evaluation Register for MLC (MLC_ECC1W) **0x80000944**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	MLC_ECC1W[30:16]														
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MLC_ECC1W[15:0]															

To evaluate ECC for MLC, write acquired ECC to these registers. The MLC_ECC0W is LSB word and MLC_ECC1W is MSB. The order of writing should be LSB first and then MSB. After writing to MLC_ECC1W, ECC module starts evaluation and its state can be monitored by checking MLC_STAT field of ECC_CTRL register.

After finishing evaluation, user can determine whether ECC error occurred or not by checking EC0 flag of ECC_CTRL register or checking MLC_ECC0R & MLC_ECC1R registers.

ECC Output Register for MLC (MLC_ECC0R) **0x80000948**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MLC_ECC0R[31:16]															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MLC_ECC0R[15:0]															

ECC Output Register for MLC (MLC_ECC1R) **0x8000094C**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	MLC_ECC1R[30:16]														
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MLC_ECC1R[15:0]															

If there are ECC error, the EC0 flag of ECC_CTRL register is set to 1. By reading MLC_ERR1R & MLC_ERR0R register and using appropriate algorithm, user can fix maximum 3 symbols of error.

17 I2C CONTROLLER

17.1 Functional Description

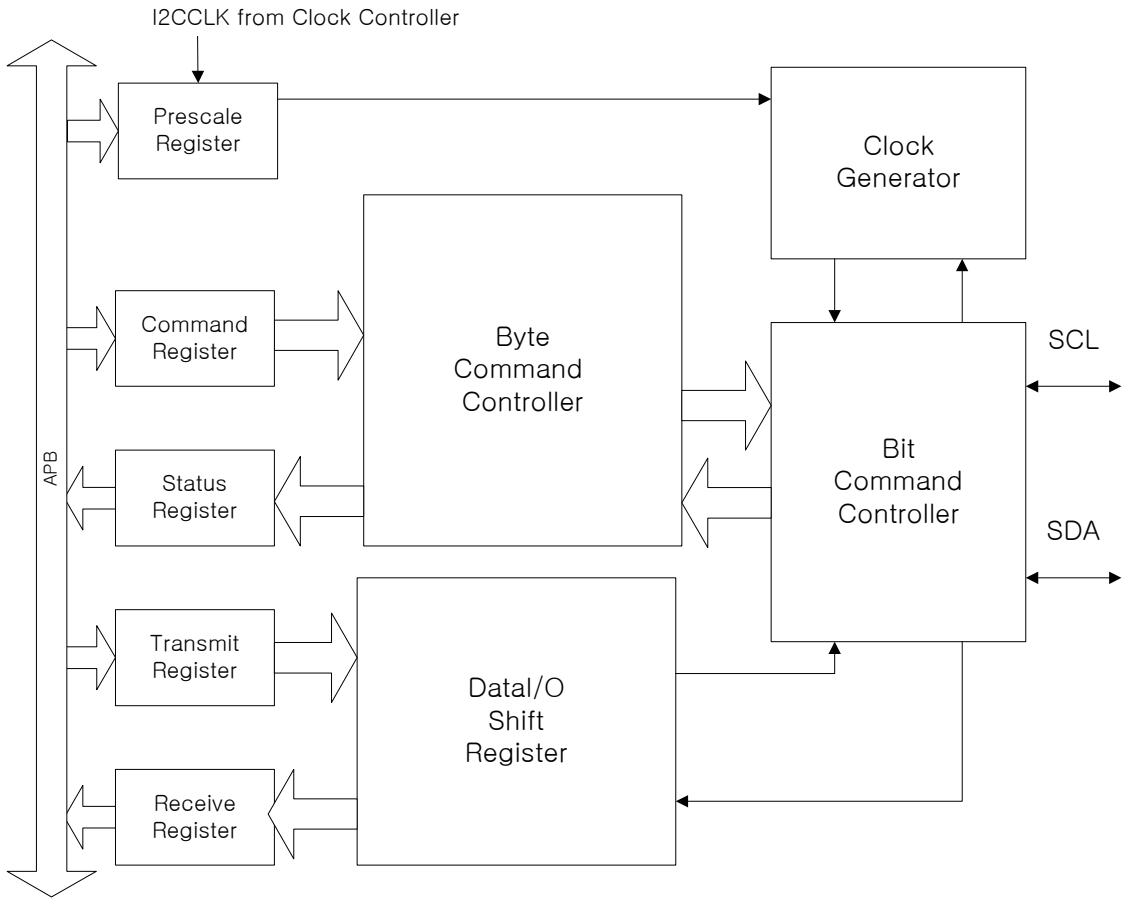


Figure 17.1 I2C Block Diagram

17.2 Related Blocks

Before enable the I2C Controller, CFGI2C[1:0] of MISCFG register (0x80000A1C) must be set according to the external connection. CFGI2C[1:0] enables I2C signals on to the GPIO pins as listed in the table below. CFGI2C has a priority over GPIO control bits. Note that GPIO_D[17:16] is also shared with CIF (Camera Interface) signals. When CIFEN is set, GPIO_D[17:16] will be assigned to CIF signals regardless of CFGI2C value.

Table 17.1 I2C Signal Mapping

CIFEN	CFGI2C[1:0]	SCL	SDA
X	00	Disabled	Disabled
X	01	GPIO_A[9]	GPIO_A[8]
X	10	GPIO_A[11]	GPIO_A[10]
0	11	GPIO_D[17]	GPIO_D[16]
1	11	Disabled	Disabled

At power on reset, CFGI2C is disabled and the I2C signals are treated as normal GPIO. GPIO_A[9:8] are used as Bus Width Configuration bits (BW[1:0]) at power on reset. Due to this functionality, I2C signals may not be selected. Refer to section “MEMORY CONTROLLER” for BW[1:0] description. (MCFG register)

After the signals are enabled, I2CCLK (the main clock of I2C) must be enabled and configured to the proper frequency. Refer to section "CLOCK GENERATOR" for I2CCLK (EX2CLK) related descriptions.

For internal synchronization, the APB clock frequency must be faster than the I2CCLK frequency.

$$f_{I2CLK} \leq f_{HCLK} / 4.0$$

17.3 Register Description

Table 17.2 I2C Register Map (Base Address = 0x80000800)

Name	Address	Type	Reset	Description
PRES	0x00	R/W	0xFFFF	Clock Prescale register
CTRL	0x04	R/W	0x0000	Control Register
TXR	0x08	W	0x0000	Transmit Register
CMD	0x0C	W	0x0000	Command Register
RXR	0x10	R	0x0000	Receive Register
SR	0x14	R	0x0000	Status Register

Prescale Register (PRES) **0x80000800**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Clock Prescale data															

This register is used to prescale the SCL clock line. Due to the structure of the I2C interface, the core uses a 5*SCL clock internally. The prescale register must be programmed to this 5*SCL frequency (minus 1). Change the value of the prescale register only when 'EN' bit is cleared.

Example :

CLK Input frequency = 8MHz , Desired SCL frequency = 100KHz

Prescale = (8MHz / (5*100KHz)) – 1 = 15

Control Register (CTR) **0x80000804**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0								EN	IEN	MOD	RESERVED				

EN [7]	I2C Core enable bit
0	Disabled
1	Enabled

IEN [6]	I2C Core interrupt enable bit
0	Disabled
1	Enabled

MOD [5]	I2C Data Width
0	8bit Mode
1	16bit Mode

Transmit Register (TXR) **0x80000808**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Transmit Data															

When CTRL[5] is set, in case of 16Bit Mode is selected, Transmit Data bit width become 16 bit. Default mode is 8bit mode.

Command Register (CMD) **0x8000080C**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0								STA	STO	RD	WR	ACK	RESERVE		IACK

STA [7]	Start Condition Generation
0	Disabled
1	Enabled

STO [6]	Stop Condition Generation.
0	Disabled
1	Enabled

RD [5]	Read From Slave
0	Disabled
1	Enabled

WR [4]	Write to Slave
0	Disabled
1	Enabled

ACK [3]	Sent ACK
0	Enabled
1	Disabled

IACK [0]	Interrupt Acknowledge
0	-
1	Clear a pending interrupt

Receive Register (RXR) **0x80000810**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Receive Data															

When CTRL[5] is set, in case of 16Bit Mode is selected, Receive Data bit width become 16 bit. Default mode is 8bit mode.

Status Register (SR) **0x80000814**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0								RxACK	BUSY	AL				TIP	IF

RxACK [7]	Received acknowledge from slave
0	No Acknowledge received
1	Acknowledge received

BUSY [6]	I2C Bus Busy
0	'0' after STOP signal detected
1	'1' after START signal detected

AL[5]	Arbitration lost
0	The core don't lost arbitration
1	The core lost arbitration

Arbitration is lost when :

a STOP signal is detected, but non requested
the master drives SDA high, but SDA is low

TIP [1]	Transfer in progress
0	Transferring Data
1	Transfer Complete

IF [0]	Interrupt Flag
0	-
1	Interrupt is pending

18 CAMERA INTERFACE

18.1 Overview

The TCC76x provides Camera Interface (CIF). The features of CIF are

- Various formats timings are supported.
- CCIR 601/656 4:4:4, 4:2:2, 4:2:0 YCbCr(YUV/RGB)
- Bayer RGB, 555RGB, 565RGB (16/8 bits bus)
- Data Packing from each channel data
- DMA transfer with programmable burst count (1, 2, 4, 8 bursts)
- 32 depths, 32 bits FIFO

The following parameters can be programmed.

- The input format of image
- The horizontal and vertical size of image
- The packing method of the each channel data

The following figure shows the block diagram of Camera Interface.

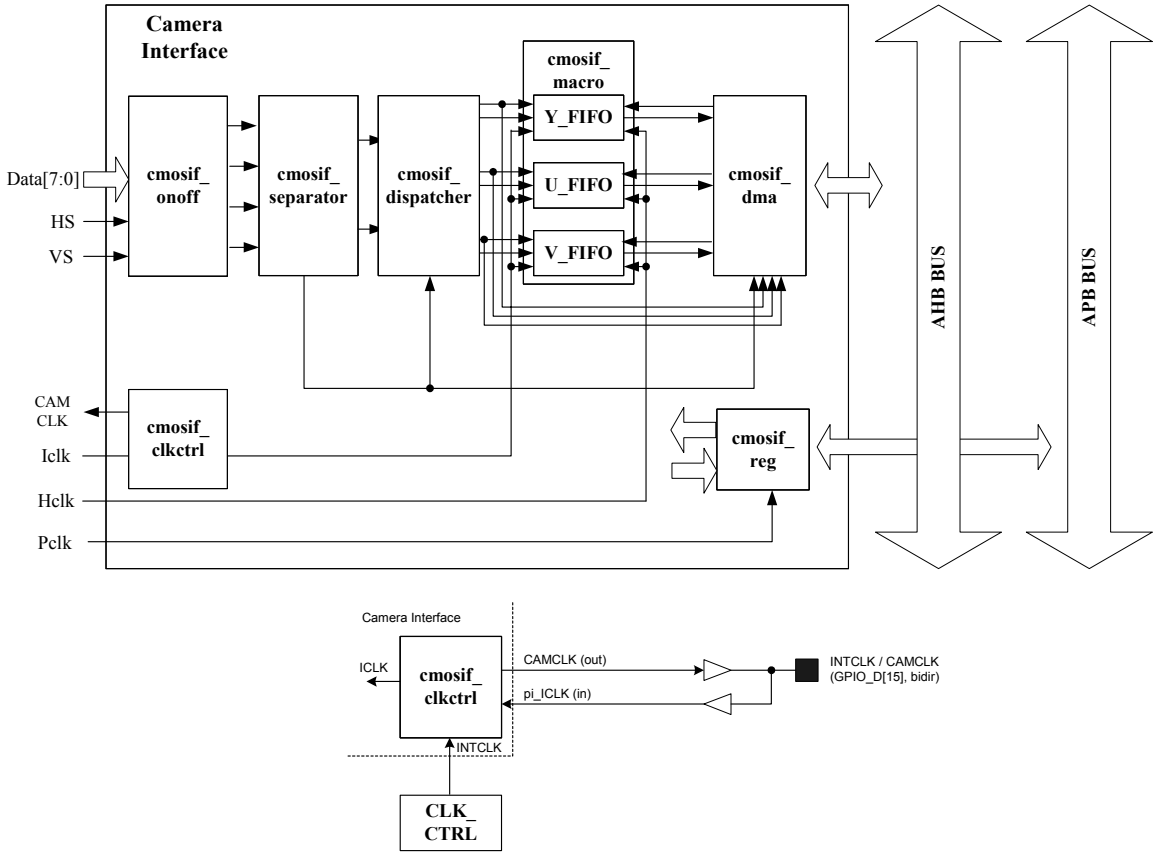


Figure 18.1 CIF Block Diagram

The input data can be optionally separated into three color components. Each channel composes of 8 bits and can be packed up to 32 bits. The packing sequence starts from LSB and the results are stored to the FIFOs. The data stored in the FIFOs are transferred to memory by its own DMA master controller. 1, 2, 4 and 8 burst transfer are supported by DMA master.

Figure 18.2 shows the packing method.

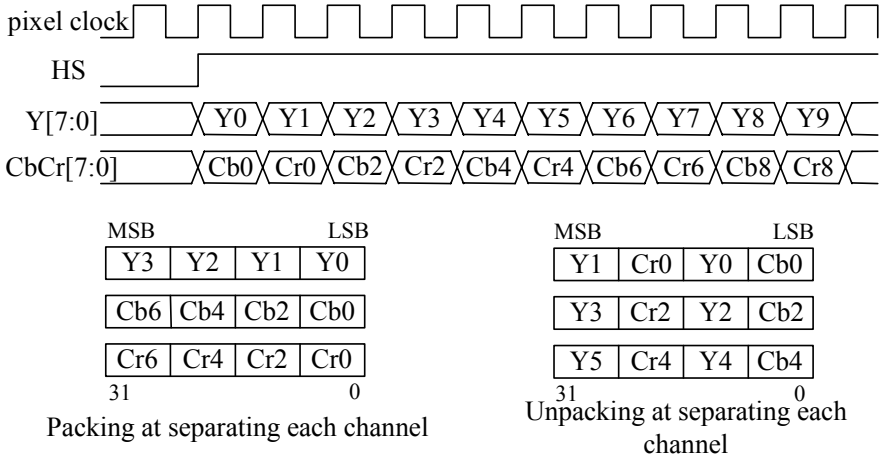


Figure 18.2 Packing Method

The CIF asserts interrupt signal after each frame image has been stored to memory.

18.2 Related Blocks

To enable CIF (Camera Interface), CIFEN bit of MISCFG register (0x80000A1C) must be set to "1". CIFEN bit enables Camera Interface signals on to the GPIO pins listed in the table below. CIFEN has a precedence over GPIO control bits.

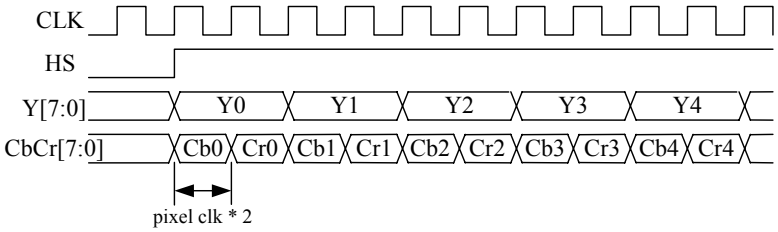
Table 18.1 CIF Signal Mapping

Camera Interface Signals	GPIO Pins
HS	GPIO_D[17]
VS	GPIO_D[16]
CAMCLK	GPIO_D[15]
Data[7:4]	GPIO_D[21:18]
Data[3:0]	GPIO_A[3:0]

At power on reset, CIFEN is disabled and the CIF signals are treated as normal GPIO.

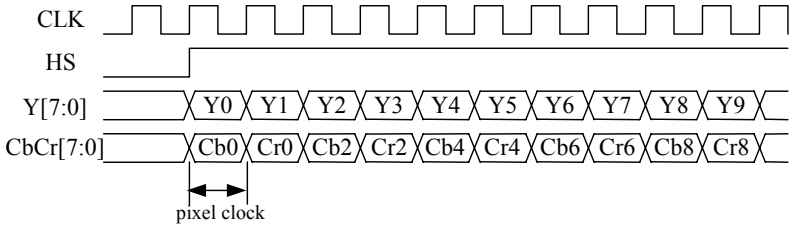
After the signals are enabled, CIFCLK (the main clock of CIF) must be enabled and configured to the proper frequency. Refer to section "CLOCK GENERATOR" for CIFCLK related descriptions.

4:4:4 format



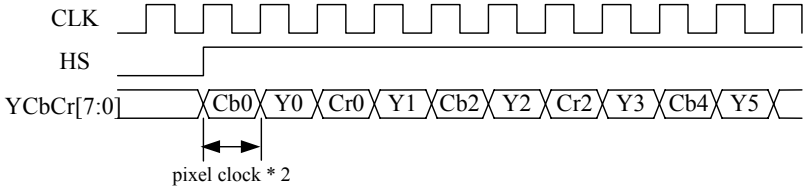
* YCbCr, YUV, RGB [Y(G), Cb(U,R), Cr(V,B)]

4:2:2 16bits format (CCIR-601)



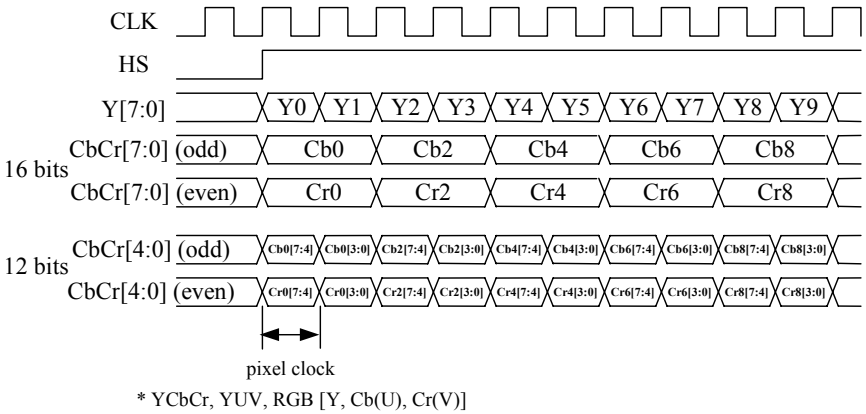
* YCbCr, YUV, RGB [Y(G), Cb(U,R), Cr(V,B)]

4:2:2 8bits format (CCIR-656)



* YCbCr, YUV, RGB [Y(G), Cb(U,R), Cr(V,B)]

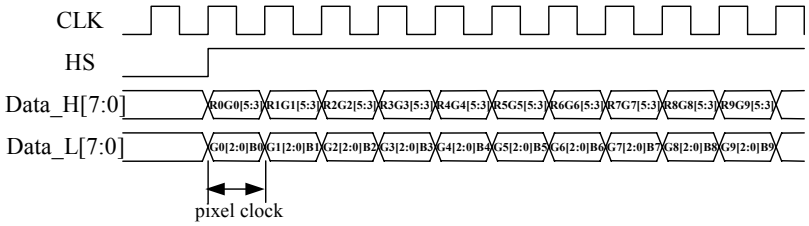
4:2:0 16, 12bits format



* YCbCr, YUV, RGB [Y, Cb(U), Cr(V)]

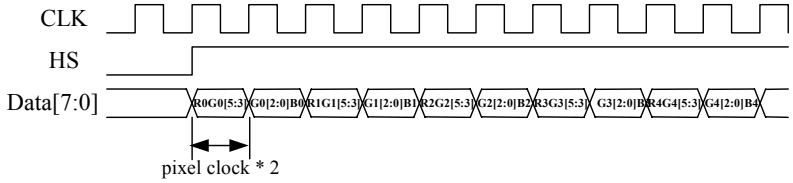
Figure 18.3 YCbCr/RGB 4:4:4/4:2:2/4:2:0 Timing Diagram

565RGB 16bits format



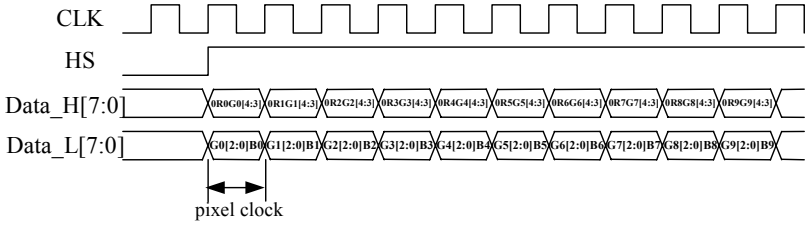
* R and B channels are composed 5 bits and G channel is 6 bits.

565RGB 8bits format



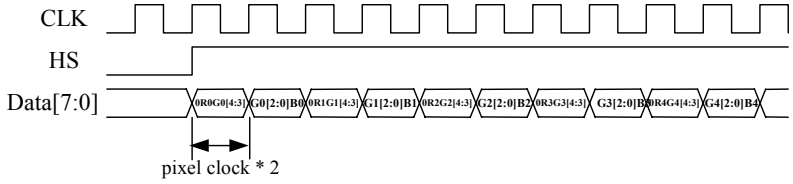
* R and B channels are composed 5 bits and G channel is 6 bits.

555RGB 16bits format



* RGB channels are composed 5 bits and 1 bit is garbage. The garbage locates MSB or LSB 1bit. In figure, the garbage located MSB

555RGB 8bits format



* RGB channels are composed 5 bits and 1 bit is garbage. The garbage locates MSB or LSB 1bit. In figure, the garbage located MSB

Bayer RGB format

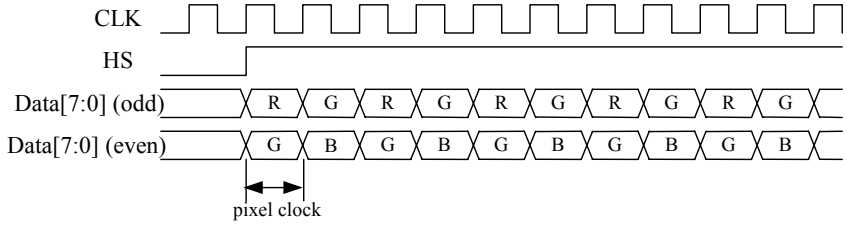


Figure 18.4 RGB 565/555/bayer Timing Diagram

18.3 Register Description

Table 18.2 CIF Register Map (Base Address = 0x80000B00)

Name	Address	Type	Reset	Description
CPCR	0x00	W	0x00000402	Color/Pattern Configuration Register
656FCR1	0x04	W	0x06FF0000	CCIR656 Configuration Register 1
656FCR2	0x08	W	0x0000010B	CCIR656 Configuration Register 2
IICR1	0x0C	W	0x028001E0	Input Image Configuration Register 1
IICR2	0x10	W	0x00000000	Input Image Configuration Register 2
CDCR1	0x14	W	0x00000003	CIF DMA Configuration Register
CDCR2	0x18	W	0x20000000	Memory Address for Y Channel
CDCR3	0x1C	W	0x28000000	Memory Address for Cb(U) Channel
CDCR4	0x20	W	0x2C000000	Memory Address for Cr(V) Channel
FIFOSTATE	0x24	R	0x00000000	FIFO Status Register
CIRQ	0x28	W/R	0x00000000	Interrupt & CIF Operating Register
ICCTRL	0x2C	W	0x00000000	Image Clock Control

Color/Pattern Configuration Register (CPCR) **0x80000B00**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BP	BBS	CP<1:0>		PF<1:0>		RGBM<1:0>		RGBBM<1:0>		CS<1:0>		0	BO	HSP	VSP

BP [15]	Bypass
0	Separated each channel data and stored into memory (default)
1	Don't separate each channel data and stored into memory

BBS [14]	Bypass Bus Select
0	Packing the data from MSB 8bits first in bypass 16bit mode (default)
1	Packing the data from LSB 8bits first in bypass 16bit mode

CP [13:12]	Color Pattern
00	YCbCr color pattern (default)
01	YUV color pattern
10	RGB color pattern

PF [11:10]	Pattern Format
00	4:4:4 format
01	4:2:2 format (default)
10	4:2:0 format or RGB mode

RGBM [9:8]	RGB Mode
00	Bayer RGB mode (default)
01	RGB555 mode
10	RGB565 mode

This mode is operated in RGB mode.

RGBBM [7:6]	RGB Bit Mode
00	16bit mode (4:2:0/4:2:2/4:4:4 YCbCr/YUV/GRB. RGB555/565 format) (default)
01	12bit mode (4:2:0 YCbCr/YUV), 8 bit disable sync (Non sync-port, CCIR656)
10	8 bit mode (Bayer/555/565RGB), 8 bit enable sync (sync-port, 4:2:2 format)

CS [5:4]	Color Sequence				
	555RGB	565RGB	4:4:4/4:2:2:/4:2:0	Bayer RGB	CCIR656
00	RGB(MG)	RGB	R/Cb/U first	BG->GR	YCbYCr
01	RGB(LG)	RGB	R/Cb/U first	GR->BG	YCrYCb
10	BGR(MG)	BGR	B/Cr/V first	RG->GB	CbYCrY
11	BGR(LG)	BGR	B/Cr/V first	GB->RG	CrYCbY

- MG/LG of 555RGB item means MSB/LSB 1bit garbage.
- The sequence of Bayer RGB means that odd line is BGBGBG… and even line is GRGRGR…. at 00.
- Default value is 00.

BO [2]	Bus Order
0	Don't switch the MSB/LSB order (default)
1	Switch the MSB/LSB order.

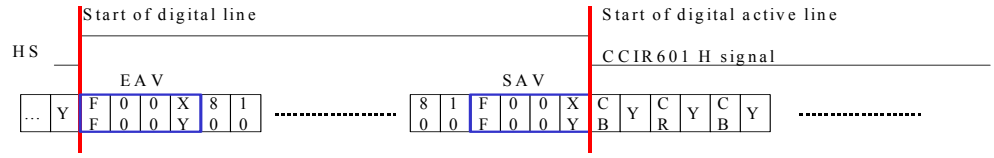
HSP [1]	Horizontal Sync Polarity
0	Active low
1	Active high (default)

VSP [0]	Vertical Sync Polarity
0	Active low (default)
1	Active high

CCIR656 Format Configuration Register 1 (656FCR1) **0x80000B04**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved					PSL<1:0>		0	FPV<7:0>							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SPV<7:0>								TPV<7:0>							

This register and next register (656FCR1 and 656FCR2) define the configuration of CCIR656. Figure 18.5 shows the control signals of this format.



	8-bit data							
	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0
preamble	1	1	1	1	1	1	1	1
	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0
status	1	F	V	H	P3	P2	P1	P0

- Status word define
  - F='0' for field 1, '1' for field 2 (interlace mode. If progressive, this value is '0')
  - V='1' during vertical blanking
  - H='0' at SAV, '1' at EAV
- Protection bits
  - P3=V xor H
  - P2=F xor H
  - P1=F xor V
  - P0=F xor V xor H

Figure 18.5 CCIR-656 Format Diagram

PSL [26:25]	Preamble and Status Location
00	The status word is located the first byte of EAV & SAV
01	The status word is located the second byte of EAV & SAV
10	The status word is located the third byte of EAV & SAV
11	The status word is located the forth byte of EAV & SAV

- If RGB bit mode is 8 bit disable mode, we must find the location of preamble and status for getting sync information. The total size of preamble and status is composed 4 bytes that preamble is 3 bytes and status is 1 byte. This register used to find the location of status word.

FIELD	Description
FPV [23:16]	First preamble value. Default value is 0xFF.
SPV [15:8]	Second preamble value. Default value is 0x00.
TPV [7:0]	Third preamble value. Default value is 0x00.

CCIR656 Format Configuration Register 2 (656FCR2) **0x80000B08**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							HB<3:0>				0	VB<3:0>			

FIELD	Description
HB [8:5]	Horizontal blank In status word, location of 'H' and H value at blanking. The MSB 3 bit means the location of 'H', the other bit means value at blanking. Default value is 0x09.
VB [3:0]	Vertical blank In status word, location of 'V' and V value at blanking. The MSB 3 bit means the location of 'V', the other bit means value at blanking. Default value is 0x0B

Input Image Control Register 1 (IICR1) **0x80000B0C**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSIZE <15:0> Horizontal size of input image. Default value is 0x0280. (decimal 640)															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VSIZE <15:0> Vertical size of input image. Default value is 0x01E0 (decimal 480)															

Input Image Control Register 2 (IICR2) **0x80000B10**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	HO <6:0>							0	VO <6:0>						

FIELD	Description
HO [14:8]	Horizontal offset of input image in horizontal sync. Default value is 0x00.
VO [6:0]	Vertical offset of input image in horizontal sync. Default value is 0x00.

CMOSIF DMA Configuration Register 1 (CDCR1) **0x80000B14**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved													Lock	BS <1:0>	

BS [1:0]	Preamble and Status Location
00	The DMA transfers the image data as 1 word to memory.
01	The DMA transfers the image data as 2 words to memory.
10	The DMA transfers the image data as 4 words to memory.
11	The DMA transfers the image data as 8 words to memory. (default)

- Using the burst of AMBA system.

LOCK [2]	Lock Transfer
0	Non-Lock (default)
1	Lock Transfer

CMOSIF DMA Configuration Register 2 (CDCR2) **0x80000B18**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Y-ADDR[31:16]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Y-ADDR[15:0]															

- In bypass mode, all data is stored to the base address defined by CDCR2 register. The other base address registers are ignored.

CMOSIF DMA Configuration Register 3 (CDCR3) **0x80000B1C**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Cb-ADDR[31:16]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Cb-ADDR[15:0]															

CMOSIF DMA Configuration Register 4 (CDCR4) **0x80000B20**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Cr-ADDR[31:16]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Cr-ADDR[15:0]															

FIELD	Description
Y-ADDR [31:0]	Memory Base Address for Y(G) channel (Default = 0x20000000)
Cb-ADDR [31:0]	Memory Base Address for Cb(U/R) channel (Default = 0x28000000)
Cr-ADDR [31:0]	Memory Base Address for Cr(V/B) channel (Default = 0x2C000000)

FIFO States (FIFOSTATE) **0x80000B24**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
							RE	WE	0	EY	EC1	EC2	FY	FC1	FC2

- There are three FIFOs; Y(G) channel, Cb(U/R) channel, Cr(V/B) channel FIFO.

RE [8]	Read Error
0	The empty signal is Low, or empty is High and read enable signal is Low.
1	The empty signal and read enable signal are High.

WE [7]	Read Error
0	The full signal of FIFO is Low, or full is High and write enable signal is Low.
1	The full signal of FIFO and write enable signal are High.

EY [5]	Empty Signal from Y(G) Channel FIFO
0	The state of Y(G) channel FIFO is non-empty.
1	The state of Y(G) channel FIFO is empty.

EC1 [4]	Empty Signal from Cb(U/R) Channel FIFO
0	The state of Cb(U/R) channel FIFO is non-empty.
1	The state of Cb(U/R) channel FIFO is empty.

EC2 [3]	Empty Signal from Cr(V/B) Channel FIFO
0	The state of Cr(V/B) channel FIFO is non-empty.
1	The state of Cr(V/B) channel FIFO is empty.

FY [2]	Full Signal from Y(G) Channel FIFO
0	The state of Y(G) channel FIFO is non-full.
1	The state of Y(G) channel FIFO is full.

FC1 [1]	Full Signal from Cb(U/R) Channel FIFO
0	The state of Cb(U/R) channel FIFO is non-full.
1	The state of Cb(U/R) channel FIFO is full.

FC2 [0]	Full Signal from Cr(V/B) Channel FIFO
0	The state of Cr(V/B) channel FIFO is non-full.
1	The state of Cr(V/B) channel FIFO is full.

CMOSIF Interrupt Register (CIRQ) 0x80000B28

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							PWDN	0	Pattern	0	RIQ	0	SII	0	ON

PWDN [8]	Camera Power Down
0	Power down
1	Power on

Pattern [6]	Pattern
0	Pattern off.
1	Pattern on.

RIQ [4]	Respond IRQ
0	Don't acknowledge the Stored Image IRQ.
1	Acknowledged the Stored Image IRQ.

SII [2]	Stored Image IRQ
0	Don't store the one frame image.
1	Stored the one frame image.

ON [0]	On/Off
0	Can't operate CIF.
1	Operating CIF (default)

Image Clock Control (ICCTRL) 0x80000B2C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												DIV		CPH	CLK

DIV [3:2]	Divided Clock
n	Clock is divided by (n+1).

CPH [1]	Image Clock Phase
0	0 degree
1	Shift 180 degree

CLK [0]	Usage Image Clock
0	External clock
1	Internal clock

19 FAST GPIO

19.1 Description

In the TCC76x, there is special I/O facilities that enable high speed access for I/O port. These ports are shared with normal GPIO pins and can be accessed through some special instructions of dedicated coprocessor for these I/O. The dedicated coprocessor number is 5, so user can access these ports by using coprocessor instruction of ARM.
Because there is no control signal to select between the two method (fast GPIO mode and normal GPIO mode), it is mandatory to clear one set of registers for these two method. For example, to use Fast GPIO, user must clear corresponding normal GPIO data and direction control register to zero, and vice versa.
Besides of fast I/O port accessing, the dedicated coprocessor has additional functions for various purposes. It has bit-reversing functions on the 32bit or 12bit data. And it can calculate the number of leading zero of 32bit data.

The following table shows coprocessor register for the above functions.

Table 19.1 Register of Fast GPIO

Name	Opcode1	Description
C0	0	It is for I/O direction and I/O data control. Bit allocation of C0 register is as follows. C0[14:0] : FGPDATA(Fast GPIO Data Register) [14:0] FGPDATA[7:0] are shared with GPIO_A[7:0] FGPDATA[14:8] are shared with GPIO_A[14:8] / GPIO_D[21:15] C0[15] : Not used C0[30:16] : FGPCON(Fast GPIO Control Register) [14:0] C0[31] : Selection control for FGPDATA[14:8] path. 0 : FGPDATA[14:8] are shared with GPIO_D[21:15] 1 : FGPDATA[14:8] are shared with GPIO_A[14:8]
	1	It is for toggling C0 register bit-by-bit method.
C1	0	It is for accessing C1 register.
	1	It is for getting 32bit reverse information of C1 register.
	2	It is for getting 12bit reverse information of C1 register.
	3	It is for getting the number of leading zero of C1 register.

To access the above registers, user must use the following instructions.

Table 19.2 Instruction of CP5

Instruction	Description
MCR p5, 0, Rd, Cn, Cn, 0	To write Cn register as Rd value.
MRC p5, 0, Rd, Cn, Cn, 0	To read Cn register on Rd register.
MCR p5, 1, Rd, C0, C0, 0	To invert Fast GPIO, set certain bit field on Rd using this code.
MRC p5, 1, Rd, C1, C0, 0	To get the 32bit-reverse of C1 register on Rd register.
MRC p5, 2, Rd, C1, C0, 0	To get the 12bit-reverse of C1 register on Rd register.
MRC p5, 3, Rd, C1, C0, 0	To get the number of leading zero in C1 register on Rd register.

Note: Fast GPIO register access is guaranteed up to 90MHz of FCLK frequency. Do not access Fast GPIO reigisters when FCLK frequency exceeds the limit.

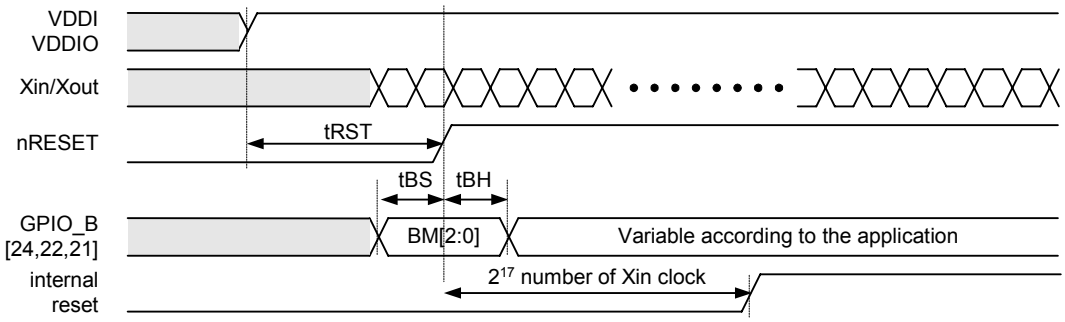
20 BOOTING PROCEDURE

20.1 Overview

In the TCC76x, there is an internal boot ROM for system initialization process. It contains the fundamental routines for system initialization or boot procedure through various interface such as USB, NAND flash, and I2C.

There are 5 modes for booting procedure. Figure 20.1 illustrates the timing of reset sequence at power-up. During this process, the boot mode is selected by the state of GPIO_B[24,22,21] at nRESET going to high.

Table 20.1 represents the boot mode of the TCC76x.



tBH : Hold time for boot mode setting. Minimum 10ns
tBS : Setup time for boot mode setting. Minimum 10ns
tRST : Time of reset activation must be maintained during power-up. Depending upon the stabilization time of crystal oscillator. Typically about 10us.

Figure 20.1 Reset Sequence

Table 20.1 Booting Mode of the TCC76x

BM[2:0]	Description
x1x	**F/W download from USB interface** If one of other boot processing (except external boot) fails, it starts this boot procedure automatically.
001	**I2C or NAND boot** I2C interface using GPIO_D17 as I2C clock and GPIO_D16 as I2C data. NAND chip enable is controlled either by GPIO_A7 or A6 or D13 or D12, and NAND out-enable is controlled by nCS2. It can be used to attach serial EEPROM acquiring another function, or can remove NOR flash by put the F/W code in NAND flash.
100	**NOR boot, F/W download from USB I/F**. NOR must be attached to nCS3 pin, and bus width can be configured by GPIO_A[9:8]. NOR can contain encrypted code or normal code. If NOR code is corrupted, the TCC76x automatically changes to USB boot mode so user can fix NOR contents via USB interface.
101	**Development mode** JTAG and SDRAM are enabled, and the base address of SDRAM is remained. The TCC76x is waiting for JTAG connection while toggling the GPIO_A[0] output.
000	**NOR boot without encryption** NOR flash must be attached to nCS3 pin. In the TCC760 and TCC761 the NOR flash is externally attached to nCS3. In the other TCC76x derivatives with on chip NOR flash, the nCS3 must be externally connected to FCSN pin.

20.2 External ROM Boot without Encryption (BM == 000)

It supports an external boot ROM.
When external boot mode, the sequence begins from external ROM that is attached to nCS3.

The bus width of external boot ROM can be determined by state of GPIO_A[9:8] at the rising edge of nRESET pin. If GPIO_A[9:8] == 0, the bus width is 16bit, if GPIO_A[9:8] == 1, it is 8bit, otherwise, it is 32bit. (Refer to the chapter of memory controller for more details)

20.3 USB Boot (BM == x1x)

This mode is mainly for firmware upgrade mode. In this mode, user can download a program into internal SRAM and execute. The procedure of this mode is as follows.

i) The TCC76x makes internal SRAM area starts from zero, and copies USB service routine to internal SRAM area.
ii) It change control flow from boot ROM to internal SRAM where the USB service routine just copied.
iii) It waits until USB connection is established.
iv) Once it is connected, host transfers first the parameter for USB loader routine including start address, destination address, and the amount of data to be transferred.
v) The TCC76x starts communicating between a host PC with fixed amount of data which is called as packet.
vi) At every successful reception of packet, it copies that where the destination address pointed, and after all amount of data has been copied, it starts program where the start address pointed.

Normally, the program downloaded is for writing user system firmware to non-volatile memory like NOR or NAND flash.

To use USB boot, the clock frequency of XIN must be 12MHz. The internal PLL is used to generate 48MHz of USB clock from XIN.

The following figure illustrates the sequence of USB boot mode described above.

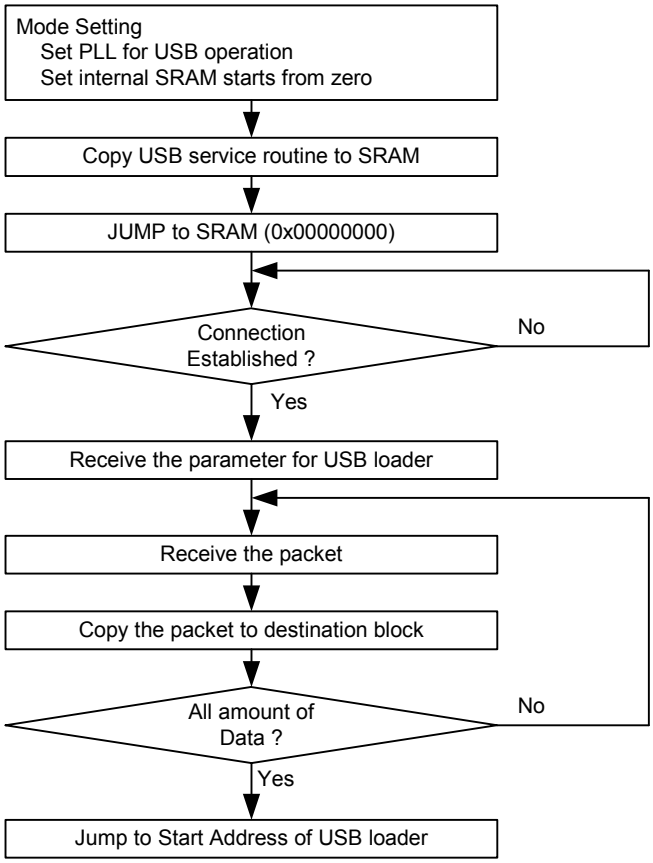


Figure 20.2 USB boot procedure

20.4 I²C or NAND Boot (BM == 001)

There are 2 modes in the TCC76x when BM[2:0] is equal to 001. One is booting from serial EEPROM through I2C interface and the other is booting from NAND flash.
The EEPROM must have I2C address of 0xA0 (for write) and 0xA1 (for read), and the NAND chip enable is controlled either by GPIO_A7 or GPIO_A6 or GPIO_D13 or GPIO_D12, and NAND out-enable is connected via nCS2 pin.

The procedure checks if there exist EEPROM first, the I2C interface must be connected via GPIO_D17 for clock and GPIO_D16 for data. If there exist an EEPROM, the procedure follows I2C boot sequence or it checks if NAND flash is connected with some GPIO pins. The sequence of checking starts from GPIO_A7, then GPIO_A6, then GPIO_D13, and end with GPIO_D12.

The boot sequence of I2C interface is as follows.

i) Read init line from EEPROM. The init line consists of the following information.
   1st word ~ 2nd word: security information
   3rd word : size of code.
ii) Check if the security information is correct.
iii) Decrypt codes and copy them to internal SRAM (starts from 0x30000000).
iv) After all amount of codes are decrypted and copied, the program executes from the start of internal SRAM (0x30000000).

It is considered that the output enable of NAND flash is to be connected with nCS2. The boot sequence of NAND flash is as follows.

i) Check if device id exist in the device id table while changing chip select pin from GPIO_A7 to GPIO_D12. (GPIO_A7 → GPIO_A6 → GPIO_D13 → GPIO_D12)
ii) Set CSCFG2 register according to device id value.
iii) Read data by 512 bytes unit from the last page down to half of NAND size until the ECC (SSFDC standard) of them and the 1st and 2nd word in them are all correct. Select lower or upper half of 512 bytes as an initialization code block according to the result of ECC checking.
   1st word ~ 2nd word: security information.
iv) If the correct block is found, copy the remaining of code in selected block from the 3rd word to internal SRAM (starts from 0x30000000). After all amount of codes are copied (initialization codes are not encrypted), the program sequence is changed to internal SRAM (0x30000000). And these codes take responsibility of the remaining boot process.

The overall flow of I2C and NAND boot is illustrated in the Figure 20.3

The supported NAND flash types are as follows.

Table 20.2 Supported NAND flash types

Size (bytes)	Size of Page (bytes)	Number of Page	CADR	Device ID x8 / x8 / x16 / x16
8M	512	16K	3	39 / E6 / 49 / 59
16M	512	32K	3	33 / 73 / 43 / 53
32M	512	64K	3	35 / 75 / 45 / 55
64M	512	128K	4	36 / 76 / 46 / 56
128M	512	256K	4	78 / 79 / 72 / 74
256M	512	512K	4	71
512M	512	1024K	4	DC
128M	2048	64K	4	A1 / F1 / B1 / C1
256M	2048	128K	5	AA / DA / BA / CA
512M	2048	256K	5	AC / DC / BC / CC
1G	2048	512K	5	A3 / D3 / B3 / C3
2G	2048	1024K	5	A5 / D5 / B5 / C5

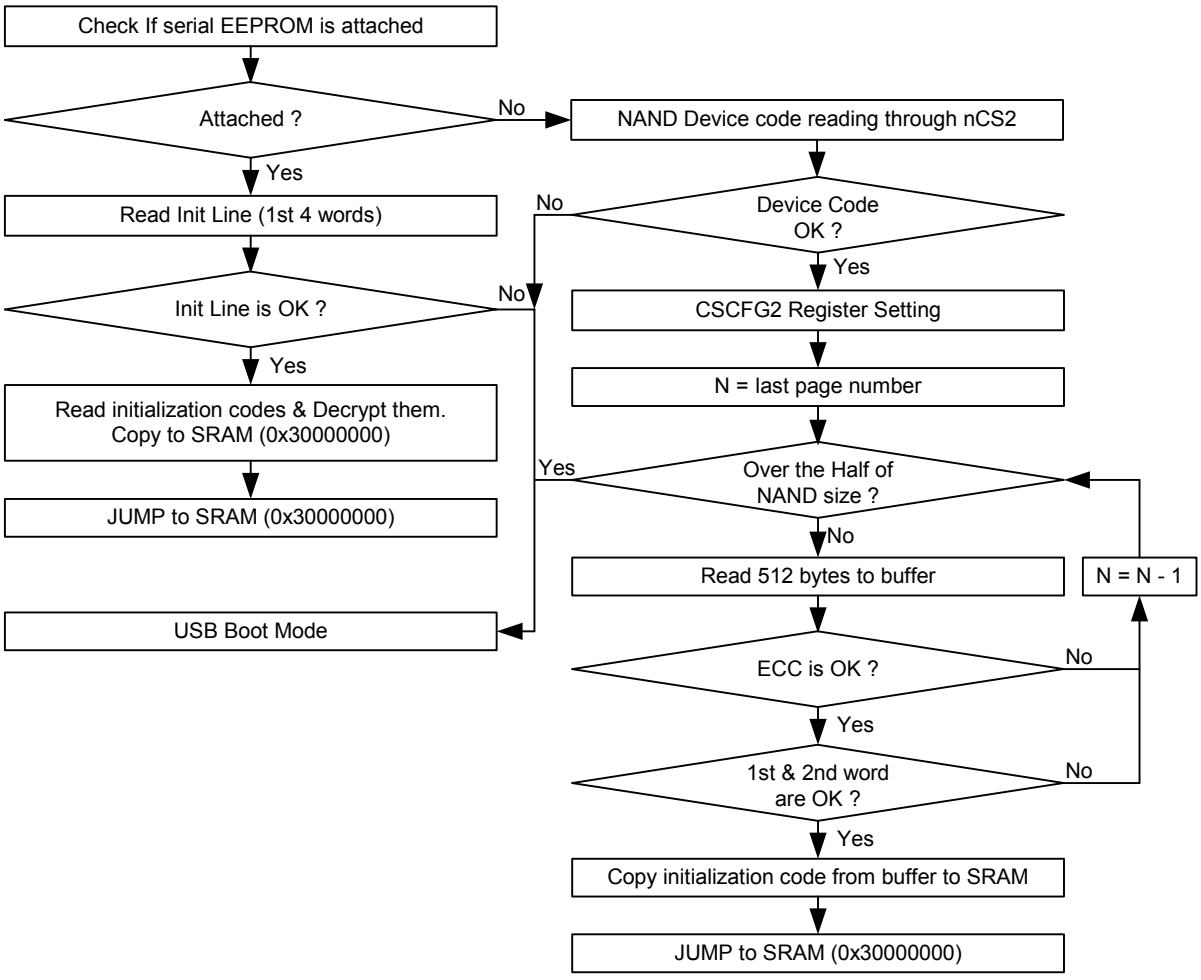


Figure 20.3 I2C and NAND boot procedure

20.5 External ROM Boot with Encryption (BM == 100)

The NOR flash must be connected via nCS3 signal. The boot sequence of this mode is as follows.

i) Read init line from NOR flash. The init line consists of the following information.
   1st word ~ 2nd word: security information
   3rd word : size of initialization code.
ii) If 1st or 2nd word is 0xFFFFFFFF, it goes to USB boot mode for F/W downloading.
iii) If 1st and 2nd word don't contain security information, then it calculates CRC-32 for the 1st 512kbytes of NOR flash and compare the CRC-32 code with 6th word of NOR flash. If the CRC checking is success, it goes to external NOR boot by jumping 0x70000000. Or if the CRC check is failed, it goes to USB boot mode for F/W downloading.
iv) If the 1st and 2nd word are correct, read initialization code from the next data of init line, and copy them to internal SRAM (starts from 0x30000000). After all amount of codes are copied (initialization codes are not encrypted), the program make a call (branch with link) command to internal SRAM (0x30000000). The initialization code must be encapsulated by the entrance command of 'STR LR, [SP - #4]!', and the exit command of 'LDR PC, [SP], #4'.
v) The initialization code must make arrange the memory area so that the zero base area (0x00000000 ~ 0x0FFFFFFF) can contain the main F/W code and then goes back to booting sequence while setting r0 register to the start address of F/W code.
vi) Read the size of F/W code at the address designated by r0 register.
vii) The F/W code is read from the next address of the r0 register and decrypted and copied to the zero base area (0x00000000 ~ 0x0FFFFFFF).
viii) After all of amount of F/W codes are decrypted and copied, the program jumps to 0x00000000.

Figure 20.4 illustrates the allocation map of encrypted F/W code in NOR flash.

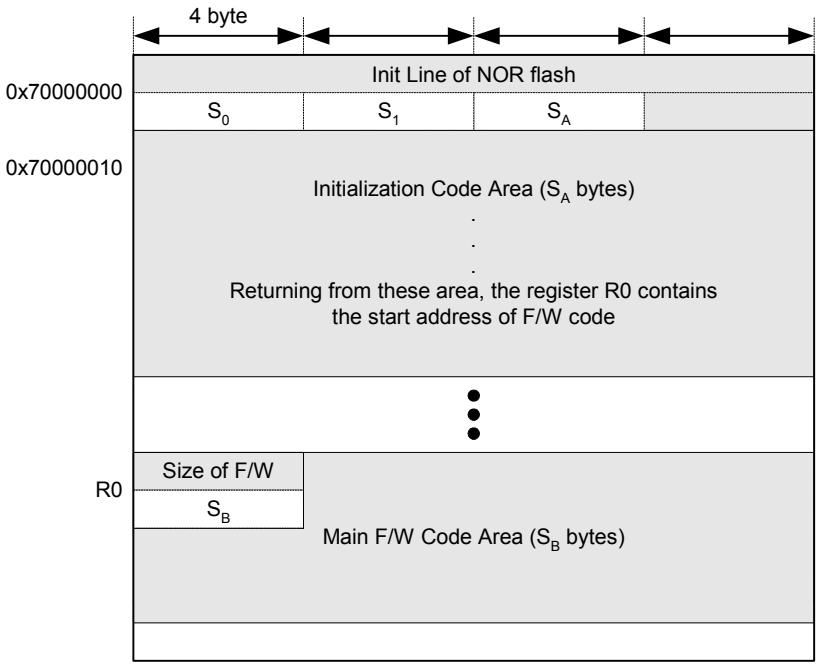


Figure 20.4 Allocation of encrypted F/W code

20.6 Development mode (BM == 101)

To ease the effort for starting development with the TCC76x, the TCC76x provides development mode in booting. In this mode, JTAG and SDRAM interface are enabled and set protection unit of the TCC76x appropriately.

The Table 20.3 describes the region setting in this mode.

Table 20.3 Region Settings in Development Mode

Region #	Start	End	I Cache	D Cache	Buffer	Protection
0	0x00000000	0xFFFFFFFF	Disabled	Disabled	Disabled	Full Access
1	0x20000000	0x3FFFFFFF	Disabled	Disabled	Disabled	Full Access
2	0x40000000	0x4FFFFFFF	Disabled	Disabled	Disabled	Full Access
3	0x50000000	0x5FFFFFFF	Disabled	Disabled	Disabled	Full Access
4	0x60000000	0x6FFFFFFF	Disabled	Disabled	Disabled	Full Access
5	0x70000000	0x7FFFFFFF	Disabled	Disabled	Disabled	Full Access
6	0x80000000	0xFFFFFFFF	Disabled	Disabled	Disabled	Full Access
7	0x3000F000	0x3000FFFF	Disabled	Disabled	Disabled	Full Access

*) The region of higher number has higher priority than that of other regions. So region 7 has highest priority and region 0 has lowest priority.

After region setting finishes, it goes into a infinite loop while toggling GPIO_A[0].

21 JTAG DEBUG INTERFACE

The TCC76x has the ARM940T core as main controller, and JTAG interface for developing the application programs. It can be connected with OPENice32 of AIJI System or Multi-ICE of ARM or other third party's in-circuit emulator supporting for ARM940T core.

With the use of in-circuit emulator, users can easily develop the program for their own system. It provides hardware breakpoints, internal register monitoring, memory dump, etc. Refer to user's manual of in-circuit emulator for more detail functions of it.

Figure 21.1 shows the application circuit for JTAG interface. Care must be taken not to combine system reset with JTAG reset signal.

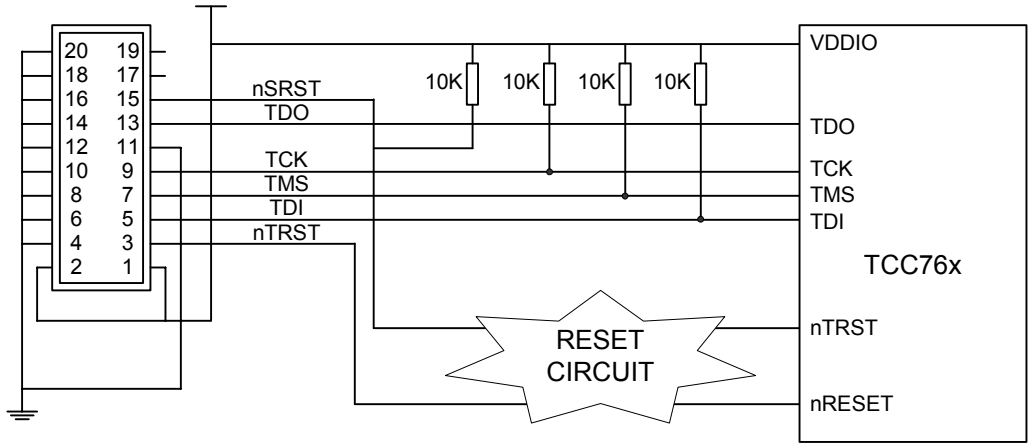


Figure 21.1 JTAG Interface Circuit Diagram

21.1 Debugging with OPENice32 & AIJI Spider

OPENice32 is a powerful and convenient emulator for ARM processor. It provides the best debugging solution for Telechips ARM processor, TCC76x series. A powerful debugger, AIJI Spider, is supplied with OPENice32.

It also provides a TCC76x device file and flash device file.
To debug the target system using TCC76x with OPENice32, you should set the Boot Mode as development mode. Refer to the Boot Procedure chapter to set the Boot Mode.

For more information, refer to OPENice32 manual or application note.

System Configuration

OPENice32 is connected to the host PC with serial, USB or Ethernet that provides high speed downloading. It is connected to the target JTAG connector with a 20-way cable.

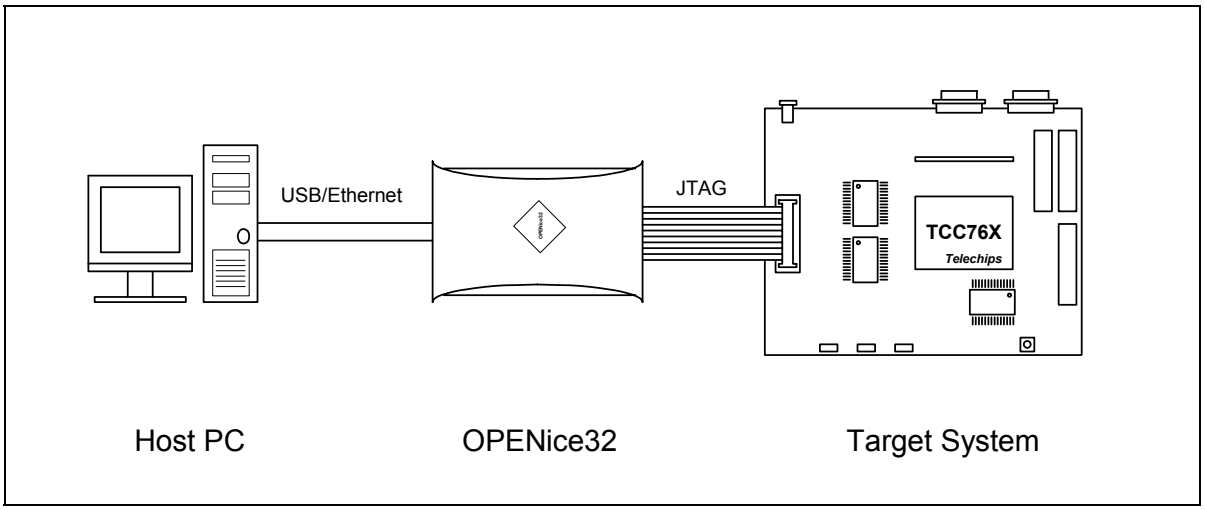
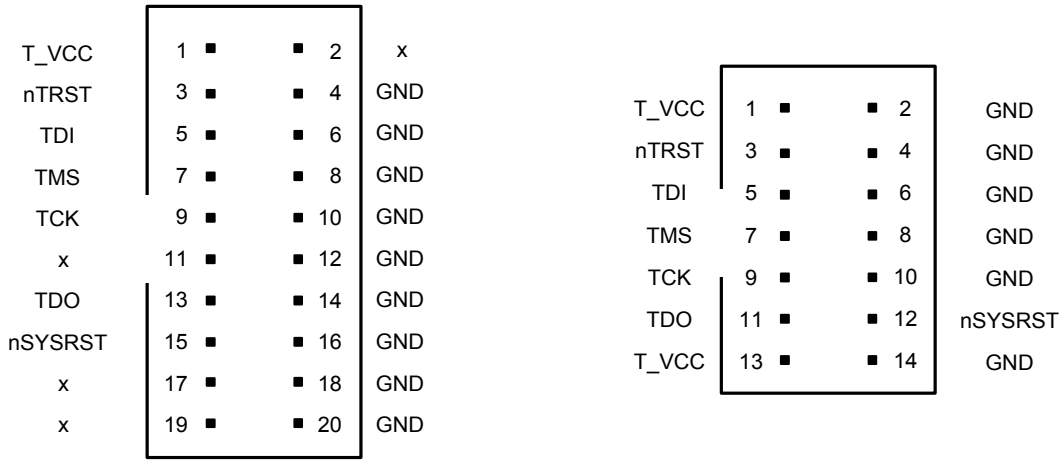


Figure 21.2 Connection between Host PC and OPENice32 and Target System

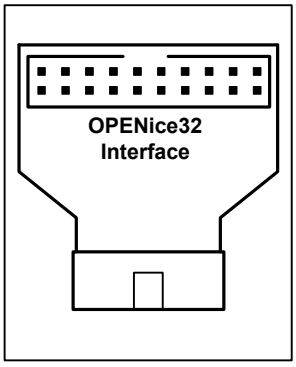
JTAG connector on the target

The following diagram shows the JTAG connector on a target system and a 20-14pin-adapter board.
When designing a target board, users can select a 14pin header or 20pin header. The pin configuration of header on the target board should be same as following diagram.



[20 pin Connector] **[14 pin Connector]**

Figure 21.3 Pin Configuration of 20 and 14 pin Connector



[20-14 Adapter]

Figure 21.4 20-14 Adapter Board

Contact Point

If you have any question regarding OPENice32, please contact AIJI System.

AIJI System.Co., Ltd.
Tel: +82-32-223-6611 email:stroh@aijisystem.com
http://www.aijisystem.com http://www.mculand.com

22 USB 2.0 & CARD INTERFACE

This section describes USB 2.0 device controller and Memory Card Interface block in the TCC766 and TCC767.

22.1 Overview

- USB 2.0 Interface
  - USB Specification 2.0 & 1.1 Compliant
  - Supports High Speed Transfers (480Mbit/sec)
  - Supports Full Speed Transfers (12Mbit/sec)
  - Supports Four Endpoints :
    - Endpoint 0 : 64 Bytes CONTROL transfer
    - Endpoint 1 : 512*2 Bytes BULK IN transaction
    - Endpoint 2 : 512*2 Bytes BULK OUT transaction
    - Endpoint 3 : 64 Bytes INTERRUPT IN transaction

- Memory Card Interfaces
  - Memory Stick (MS)
  - Memory Stick PRO(MSPRO)
  - SecureDigital Card (SD)
  - MultiMedia Card (MMC)
  - Build-in NAND Flash Memory

- Memory Stick / Memory Stick PRO Interface
  - Fully compatible with the Memory Stick Standard Format Specification Version 1.4
  - Fully compatible with the Memory Stick PRO Standard Format Specification Version 1.00
  - Auto Data CRC generating & checking
  - Memory Stick Support capacity 4/8/16/32/64/128MB
  - Memory Stick PRO Support capacity 256/512/1024MB

- Secure Digital Card / MultiMedia Card Interface
  - Fully compatible with MultiMediaCard System Specification 3.0
  - Fully compatible with Secure Digital Specification 1.01
  - MMC Support capacity 4/8/16/32/64/128MB
  - SD Support capacity 4/8/16/32/64/128/256/512MB
  - Auto Data CRC generating & checking
  - Auto Command/Response CRC generating & checking
  - Standard MMC/SPI/SD 4-bit mode interface support

- Build-In NAND Flash Memory Interface
  - Build-in hardware ECC circuit (Hamming & Reed-Solomon).
  - Support SLC(Single Level Cell) NAND Flash Memory. Ex: 128Mb,256Mb,512Mb,1Gb.
  - Support Big Block(2K+64 Bytes per page) NAND Flash Memory. Ex: 1Gb, 2Gb, 4Gb.
  - Support MLC(Multi Level Cell) NAND flash. Ex: 512Mb, 1Gb.

22.2 Register Description

Table 22.1 I/O Port Functions and Selection Addresses

Addresses					Functions	
nCS0	nCS1	A2	A1	A0	Read (nIOR)	Write (nIOW)
1	1	X	X	X	Data bus high impedance	Not used
					Control block registers	
1	0	0	X	X	Data bus high impedance	Not used
1	0	1	0	X	Data bus high impedance	Not used
1	0	1	1	0	Alternate Status	Device Control
1	0	1	1	1	Obsolete	Not used
					Command block registers	
0	1	0	0	0	Data	Data
0	1	0	0	1	Error	Features
0	1	0	1	0	Sector Count	Sector Count
0	1	0	1	1	Sector Number	Sector Number
0	1	1	0	0	Cylinder Low	Cylinder Low
0	1	1	0	1	Cylinder High	Cylinder High
0	1	1	1	0	Device/Head	Device/Head
0	1	1	1	1	Status	Command
0	0	X	X	X	Invalid address	Invalid address

Table 22.2 The Relationship of MST[2:0] Pins and Feature Register

MST[2:0]	Configuration	Feature register
111	Record in flash memory by AP. In USB Mode, First slot is NAND Flash memory, Second slot is MMC/SD and Third slot is MS/MS Pro/New MS card	0x80: direct to Flash Memory Hidden disk 0x00: direct to NAND Flash Memory FAT disk. 0x01: direct to MMC/SD card 0x02: direct to MS/MS Pro card
001	Only support MMC/SD card	0x00: direct to MMC/SD card
010	Only support MS/MS_Pro card	0x00: direct to MS/MS Pro card
011	Support two kinds of card above. And MMC/SD is the first slot in USB mode.	0x00: direct to MMC/SD card 0x01: direct to MS/MS Pro card
100	Support two kinds of card above. And MS/MS_Pro card is the first slot in USB mode.	0x00: direct to MS/MS Pro card 0x01: direct to MMC/SD card

Value of Feature register is slot number of each memory.
Fill feature register before access command

After Feature register has been filled, Initial Media Command(0x62) should be issued.

22.3 IDE Commands

Table 22.3 Summary of IDE Commands

	Command Name	Command Code	Description
Standard Command	ReCalibrate	0x1F	Refer to ATA/ATAPI-4 Standard.
	ReadSectors	0x20	
	WriteSectors	0x30	
	ReadVerify	0x40	
	Seek	0x70	
	TranslateSector	0x87	
	Diagnostics	0x90	
	ReadMultiple	0xC4	
	WriteMultiple	0xC5	
	SetMultiple	0xC6	
	ReadBuffer	0xE4	
	WriteBuffer	0xE8	
	AtaIdentifyDrive	0xEC	
Vendor Command	IDEGetMaxLun	0x60	Get Maximum number of LUN value.
	ATACheckMedia	0x61	Check Media Status.
	ATAInitial	0x62	Initialize Media.
	GetSerialNumber	0x63	Read Serial Number(16bytes), VID and PID.
	SetIDESuspend	0x64	Go to Suspend Mode.

22.3.1 Standard Commands

The Commands except PACKET and SERVICE commands are listed in Table 22.3. Refer to the ATA/ATAPI-4 Standard for detailed description.

22.3.2 Vendor Commands

There are five vendor commands as described in the following table. Before access command, Feature register should be written.

Table 22.4 Vendor Commands

Name	Code	Protocol	Input	Output	Description
IDEGetMaxLun	0x60	Non-data	None	Number of slots	Get slot number. Register Sector Number will response how many slot is supported.
ATACheckMedia	0x61	Non-data	None	Media status	Check media connection. Error register response media status. Definition of error register: if bit 1 is true, and if bit 4 is true. no media insert, else (false) media is insert if bit 5 is true, media write protect, else (false) media write enable if bit 6 is true, media initial failed, else (false) media initial pass if bit 7 is true, same with bit 4 if bit 1 is false, and if bit 5 is true, media change, (memory card already been change, need to initial command 0x62)
ATAInitial	0x62	Non-data	None	None	Initialize Media. After power on or media change, Initial media command must be executed.
GetSerialNumber	0x63	PIO data in	None	512 Bytes of S/N, VID and PID	Read Serial Number(16bytes), VID and PID. It is some control flow with command 0xEC. 512 bytes will be sent out as follows, Byte: Description 0: Valid serial number length 1 ~ 24: Serial Number (valid data is according length) 25: VID (Low Byte) 26: VID(High Byte) 27: PID(Low Byte) 28: PID(High Byte)
SetIDESuspend	0x64	Non-data	None	None	When this command is accessed, it will go to suspend mode and force pin ACT_nSPND low. When next IDE command access, it will auto wake up and force pin ACT_nSPND high.

23 ELECTRICAL SPECIFICATION

Unless otherwise specified, all the electrical specifications are valid only for the TCC760 / TCC761 signals.

23.1 Absolute Maximum Ratings

Table 23.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
DC Supply Voltage for 3.3V I/O	V_{DDIO}	3.8	V
DC Supply Voltage for 1.8V I/O	V_{DD_OSC}	2.5	V
DC Supply Voltage for Internal Digital Logic	V_{DDI}	2.5	V
DC Supply Voltage for Analog Part of ADC	V_{DDA_ADC}	3.8	V
DC Supply Voltage for PLL	V_{DDA_PLL}	2.5	V
Digital Input Voltage for 3.3V Input Buffer	V_{IN}	4.6	V
Digital Input Voltage for 1.8V Input Buffer	V_{IN_OSC}	2.5	V
Analog Input Voltage for ADC	V_{INA}	0 ~ V_{DDA_ADC}	V
DC Input Current	I_{IN}	+/- 200	mA
Storage Temperature	T_{STG}	-45 to 125	^{o}C

Notes:

1. Absolute maximum ratings specify the values beyond which the device may be damaged permanently. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Each condition value is applied with the other values kept within the following operating conditions and functional operation under any of these conditions is not implied.
2. All voltages are measured with respect to VSS unless otherwise specified.
3. V_{DDI} must always be less than or equal to V_{DDIO} or V_{DD_OSC}
4. V_{DD_OSC} must always be less than or equal to V_{DDIO}

23.2 Recommended Operating Conditions

Table 23.2 Recommended Operating Conditions

Parameter	Symbol	MIN	TYP	MAX	Unit
DC Supply Voltage for 3.3V I/O (TCC760/TCC761 only)	V_{DDIO}	1.65	-	3.6	V
DC Supply Voltage for 3.3V I/O	V_{DDIO}	2.7	-	3.6	V
DC Supply Voltage for 1.8V I/O	V_{DD_OSC}	1.65	-	1.95	V
DC Supply Voltage for Internal Digital Logic	V_{DDI}	1.65	-	1.95	V
DC Supply Voltage for Analog Part of ADC	V_{DDA_ADC}	3.0	-	3.6	V
DC Supply Voltage for PLL	V_{DDA_PLL}	1.65	-	1.95	V
Digital Input Voltage for 3.3V Input Buffer	V_{IN}	-0.1	-	V_{DDIO} + 0.15	V
Digital Input Voltage for 1.8V Input Buffer	V_{IN_OSC}	-0.1	-	V_{DD_OSC} + 0.15	V
Digital Output Voltage	V_{OUT}	-0.1	-	V_{DDIO} + 0.15	V
Analog Input Voltage for ADC	V_{INA}	0.0		V_{DDA_ADC}	V
External Loop Filter Capacitance for PLL	L_F	315	350	385	pF
Operating Temperature	T_{OPER}	-30		85	^{o}C

23.3 Electrical Characteristics

Table 23.3 Electrical Characteristics

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Unit
High Level Input Voltage	V_{IH}	V_{DDIO} = 3.3V ± 0.3V	0.7 V_{DDIO}			V
		V_{DDIO} = 1.8V ± 0.15V	0.8 V_{DDIO}			V
Low Level Input Voltage	V_{IL}	V_{DDIO} = 3.3V ± 0.3V			0.8	V
		V_{DDIO} = 1.8V ± 0.15V			0.57	V
Schmitt Trigger, Positive-going Threshold	V_{T+}	V_{DDIO} = 3.3V ± 0.3V			2.0	V
		V_{DDIO} = 1.8V ± 0.15V			1.27	V
Schmitt Trigger, Negative-going Threshold	V_{T-}	V_{DDIO} = 3.3V ± 0.3V	0.8			V
		V_{DDIO} = 1.8V ± 0.15V	0.57			V
High Level Input Current	I_{IH}	V_{IN} = V_{DDIO}	-10		10	μA
Low Level Input Current	I_{IL}	V_{IN} = V_{SS}	-10		10	μA
Low Level Input Current (pull-up enabled)			-66	-33	-10	μA
High Level Output Voltage	V_{OH}	V_{DDIO} = 3.3V ± 0.3V I_{OH} = -4/6/8/12mA	2.4			V
		V_{DDIO} = 1.8V ± 0.15V I_{OH} = -2/3/4/6mA	1.1			V
Low Level Output Voltage	V_{OL}	V_{DDIO} = 3.3V ± 0.3V I_{OL} = 4/6/8/12mA			0.4	V
		V_{DDIO} = 1.8V ± 0.15V I_{OL} = 2/3/4/6mA			0.5	V
Tri-state Output Leakage Current	I_{OZ}	V_{OUT} = V_{SS} or V_{DDIO}	-10		10	μA
Quiescent Supply Current for I/O	I_{DS_IO}	V_{DDIO} = 3.3V, No Load V_{IN} = V_{SS} or V_{DDIO}			10	μA
XIN/XOUT Operating Frequency	F_{OSC1}		10	-	40	MHz
XTIN/XTOUT Operating Frequency	F_{OSC2}		32	-	100	kHz
PLL Dynamic Current	I_{DD_PLL}	V_{DDA_PLL} = 1.8V			3	mA
PLL Power Down Current	I_{PD_PLL}	V_{DDA_PLL} = 1.8V			20	μA
PLL Input Frequency	F_{IN_PLL}	V_{DDA_PLL} = 1.8V	5		50	MHz
PLL Output Frequency	F_{OUT_PLL}	V_{DDA_PLL} = 1.8V	50		500	MHz
PLL Locking Time	T_{LT}	V_{DDA_PLL} = 1.8V		150		μs
ADC Differential Nonlinearity	DNL	V_{DDA_ADC} = 3.3V		± 0.8	± 1.0	LSB
ADC Integral Nonlinearity	INL	V_{DDA_ADC} = 3.3V		± 1.0	± 2.0	LSB
ADC Offset Voltage Error (Top / Bottom)	EOT/EOB	V_{DDA_ADC} = 3.3V		3.0	8.0	LSB
ADC Maximum Conversion Rate	f_C	f_{CKIN} = 2.5 MHz			500	KSPS
ADC Dynamic Current	I_{DD_ADC}	V_{DDA_ADC} = 3.3V			4	mA
ADC Standby Supply Current	I_{PD_ADC}	V_{DDA_ADC} = 3.3V			20	μA

Ta = 25°C, V_{DDIO} = V_{DDA_ADC} = 3.3V ± 0.3V, V_{DD_OSC} = V_{DDA_PLL} = V_{DDI} = 1.8V ± 0.15V, V_{SSIO} = V_{SSI} = V_{SSA_PLL} = V_{SSA_ADC} = 0.0V unless otherwise specified.

V_{DDIO} = 1.8V ± 0.15V condition is valid only for the TCC760 and TCC761.

Not all parameters are tested. Guaranteed by design characterization.

23.4 Absolute Maximum Ratings – NOR Flash

Table 23.4 Absolute Maximum Ratings – NOR Flash

Parameter	Symbol	Rating	Unit
DC Supply Voltage for NOR Flash	V_{DD_NOR}	-0.5 to 3.8	V
Input Voltage for NOR Flash	V_{IN_NOR}	-0.5 to V_{DD_NOR} + 0.5	V
DC Input Current for NOR Flash	I_{IN_NOR}	+/- 100	mA
Storage Temperature	T_{STG_NOR}	-45 to 85	°C

The voltage difference between V_{DDIO} and V_{DD_NOR} must always be within 0.3V

23.5 Recommended Operating Conditions – NOR Flash

Table 23.5 Recommended Operating Conditions – NOR Flash

Parameter	Symbol	MIN	TYP	MAX	Unit
DC Supply Voltage for NOR Flash	V_{DD_NOR}	2.7	-	3.6	V
Input Voltage for NOR Flash	V_{IN_NOR}	-0.1	-	V_{DD_NOR} + 0.15	V
Operating Temperature for NOR Flash	T_{OPER_NOR}	0		70	°C

23.6 Electrical Characteristics – NOR Flash

Table 23.6 Electrical Characteristics – NOR Flash

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Unit
High Level Input Voltage	V_{IH_NOR}	V_{DD_NOR} = 3.3V ± 0.3V	0.7 V_{DD_NOR}			V
Low Level Input Voltage	V_{IL_NOR}	V_{DD_NOR} = 3.3V ± 0.3V			0.8	V
High Level Input Current	I_{IH_NOR}	V_{IN_NOR} = V_{DD_NOR}	-10		10	μA
Low Level Input Current	I_{IL_NOR}	V_{IN_NOR} = V_{SS_NOR}	-10		10	μA
High Level Output Voltage	V_{OH_NOR}	V_{DD_NOR} = $V_{DD\_NOR\_MIN}$ I_{OH_NOR} = -100μA	V_{DD_NOR} - 0.2			V
Low Level Output Voltage	V_{OL_NOR}	V_{DD_NOR} = $V_{DD\_NOR\_MIN}$ I_{OL_NOR} = 100μA			0.2	V
Output Leakage Current	I_{OZ_NOR}	V_{OUT_NOR} = V_{SS_NOR} or V_{DD_NOR}	-10		10	μA
Supply Current	I_{DD_NOR}	Read			30	mA
		Program / Erase			30	mA
Stanby Supply Current	I_{DS_NOR}	FCSN = V_{DD_NOR}		3	20	μA
Endurance		Program / Erase		100,000		Cycles

Ta = 25°C, V_{DD_NOR} = V_{DDIO} = 3.3V ± 0.3V, V_{SS_NOR} = V_{SSIO} = 0.0V unless otherwise specified.

Table 23.7 AC Characteristics – NOR Flash

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Unit
Read Cycle Time	t_{RC}		70			ns
Address Access Time	t_{AA}	FCSN = nOE = V_{SS_NOR}			70	ns
Chip Enable Access Time	t_{CE}	nOE = V_{SS_NOR}			70	ns
Output Enable Access Time	t_{OE}	FCSN = V_{SS_NOR}			35	ns
Chip Enable to Output High-Z	t_{CHZ}				25	ns

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Unit
Output Enable to Output High-Z	t_{OHZ}				25	ns
Output Hold Time	t_{OH}		0			ns
Address Setup Time	t_{AS}		0			ns
Address Hold Time	t_{AH}		45			ns
Data Setup Time	t_{AS}		35			ns
Data Hold Time	t_{AH}		0			ns
Chip Enable Setup Time	t_{CS}		0			ns
Chip Enable Hold Time	t_{CH}		0			ns
Output Enable Setup Time	t_{OES}		0			ns
Output Enable Hold Time	t_{OEH}		10			ns
Write Enable Pulse Width	t_{WP}		40			ns
Write Enable Pulse Width High	t_{WPH}		30			ns

Notes:

1. Measurement Condition: C_L = 30pF, Input Rise/Fall Time = 5.0ns
2. Before accessing the NOR Flash, the CSCFG3 register must be programmed appropriately to meet the above timing parameters. (Refer to section “Memory Controller”).
3. Actual access timing is determined by the value of the CSCFG3 register and Memory Controller clock (HCLK) frequency.

Not all parameters are tested. Guaranteed by design characterization.

23.7 Absolute Maximum Ratings – Audio CODEC

Table 23.8 Absolute Maximum Ratings – Audio CODEC

Parameter	Symbol	Rating	Unit
Digital Supply Voltage for Audio CODEC	V_{DDC_CDC} V_{DDB_CDC}	-0.3 to 3.63	V
Analog Supply Voltage for Audio CODEC	V_{DDA_CDC}	-0.3 to 3.63	V
Digital Input Voltage for Audio CODEC	V_{IN_CDC}	-0.3 to V_{DDB_CDC} + 0.3	V
Analog Input Voltage for Audio CODEC	V_{INA_CDC}	-0.3 to V_{DDA_CDC} + 0.3	V
Storage Temperature for Audio CODEC	T_{STG_CDC}	-45 to 125	°C

Notes:

1. The voltage difference between analog and digital grounds (V_{SS_CDC}, AGND) must always be within 0.3V.
2. V_{DDA_CDC} includes AVDD and HPVDD.
3. V_{DDC_CDC} must not exceed V_{DDA_CDC} or V_{DDB_CDC}
4. V_{DDB_CDC} must not exceed V_{DDA_CDC}
5. The voltage difference between V_{DDIO} and V_{DDB_CDC} must always be within 0.3V

23.8 Recommended Operating Conditions – Audio CODEC

Table 23.9 Recommended Operating Conditions – Audio CODEC

Parameter	Symbol	MIN	TYP	MAX	Unit
Digital Supply Voltage for Audio CODEC (Core)	V_{DDC_CDC}	1.42	1.5	3.6	V
Digital Supply Voltage for Audio CODEC (Buffer)	V_{DDB_CDC}	2.7	3.3	3.6	V
Analog Supply Voltage for Audio CODEC	V_{DDA_CDC}	2.7	3.3	3.6	V
Digital Input Voltage for Audio CODEC	V_{IN_CDC}	-0.1	-	V_{DDB_CDC} + 0.15	V
Analog Input Voltage for Audio CODEC	V_{INA_CDC}		1		V_{RMS}
Operating Temperature for Audio CODEC	T_{OPER_CDC}	-10		70	°C

23.9 Electrical Characteristics - Audio CODEC

Ta = 25°C, V_{DDA_CDC} = V_{DDB_CDC} = 3.3V, V_{DDC_CDC} = 1.5V, V_{SSA_CDC} = 0.0V, Fs = 48kHz unless otherwise specified.

Table 23.10 Electrical Characteristics - Audio CODEC Digital I/O

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Unit
High Level Input Voltage	V_{IH_CDC}	V_{DDB_CDC} = 3.3V	0.7 V_{DDB_CDC}			V
Low Level Input Voltage	V_{IL_CDC}	V_{DDB_CDC} = 3.3V			0.3 V_{DDB_CDC}	V
High Level Input Current	I_{IH_CDC}	V_{DDB_CDC} = 3.3V V_{IN_CDC} = V_{DDB_CDC}	-10		10	μA
High Level Input Current (pull-down enabled)			-10		90	μA
Low Level Input Current	I_{IL_CDC}	V_{DDB_CDC} = 3.3V V_{IN_CDC} = V_{SS_CDC}	-10		10	μA
Low Level Input Current (pull-up enabled)			-90		10	μA
High Level Output Voltage	V_{OH_CDC}	V_{DDB_CDC} = 3.3V	0.9 V_{DDB_CDC}			V
Low Level Output Voltage	V_{OL_CDC}	V_{DDB_CDC} = 3.3V			0.1 V_{DDB_CDC}	V

Table 23.11 Electrical Characteristics - Audio CODEC Analog

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Unit
SNR of Line Input	SNR_{LI}	A-weighted, 0dB Gain		90		dB
THD of Line Input	THD_{LI}	-1dB Input, 0dB Gain		-80		dB
SNR of MIC_IN	SNR_{M}	A-weighted, 0dB Gain		84		dB
THD of MIC_IN	THD_{M}	0dB Input, 0dB Gain		-60		dB
SNR of Line Output	SNR_{LO}	A-weighted, Load = 10kΩ, 50pF		100		dB
THD of Line Output	THD_{LO}	1kHz, 0dB, Load = 10kΩ, 50pF		-88	-80	dB
Headphone Max Output Power	Po	R_L = 16Ω		50		mW
SNR of Headphone Out	SNR_{H}	A-weighted		90		dB
THD of Headphone Out	THD_{H}	1kHz, Po = 10mW			0.1	%
		1kHz, Po = 20mW			1.0	%

Table 23.12 Electrical Characteristics - Audio CODEC Power

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Unit
Supply Current	I_{DD_CDC}	Record and playback (all active) No input signal		24		mA
Static Current	I_{DS_CDC}	Power down, Clock stopped No input signal		10		μA

Notes:

1. The power dissipation in the headphone is excluded.

Not all parameters are tested. Guaranteed by design characterization.

24 PACKAGE DIMENSIONS

24.1 TCC760 Package Dimension

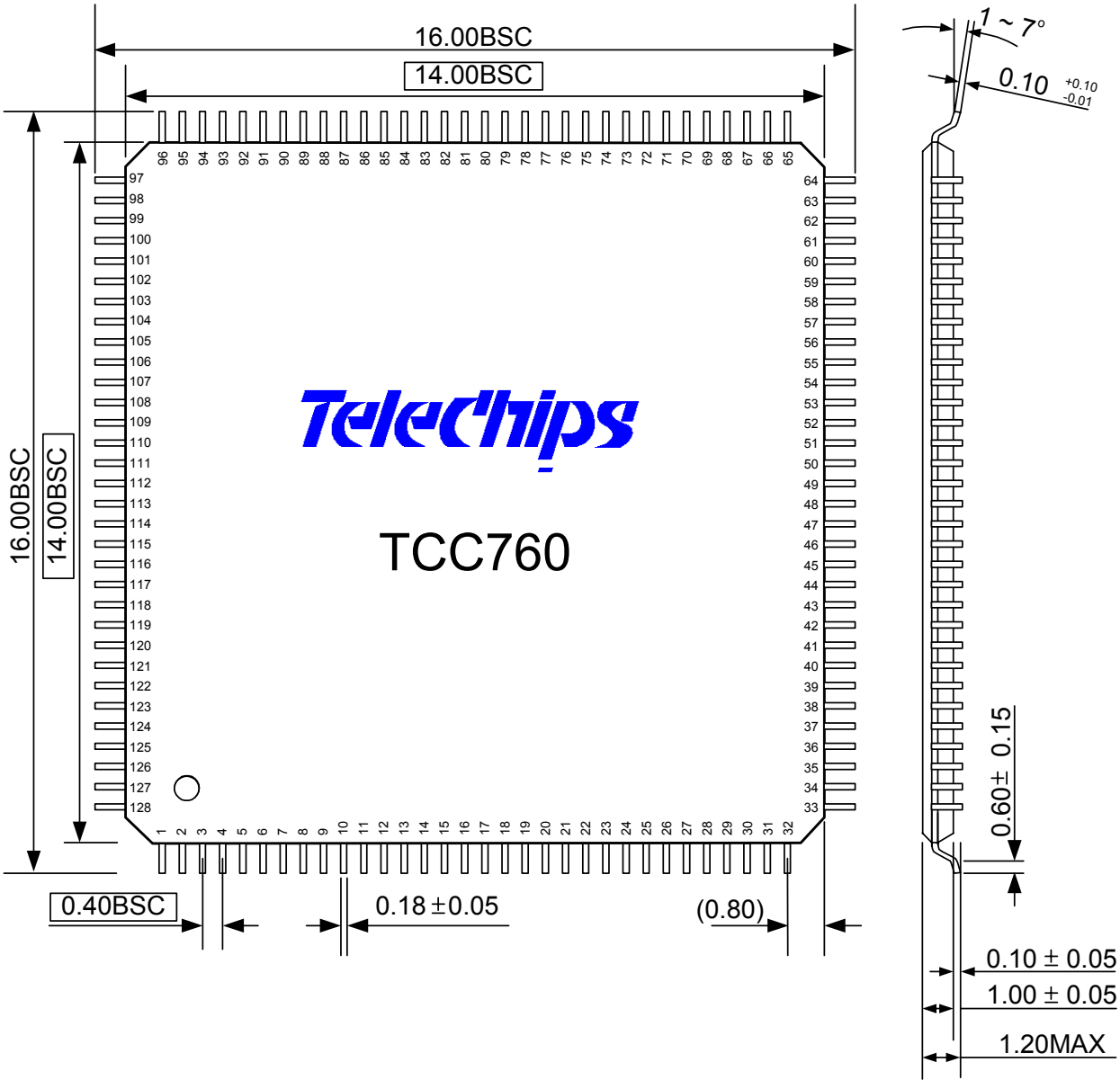


Figure 24.1 TCC760 Package Dimension (128-TQFP-1414)

24.2 TCC761 Package Dimension

24.2.1 TCC761-E Package Dimension

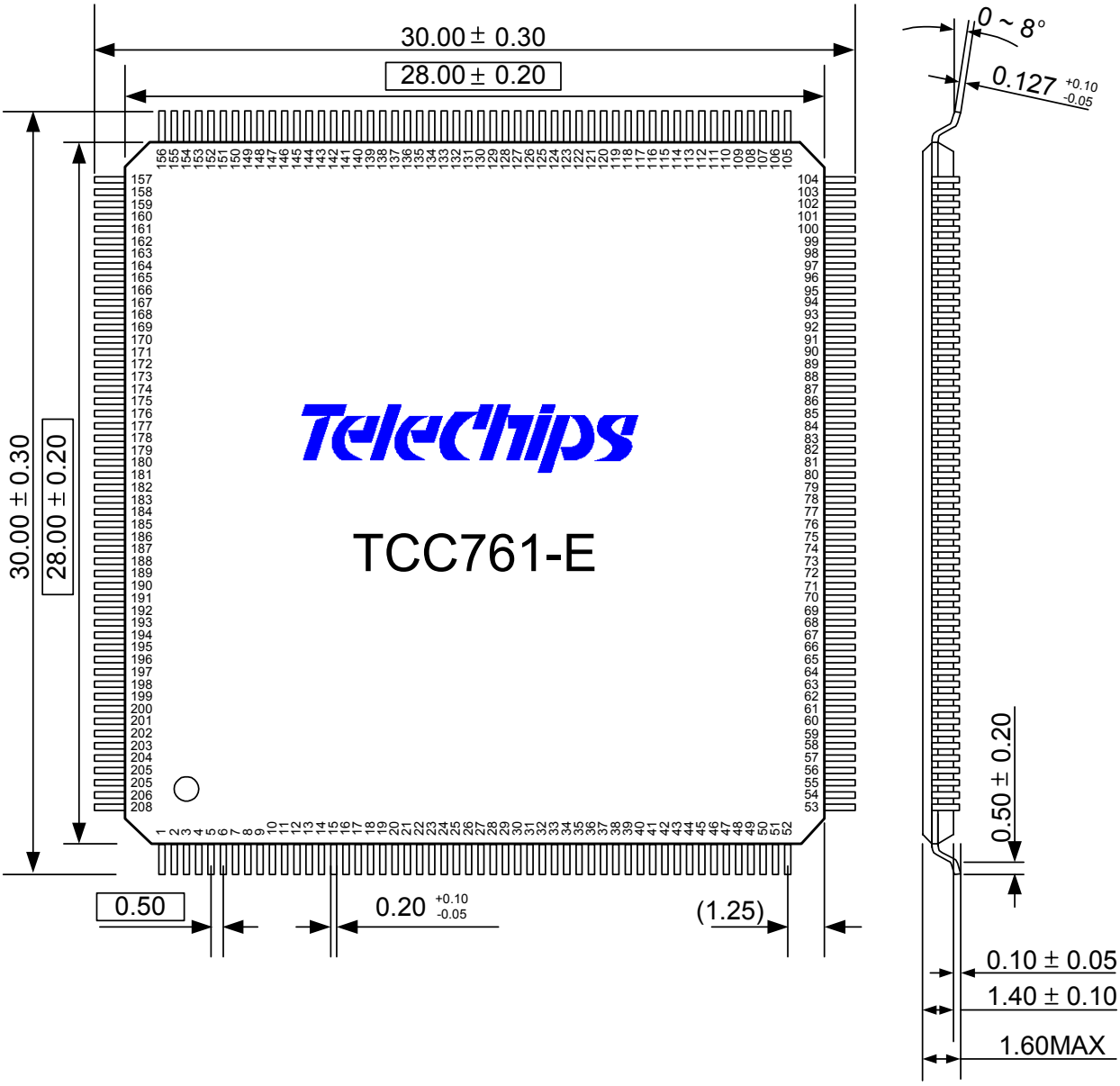


Figure 24.2 TCC761-E Package Dimension (208-LQFP-2828)

24.2.2 TCC761-Y Package Dimension

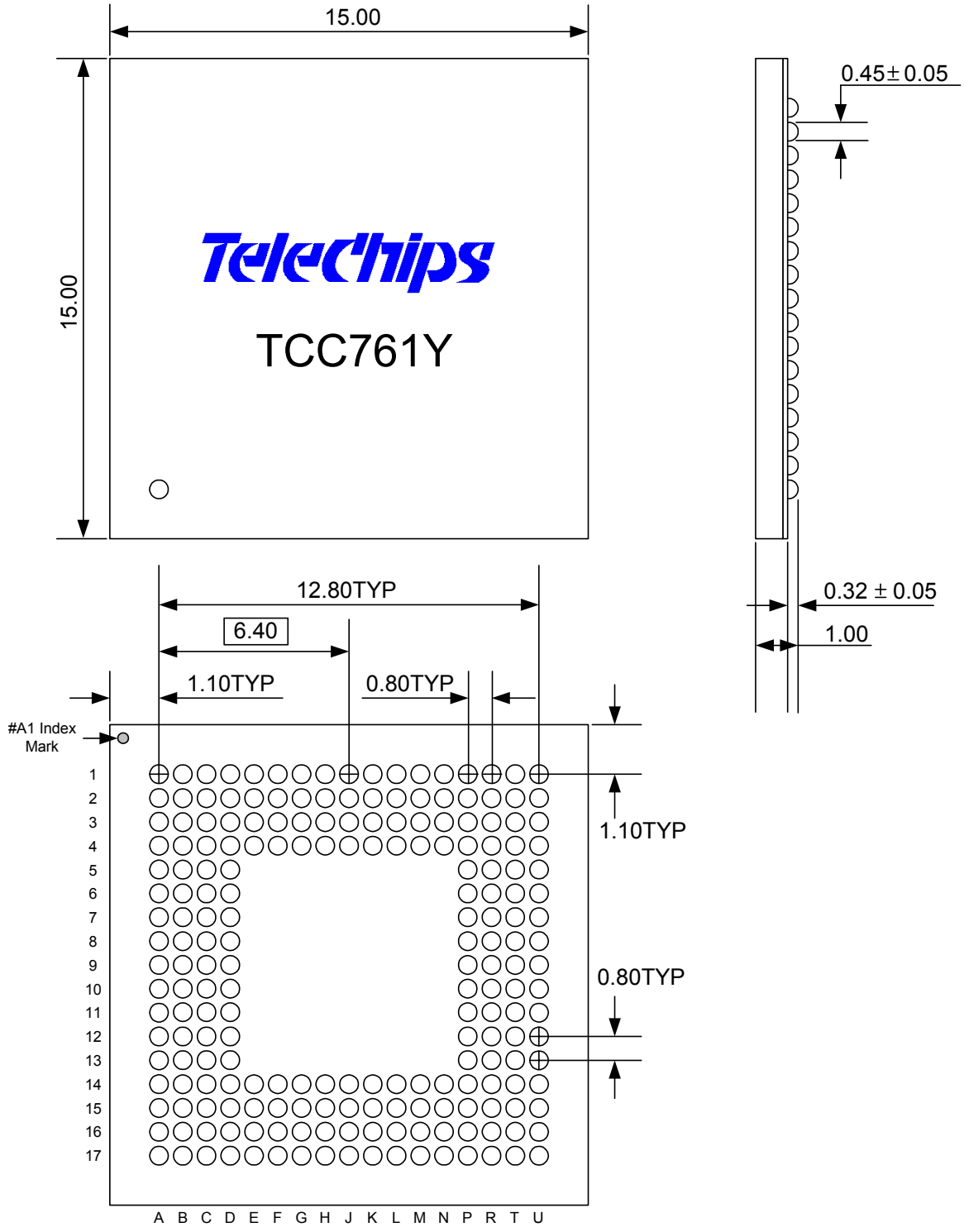


Figure 24.3 TCC761-Y Package Dimension (208-TBGA-1515)

24.3 TCC763 / TCC764 Package Dimension

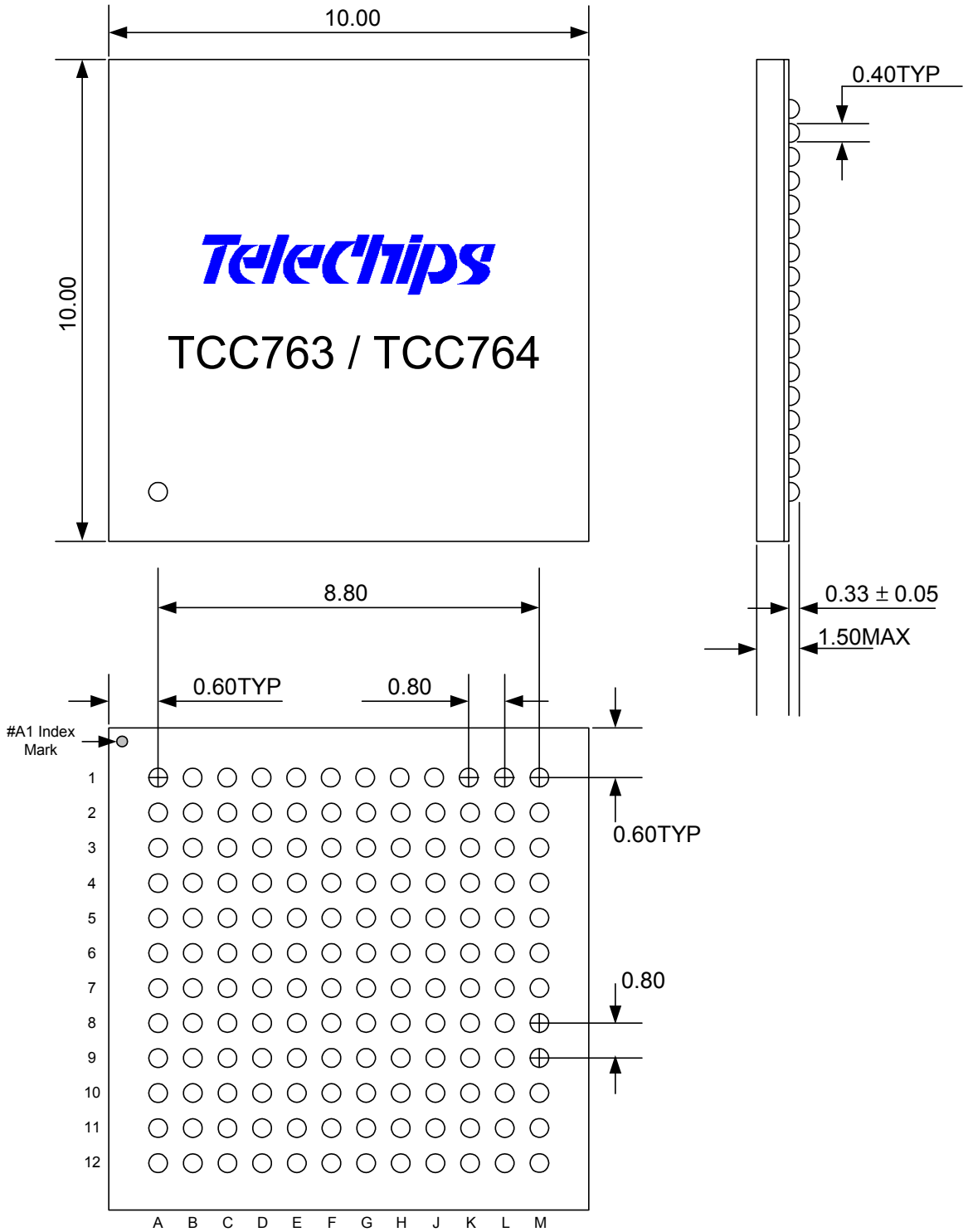


Figure 24.4 TCC763 / TCC764 Package Dimension (144-FPBGA-1010)

24.4 TCC766 Package Dimension

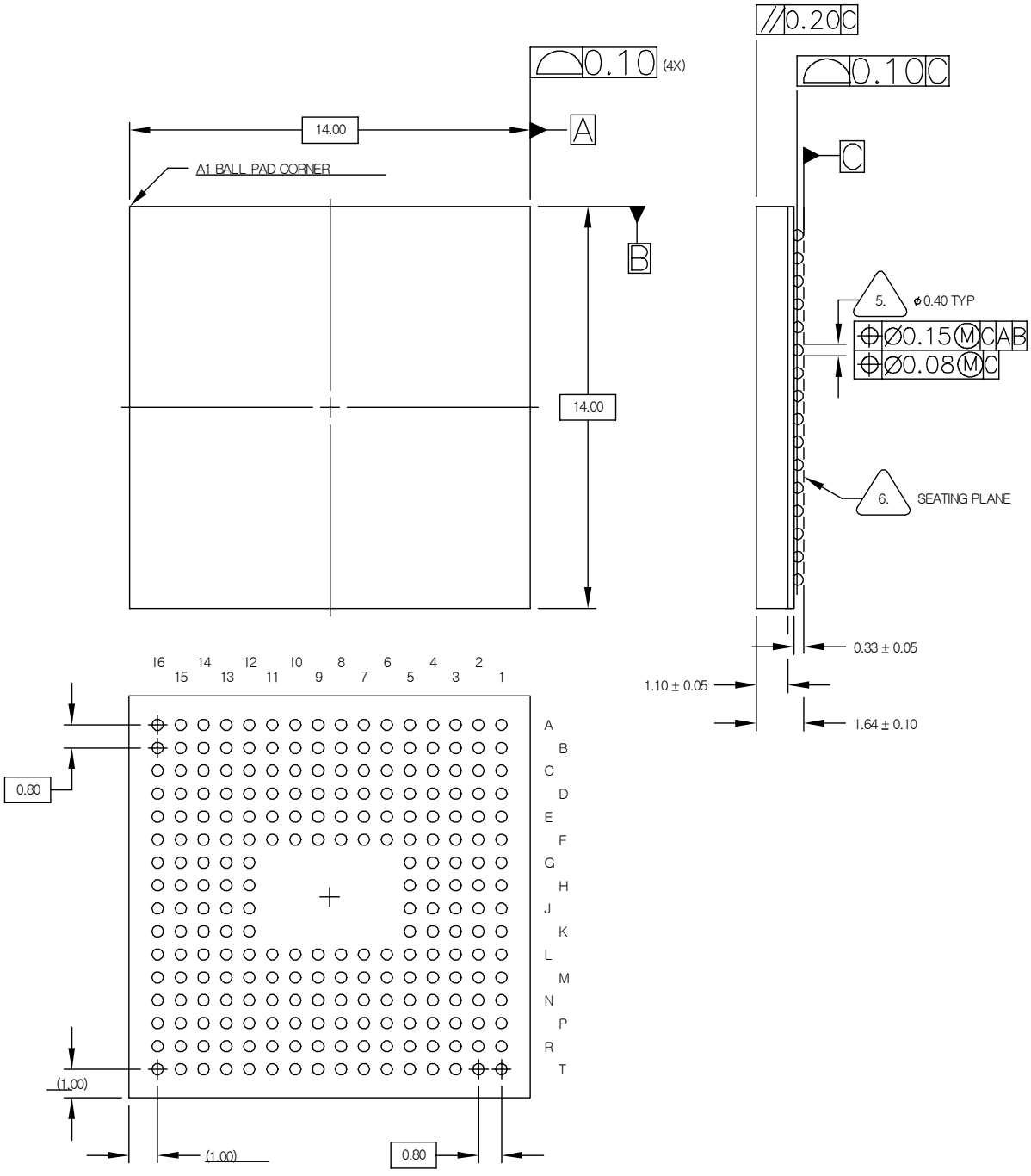


Figure 24.5 TCC766 Package Dimension (232-FPBGA-1414)

24.5 TCC767 Package Dimension

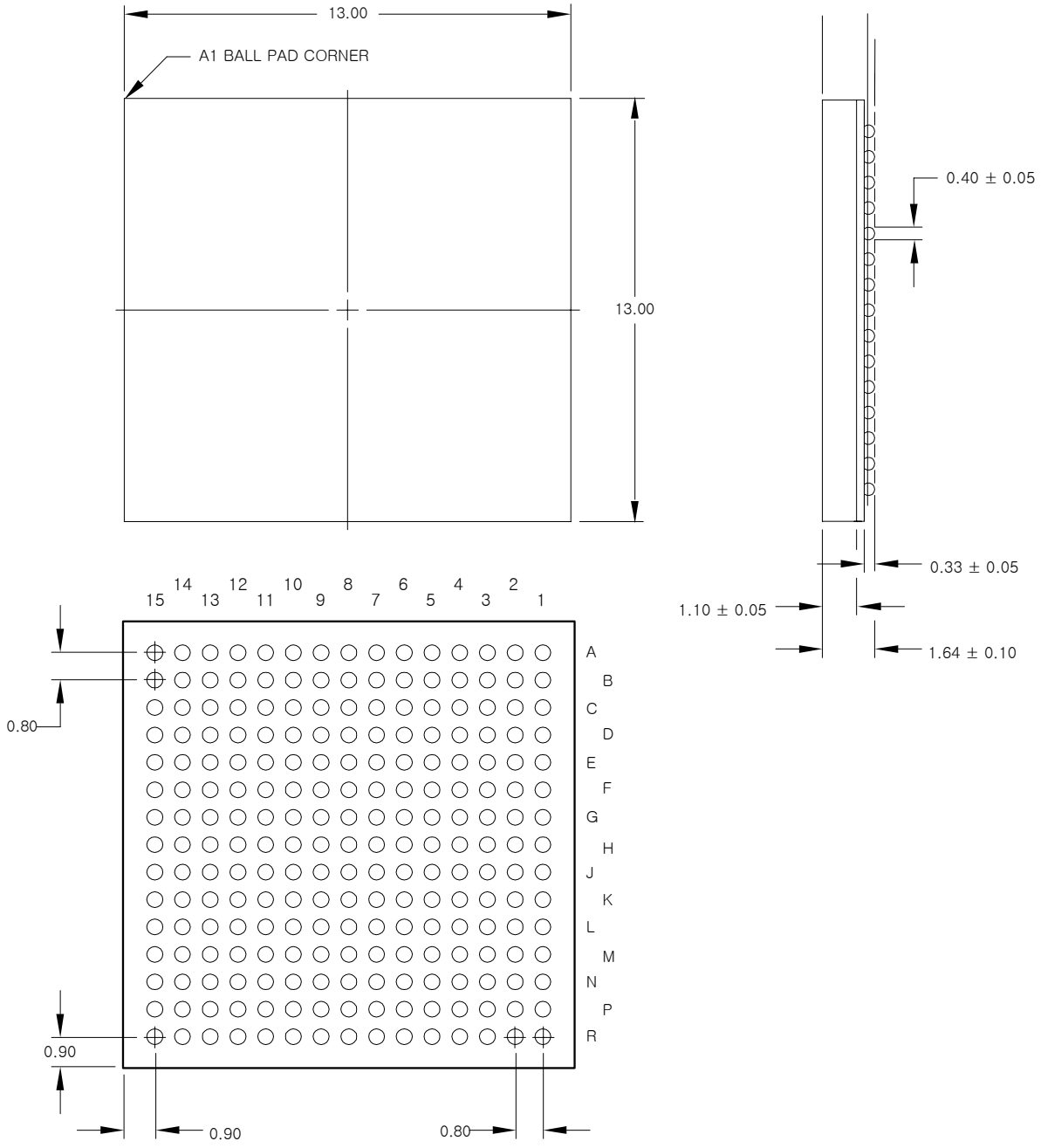


Figure 24.6 TCC767 Package Dimension (225-FPBGA-1313)

24.6 TCC768 Package Dimension

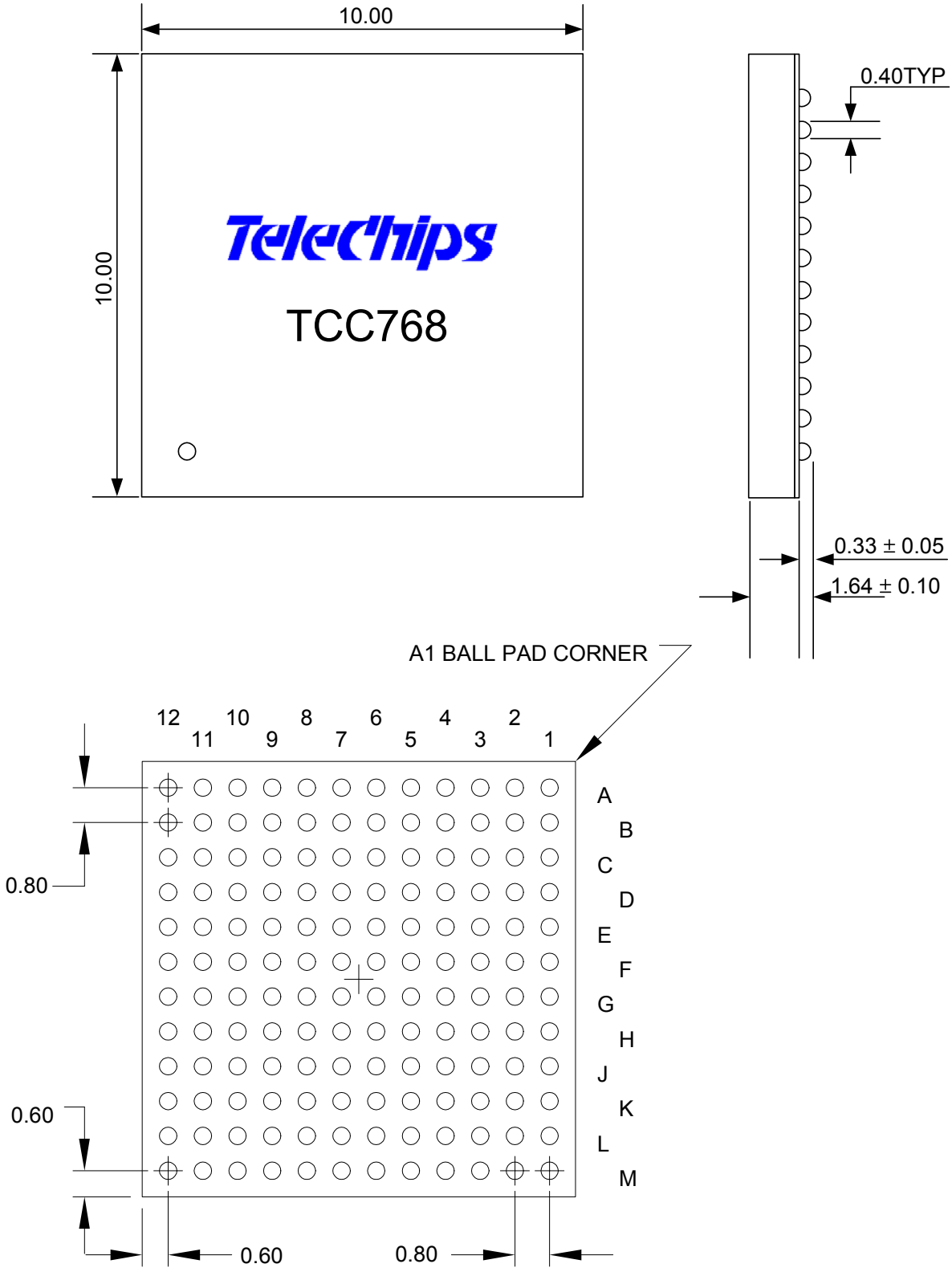


Figure 24.7 TCC768 Package Dimension (144-FPBGA-1010)

25 TCC76x vs. TCC72x

25.1 Feature Comparison

Table 25.1 Feature Comparison

Item	TCC721	TCC761	Note
Process / Typical Core Voltage	0.25µm / 2.5V	0.18µm / 1.8V	
CPU	ARM940T	ARM940T	
CPU Frequency	120MHz	140MHz	
SDRAM clock frequency	50MHz	100MHz	
DDR SDRAM support	-	100MHz	Optional
ECC Generation	Software only	Hardware ECC for SLC NAND, AGAND	
Camera Interface	-	Optional CCIR656 Input	Pins shared with GPIOs
Color Space Converter for LCD	-	YUV-to-RGB / RGB-to-YUV	
16-bpp Mode for STN LCD	-	Supported (RGB444)	
DMA Controller	1 Channel	2 Channel	
Fast GPIO Controller	-	Supports up to 15 GPIO pins	Shared with GPIO_A, D pins
I2C Master	Software only	Hardware I2C Master Core	Pins shared with GPIOs
DAI Buffer Size	2 x 4	2 x 8	
CDIF Buffer Size	4	8	
32-bit Counter	-	Programmable down to 1Hz	
IDLE/Power Down Mode Clock	XIN(12MHz)	XIN(12MHz) or XTIN (32.768kHz)	Means CPU clock source.
USB Device EP0 FIFO size	16Bytes	64Bytes	
ADC Core	500KSPS / 10bit / 2.5V	500KSPS / 10bit / .3.3V	
PLL Core Max. Frequency	300MHz	500MHz	
On-Chip Audio CODEC	Yes	-	

25.2 Pin Comparison

Table 25.2 Power Voltage Range Comparison

Pin Name	TCC72x	TCC76x	Description
VDDIO	2.7 ~ 3.3 V	1.8 ~ 3.3 V	Wide range I/O.
VDD_NOR	2.7 ~ 3.3 V	2.7 ~ 3.3 V or 1.8 V	In the TCC76x, there are 2 versions of voltage condition. One is same as that of the TCC72x and the other is for low-power consumption so it has lower voltage condition than the former one.
VDD_OSC	X	TBD ~1.8 V	In the TCC72x this pin is contained in VDDI group. In the TCC76x, it is dedicated for oscillator power for XIN and XTIN pins, so in case of lowering VDDI than 1.8V, it should be maintained at 1.8V. The voltage level of XIN and XTIN pins must not exceed VDD_OSC level.
VDDI	1.8 ~ 2.5 V	TBD ~ 1.8 V	Lower than the TCC72x The lower limit is not yet confirmed.
VDDI_ADC	1.8 ~ 2.5 V	TBD ~ 1.8 V	In the TCC72x this pin is represented as VDDI_aip. Its function is same except of voltage condition.
HPVDD VDDB_WF AVDD	2.7 ~ 3.3 V	2.7 ~ 3.3 V or 1.8 V	In the TCC76x, there are 2 versions of voltage condition. One is same as that of the TCC72x and the other is for low-power consumption so it has lower voltage condition than the former one.
VDDC_WF	1.8 ~ 3.3 V	TBD ~ 3.3 V	Same as the TCC72x but the lower limit below 1.8V will be determined later.
VDDA_PLL	2.5 V	TBD ~ 1.8 V	Lower than the TCC72x.
VDDA_ADC	2.5 V	TBD ~ 3.3 V	It has higher condition than the TCC72x.

Note: Lower limits for the voltage range under 1.8V are to be determined.

The following tables list the pins changed from the TCC72x. The other power/ground pins not listed in the tables may have different voltage ranges from the TCC72x. Refer to Table 25.2 for those power pins.

Table 25.3 Pin Comparison – TCC760

Pin #	TCC720	TCC760	Description
71	VDDI	VDD_OSC	Dedicated 1.8V power for crystal oscillator I/O (XIN/XOUT and XTIN/XTOUT)
87	VDDI_aip	VDDI_ADC	ADC core power. (1.8V)
88	VSSI_aip	VSSI_ADC	ADC core ground.
89	VDDA_cdc	PKG1	Package ID1. PKG1 must be tied to VDD.
90	LCH_OUT	GPIO_D15	
91	RCH_OUT	GPIO_D16	
92	RCH_IN	GPIO_D17	
93	MIC_IN	GPIO_D18	Internal pull-up enabled at reset.
94	LCH_IN	GPIO_D19	Internal pull-up enabled at reset.
95	VREF_cdc	GPIO_D20	Internal pull-up enabled at reset.
96	VSSA_cdc	GPIO_D21	Internal pull-up enabled at reset.

Table 25.4 Pin Comparison – TCC761

Pin #	TCC721	TCC761	Description
116	VDDI	VDD_OSC	Dedicated 1.8V power for crystal oscillator I/O (XIN/XOUT and XTIN/XTOUT)
146	VDDI_aip	VDDI_ADC	ADC core power. (1.8V)
147	VSSI_aip	VSSI_ADC	ADC core ground.
148	VSSI_aip	PKG0	Package ID0. PKG0 must be tied to VSS.
149	VDDA_cdc	PKG1	Package ID1. PKG1 must be tied to VDD.
150	LCH_OUT	GPIO_D15	
151	RCH_OUT	GPIO_D16	
152	RCH_IN	GPIO_D17	
153	MIC_IN	GPIO_D18	Internal pull-up enabled at reset.
154	LCH_IN	GPIO_D19	Internal pull-up enabled at reset.
155	VREF_cdc	GPIO_D20	Internal pull-up enabled at reset.
156	VSSA_cdc	GPIO_D21	Internal pull-up enabled at reset.

Table 25.5 Pin Comparison – TCC763/TCC764 Rev. 0

Ball #	TCC723	TCC763/TCC764 Rev. 0	Description
M11	VDDI	VDD_OSC	Dedicated 1.8V power for crystal oscillator I/O (XIN/XOUT and XTIN/XTOUT)
D12	VDDD_aip	VDDI_ADC	ADC core power. (1.8V)
F9	VSSD_aip	VSSI_ADC	ADC core ground.
J7	VSSI	PKG1	Package ID1. PKG1 should be tied to VDD. (“0” may work but not recommended).
A8	ROUT	GPIO_D15	
A9	HPGND	GPIO_D16	
B9	LOUT	GPIO_D17	

Table 25.6 Pin Comparison – TCC763/TCC764 Rev. 1

Ball #	TCC723	TCC763/TCC764 Rev. 1	Description
M11	VDDI	VDD_OSC	Dedicated 1.8V power for crystal oscillator I/O (XIN/XOUT and XTIN/XTOUT)
D12	VDDD_aip	VDDI_ADC	ADC core power. (1.8V)
F9	VSSD_aip	VSSI_ADC	ADC core ground.
J7	VSSI	PKG1	Package ID1. PKG1 should be tied to VDD. (“0” may work but not recommended).
G1	SCLK	GPIO_D15	SCLK is internally connected with GPIO_A[9]
A9	HPGND	GPIO_D16	
G2	SDIN	GPIO_D17	SDIN is internally connected with GPIO_A[8]
D2	CSB	GPIO_D18	Internal pull-up enabled at reset. CSB is internally connected with WMODE.
H12	LRCK	GPIO_D19	Internal pull-up enabled at reset. LRCK is internally connected with GPIO_B[22]

25.3 Differences in I/O Cell Characteristics

- All the digital I/O cells except XIN and XTIN have wide operating voltage range (1.65V ~ 3.6V).
- Programmable output buffer drive strength and pull-up resistors.
- Due to I/O characteristics at low voltage levels (< 1.8V), tolerarant I/O cell was not used in the TCC76x. Input voltage must not exceed VDDIO level.
- Crystal oscillator input pins (XIN, XTIN) are dedicated 1.8V cells. Do not apply voltage over VDD_OSC (Max. 1.95V) for these pins.