

## 1. Features

- Full Trusted Computing Group (TCG) Trusted Platform Module (TPM) Version 1.2 Compatibility
- Single-chip Turnkey Solution
- Hardware Asymmetric Crypto Engine
- 2048-bit RSA<sup>®</sup> Sign in 500 ms
- AVR<sup>®</sup> RISC Microprocessor
- Internal EEPROM Storage for RSA Keys
- 100 kHz System Management Bus (SMBus<sup>™</sup>) Two-wire Interface
- Secure Hardware and Firmware Design and Chip Layout
- True Random Number Generator (RNG) - FIPS 140-2 Compliant
- NV Storage Space for 1280 bytes of user defined data
- 3.3V Supply Voltage
- 28-lead TSSOP Package or 40-lead QFN Package
- 0–70°C Temperature Range

## 2. Description

The AT97SC3203S is a fully integrated security module designed to be integrated into embedded systems. It implements version 1.2 of the Trusted Computing Group (TCG) specification for Trusted Platform Modules (TPM).

The TPM includes a cryptographic accelerator capable of computing a 2048-bit RSA signature in 500 ms and a 1024-bit RSA signature in 100 ms. Performance of the SHA-1 accelerator is 50  $\mu$ s per 64-byte block. In most cases, TCG key generation operations will be completed using a proprietary mechanism in less than 1 msec.



## Trusted Platform Module

## AT97SC3203S

## SMBus Two-Wire Interface

## Summary

Note: See the full datasheet for detailed design information.

5132BS-TPM-1/08

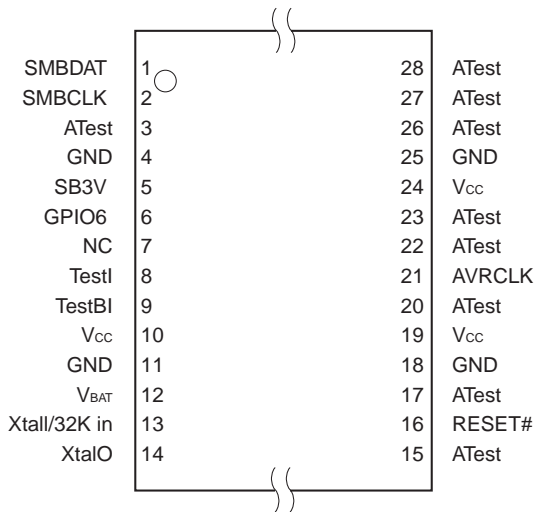


Note: This is a summary document. A complete document is available under NDA. For more information, please contact your local Atmel sales office.

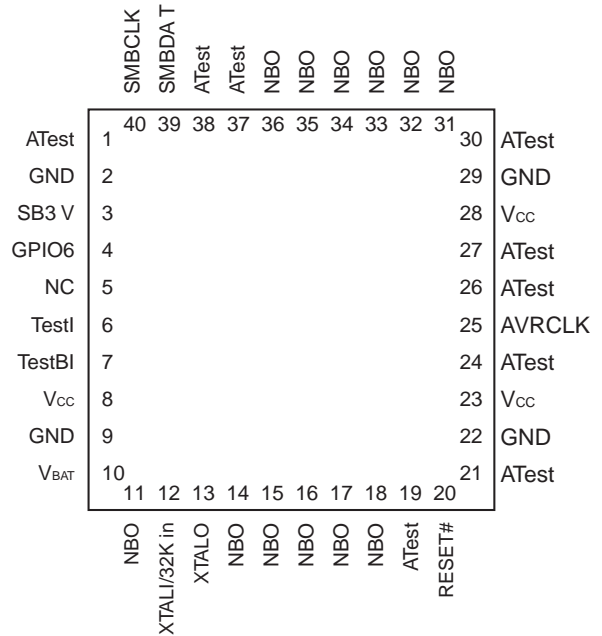
**Figure 2-1.** Pin Configurations

Pin Name	Description
V <sub>CC</sub>	3.3V Supply Voltage
SB3V	Standby 3.3V Supply Voltage
V <sub>BAT</sub>	2.5–4.0V Battery Input
GND	Ground
RESET#	Reset Input Active Low
SMBDAT	SMBus Data Input/Output
SMBCLK	SMBus Clock Input
AVRCLK	33-MHz AVR Clock Input
Xtall/32K in	32.768 kHz Crystal Input
XtalO	32.768 kHz Crystal Output
GPIO6	General Purpose Input/Output
TestI	Test Input (disabled)
TestBI	Test Input (disabled)
ATest	Atmel Test Pin
NC	No Connect
NBO	Not Bonded Out

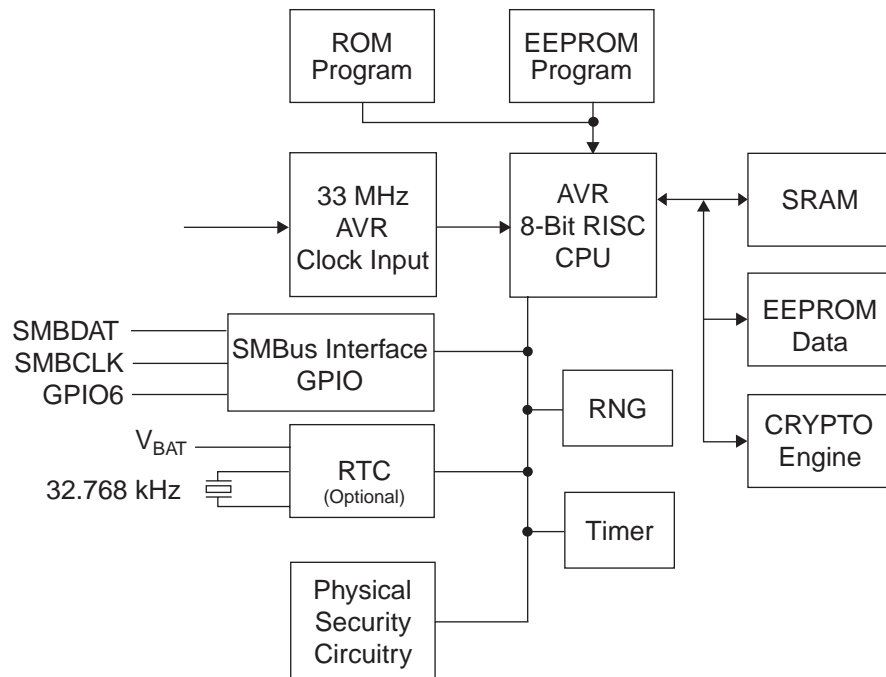
28-pin TSSOP  
6.1 mm x 9.7 mm Body  
0.65 mm Pitch



40-pin QFN  
6.0 mm x 6.0 mm Body  
0.50 mm Pitch



**Figure 2-2.** AT97SC3203S Block Diagram



## 2. Description (continued)

Communication to and from the TPM occurs through a modified 100-kHz SMBus two-wire interface. The TPM includes a hardware random number generator, including a FIPS-approved Pseudo Random Number Generator, that is used for key generation and TCG protocol functions. The RNG is also available to the system to generate random numbers that may be needed during normal operation.

The chip uses a dynamic internal memory management scheme to store multiple RSA keys. Other than the standard TCG commands (TPM\_FlushSpecific, TPM\_Loadkey2), no system intervention is required to manage this internal key cache.

Full documentation for TCG primitives can be found on the TCG Web site located at [www.trustedcomputinggroup.org](http://www.trustedcomputinggroup.org). This specification includes only mechanical, electrical and SMBus protocol information.

### 3. Ordering Information

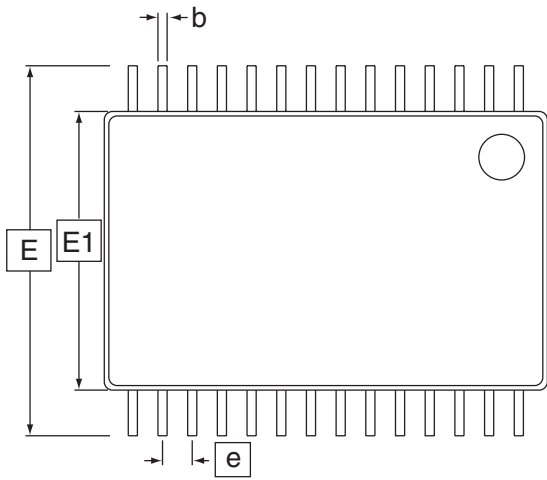
**Table 3-1.** Ordering Information

Ordering Code	Package		Operation Range
AT97SC3203S <sup>(1)</sup>	28A3 (28-pin TSSOP)	Lead-free, RoHS	Commercial (0° to 70° C)
AT97SC3203S <sup>(1)</sup>	40ML1 (40-pin QFN)	Lead-free, RoHS	Commercial (0° to 70° C)

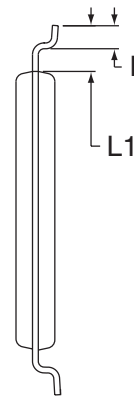
Note: 1. Please see the AT97SC3203S datasheet addendum for the complete catalog number ordering code.

4. Package Drawing

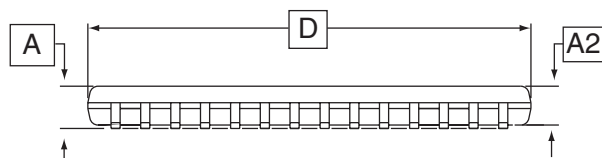
28A3 – TSSOP



Top View



End View



Side View

COMMON DIMENSIONS  
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
D	9.60	9.70	9.80	2, 5
E	8.10 BSC			
E1	6.00	6.10	6.20	3, 5
A	-	-	1.20	
A2	0.80	1.00	1.05	
b	0.19	-	0.30	4
e	0.65 BSC			
L	0.45	0.60	0.75	
L1	1.00 REF			

- Notes:
1. This drawing is for general information only. Please refer to JEDEC Drawing MO-153, Variation DB for additional information.
  2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15 mm (0.006 in) per side.
  3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25 mm (0.010 in) per side.
  4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07 mm.
  5. Dimension D and E1 to be determined at Datum Plane H.

1/8/02



2325 Orchard Parkway  
San Jose, CA 95131

TITLE

28A3, 28-lead, 6.1 x 9.7 mm Body, 0.65 pitch,  
Thin Shrink Small Outline Package (TSSOP)

DRAWING NO.

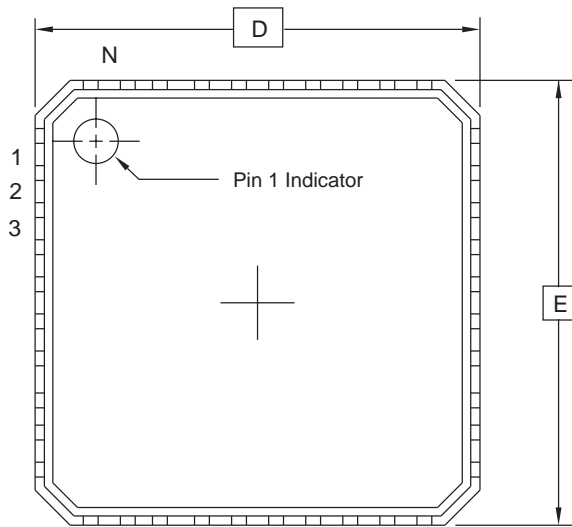
28A3

REV.

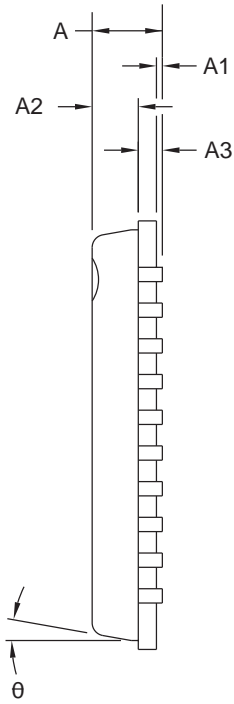
A



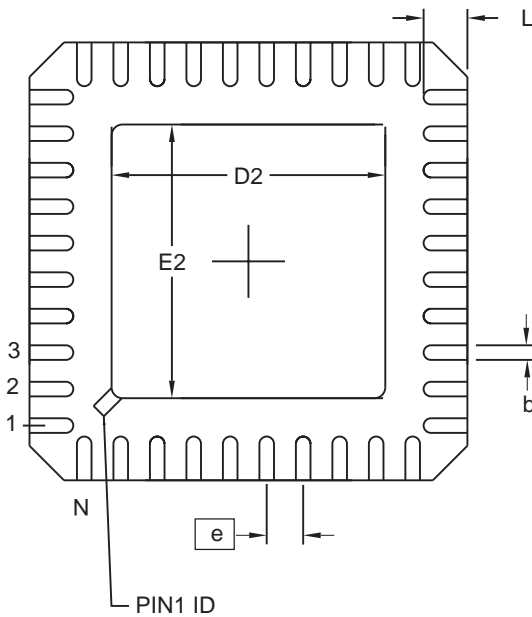
# 40ML1 - QFN



Top View



Side View



Bottom View

**COMMON DIMENSIONS**  
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
D	6.00 BSC			
E	6.00 BSC			
D2	3.95	4.10	4.25	
E2	3.95	4.10	4.25	
A	-	0.85	0.90	
A1	0.0	0.01	0.05	
A2	-	0.65	0.70	
A3	0.20 REF			
L	0.30	0.40	0.50	
e	0.50 BSC			
b	0.18	0.23	0.30	2

- Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-220, Variation WJJD-2, for proper dimensions, tolerances, datums, etc.
  2. Dimension b applies to metallized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension should not be measured in that radius area.

9/27/07



2325 Orchard Parkway  
San Jose, CA 95131

**TITLE**

**40ML1**, 40-lead 6.0 x 6.0 mm Body, 0.50 mm Pitch, Molded Quad Flat No Lead Package (QFN) Punched

**DRAWING NO.**

40ML1

**REV.**

C

**Revision History**

<b>Doc. Rev.</b>	<b>Date</b>	<b>Comments</b>
5132BS	1/2008	Implemented revision history.



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