

Fully Integrated Ku-band HBT VCO

Low cost / High linearity

GaAs Monolithic Microwave IC

Description

The CHV2270 is a multifunction for frequency generation. It integrates a C-band balanced voltage controlled oscillator providing a Ku-band output (2nd harmonic), with different modulation slopes control and other functions like linearity improvement device making it suitable for radar modulations. It also includes a dual rank prescaler, an adjustable medium power amplifier and a temperature sensor.

The VCO is fully integrated on HBT process. On chip base-collector diodes are used as varactors. All the active devices are internally self biased to ease bias configuration. This chip is compatible with automatic equipment for assembly.

The circuit is manufactured on HBT process 2µm emitter length, via holes through the substrate and high Q passive elements. It is available in chip form.

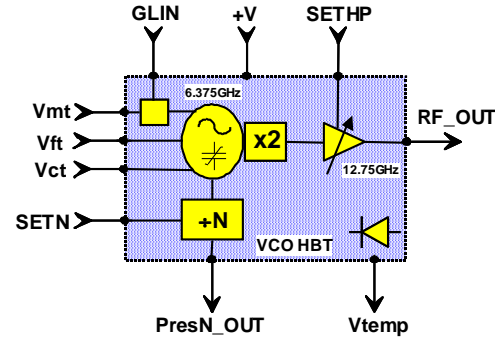
Main Features

- -40°C to +125°C temperature range
- Low temperature dependence
- Fully integrated VCO architecture
- Prescaler by up to F_{out}/128
- Low phase noise
- Low cost / high linearity oriented
- Adjustable output power
- Temperature sensor
- Very simple bias configuration
- Low DC power consumption
- Automatic assembly oriented
- SiNx layer protection
- Chip size: 1.38 x 2.05 x 0.1mm

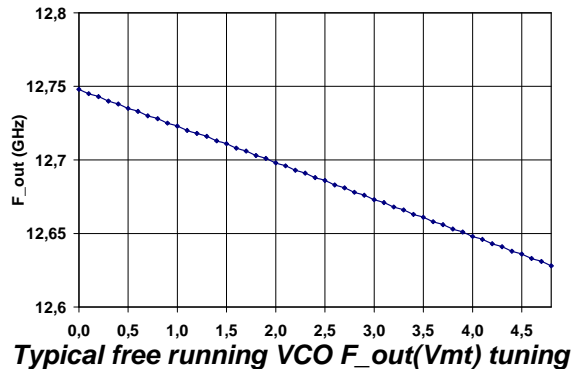
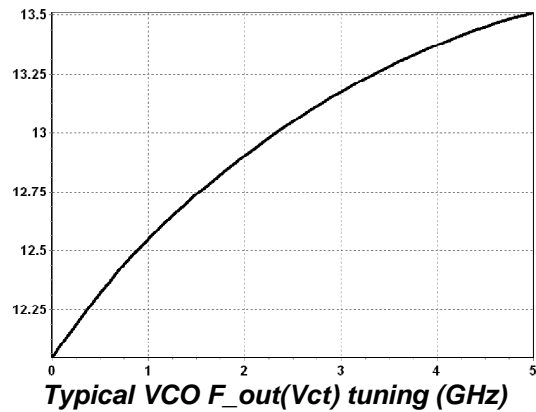
Main Characteristics

T_{amb} = +25°C

Symbol	Parameter	Min	Typ	Max	Unit
F _{out}	Specified output frequency range	12.65	12.75	12.85	GHz
PN	Phase noise @ F _{out} and 100kHz offset		-100		dBc/Hz
P _{out}	Output power		5 or 14		dBm



VCO multifunction block diagram



Electrical Characteristics

Full temperature range

Symbol	Parameter (1)	Min	Typ	Max	Unit
F_out	RF_OUT frequency for guaranteed specifications	12.65	12.75	12.85	GHz
P_out	Output power at RF_OUT port on load VSWR ≤ 1.5:1 (2)	1	5 (2)	8	dBm
VSWR_out	RF_OUT port VSWR on 50Ω load		1.5:1	2.5:1	
P_out_Lin	P_out linearity over 200MHz within F_out range		0.75		dBpp
ΔF_tune(T)	Maximum variation of F_out over temperature		250	500	MHz
Vct_F_tune	Coarse tuning total frequency range	0.5	2		GHz
Vft_F_tune	Fine tuning frequency range with guaranteed specifications	3			MHz
Vmt_F_tune	Medium tuning frequency range with guaranteed specifications		70		MHz
Vct_V_tune	Coarse tuning voltage range	0.5 - 4.3	0.5 – 4.5		V
Vft_V_tune	Fine tuning voltage range	2 - 4	0 – 4.5		V
Vmt_V_tune	Medium tuning voltage range		0 – 4.5		V
Vct_I	Coarse tuning port current			0.5	mA
Vft_I	Fine tuning port current			0.5	mA
Vmt_I	Medium tuning port current		1.5	3	mA
Vct_F_slope	Coarse tuning frequency slope	200	375	700	MHz/V
Vft_F_slope	Fine tuning frequency slope within Vft_F_tune (3)	-10	-5	-2.5	MHz/V
ΔVft_F_slope(T)	Maximum variation of Vft_F_slope over Top range [+30°C;+110°C] (3)	0		+/-10	%
Vmt_F_slope	Medium tuning frequency slope within Vmt_F_tune	-40	-20	-10	MHz/V
ΔVmt_F_slope(T)	Maximum variation of Vmt_F_slope over Top range [+30°C;+110°C] (4)	0		-20	%
Vft_Lin	Fine tuning linearity over 200kHz within Vft_F_tune (3)	-5	<0.05	+5	%
Vmt_Lin1	Medium tuning linearity over 33MHz within Vmt_F_tune (3)		+/-1 (3)		%
Vmt_Lin2	Medium tuning frequency range with +/-1% linearity within Vmt_F_tune		33		MHz
Vft_Mod3dB	Fine tuning modulation 3dB cutoff frequency within Vft_F_tune @ d(Vct_V)/dt=0	5			MHz
Vmt_Mod3dB	Medium tuning modulation 3dB cutoff frequency within Vmt_F_tune @ d(Vct_V)/dt=0	10	20		MHz
P_VSWR	Frequency pulling versus RF_OUT port load @ VSWR = 2.5:1 (2)		0.25		MHz pp
P_V+	Frequency pushing versus supply voltage	0	35	70	MHz/V
PN	F_out Phase noise @ 10kHz @ 100kHz @ 1MHz		-75 -100 -123	-65 -90 -113	dBc/Hz
AN	Amplitude noise (SSB) @ 10kHz @ 100kHz @ 1MHz		-145 -156 -167	-135 -146 -157	dBc

Hn_Rej	RF_OUT VCO harmonics rejection	10	20		dBc
Pres_Rej	RF_OUT prescaler spurious rejection	45	65		dBc
Pres_N	Prescaler rank		N=4 or 64		
Pres_F	Prescaler PRESN ports output frequency	F_out/(2*Pres_N)			GHz
Pres_P	Output power on PRESN ports	-3	0		dBm
Pres_L	PRESN ports load		100		Ω
Pres64_PN	Prescaler rank 64 phase noise: @ 10kHz @ 100kHz @ 1MHz		-117 -142 -165	-107 -130 -150	dBc/Hz
Vtemp_V	Temperature sensor port voltage @ +25°C	1.15	1.35	1.55	V
Vtemp_S	Temperature sensor port voltage slope over Top	-1.2	-1	-0.8	mV/°C
Vtemp_L	Temperature sensor port load	47k			Ω
+V	Positive supply voltage (Pads (VD1 xor VD2) and (VA1 xor VA2))	+4.4	+4.5	+4.6	V
+I	Positive supply current (Pads (VD1 xor VD2) and (VA1 xor VA2)) (2&5)		150	210	mA
Top	Operating temperature range	-40	25	+125	°C
Symbol	Parameter (1)	Min	Typ	Max	Unit

- (1) **IMPORTANT:** Fine and medium tuning port must not be used together.
Fine or medium tuning port specifications are guaranteed when respectively medium or fine tuning port is high impedance.
- (2) In low power mode. See "VCO setting matrix" for 14dBm P_out (+I increase < 80mA in high power mode).
- (3) Pad "GLIN" set to "open".
- (4) Pad "GLIN" set to "GND".
- (5) SET4 set to "GND" and SET64 set to "OPEN" (+I increase < 20mA when N=64).

Absolute Maximum Ratings (1)

Symbol	Parameter	Values	Unit
+V	Positive supply ports voltage	+5	V
VTx	Tuning ports voltage	0 to +5	V
+I	Positive supply current (N=4 & low power)	250	mA
Tstg	Storage temperature range	-55 to +150	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

CAUTION:

ESD Protections: Electrostatic discharge sensitive device, observe handling and assembly precautions !



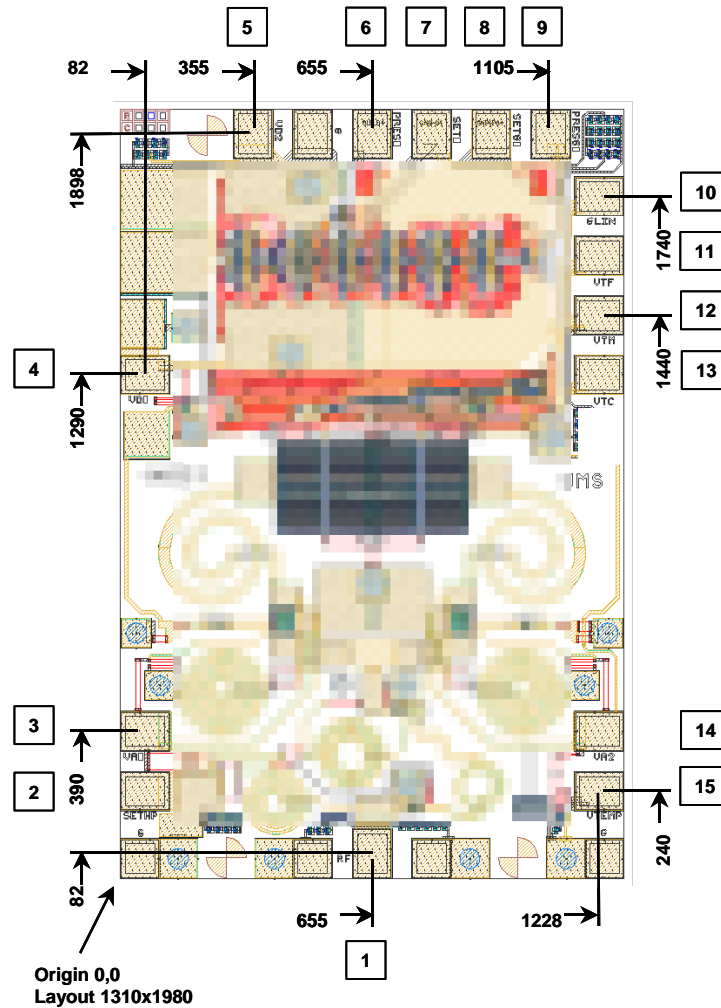
VCO Setting Matrix

Sufficient conditions

Symbol	Parameter	Setting Pad	Setting	Typical Value
P_out	Output power at RF_OUT port on load VSWR ≤1.5:1	SETHP	Open	5 dBm
			V0 to +V	5 to 14 dBm
			+V	14 dBm
Pres4_P	Output power on PRES4 port	SET4	DC GND (2)	0 dBm
		SET64	Open	
		SET4	Open	Non Active
Pres64_P	Output power on PRES64 port	SET64	DC GND (2)	0 dBm
		SET4	Open	
		SET64	Open	Non Active
Vmt_Lin1	Medium tuning linearity over 33MHz within Vmt_F_tune	GLIN	Open	+/-1%
			DC GND	+/-0.33%

(2) See “Typical Assembly and Bias Configuration” for recommendations.

Chip Mechanical Data and Pin References



Unit = μm

External chip size (layout size + dicing streets) = 1380 x 2050 \pm 35

Chip thickness = 100 \pm 10

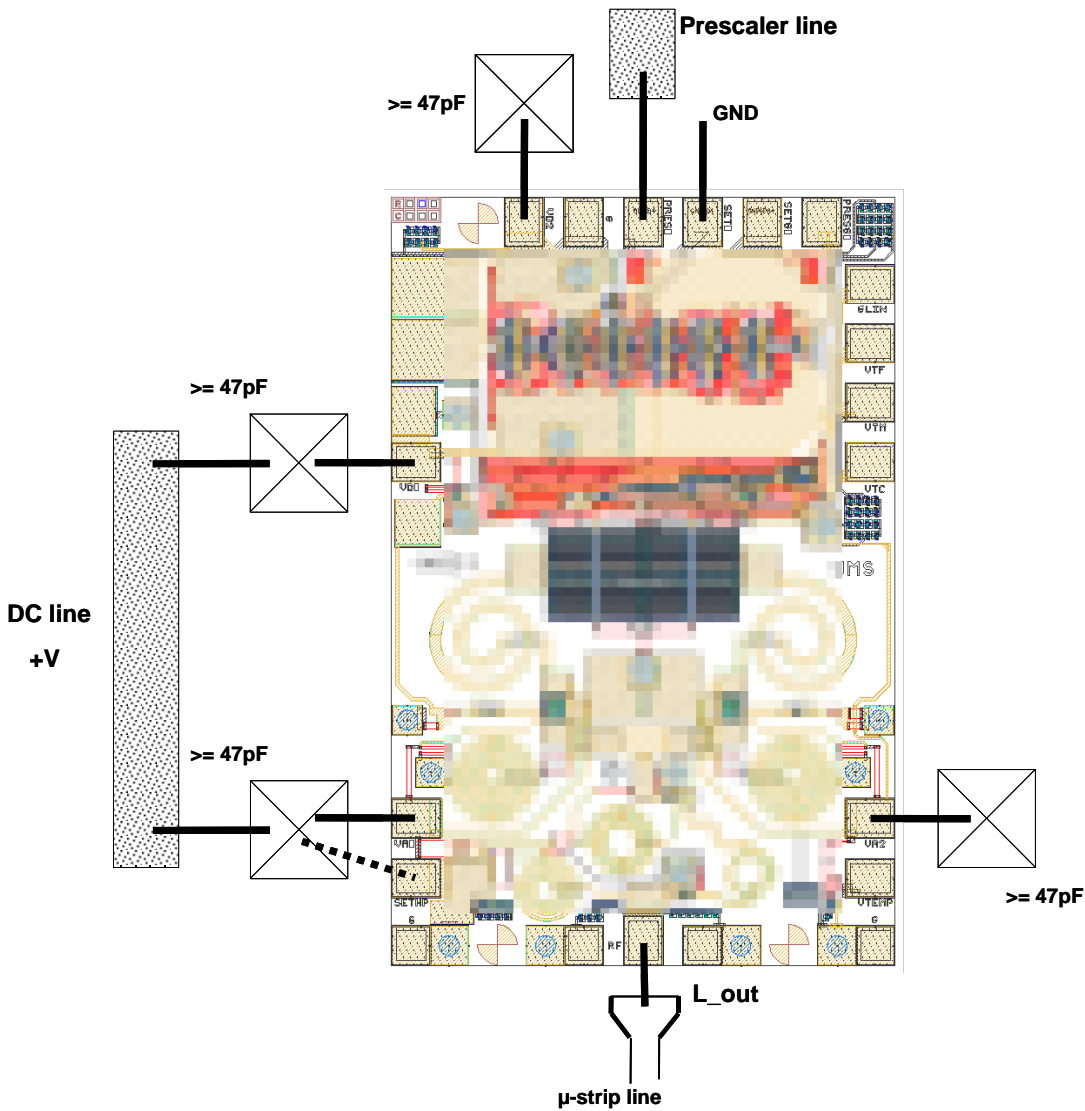
RF Pads (1, 5) = 75 x 100 (SiNx opening larger in the bonding axis)

DC/IF Pads = 75 x 100 (SiNx opening larger in the bonding axis)

SiNx layer protection thickness = 0.2

Pin number	Pin name	Description
1	RF	RF output port
2	SETHP	RF power option setting port
3	VA1	Positive supply voltage port (intra-connected to VA2)
4	VD1	Positive supply voltage port (intra-connected to VD2)
5	VD2	Positive supply voltage port (intra-connected to VD1)
6	PRES4	Prescaler rank 4 output port
7	SET4	Prescaler rank 4 option setting port
8	SET64	Prescaler rank 64 option setting port
9	PRES64	Prescaler rank 64 output port
10	GLIN	VTM linearity option setting port
11	VTF	RF Frequency fine tuning port
12	VTM	RF Frequency medium tuning port
13	VTC	RF Frequency coarse tuning port
14	VA2	Positive supply voltage port (intra-connected to VA1)
15	VTEMP	Temperature sensor output port

Typical Assembly and Bias Configuration



This drawing shows an example of assembly and bias configuration. All the transistors are internally self-biased. Some external chip capacitors of at least 47pF are necessary for the positive supply voltage. Pads to be power supplied are (VD1 xor VD2) and (VA1 xor VA2).

Prescaler outputs PRES4 and PRES64 must be AC coupled through an external serial capacitor taking into account output frequency and internal impedance of 100Ω (Typically >120pF).

SET4 and SET64 longer bonding length to DC ground than 10mm must be compensated by intermediate decoupling capacitor (Typically >120pF). Setting is done by DC load only.

For the RF pad the equivalent wire bonding inductance (diameter=25μm) have to be according to the following recommendation:

Pin name	Equivalent inductance	Wire length (1)
RF	$L_{out} < 0.3 \text{ nH}$	< 0.4 mm

(1) This value is the total length including the necessary loop from pad to pad.

☞ Chip backside must be RF grounded.

Ordering Information

Chip form : CHV2270-98F/00

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