Filtronic

FPD1050SOT89

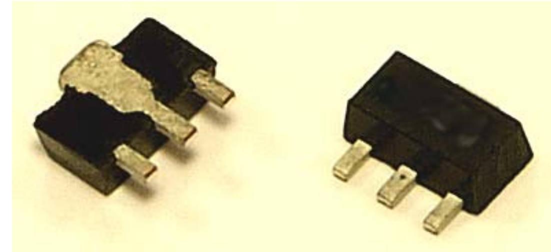
Datasheet v3.0

LOW NOISE HIGH LINEARITY PACKAGED PHEMT

FEATURES (1.8GHZ):

- 26 dBm Output Power (P1dB)
- 17.5 dB Small-Signal Gain (SSG)
- 1.1 dB Noise Figure
- 40 dBm Output IP3
- 50% Power-Added Efficiency
- FPD1050SOT89E: RoHS compliant (Directive 2002/95/EC)

PACKAGE:



GENERAL DESCRIPTION:

The FPD1050SOT89 is a packaged depletion mode AlGaAs/InGaAs pseudomorphic High Electron Mobility Transistor (pHEMT). It utilizes a 0.25 µm x 1050 µm Schottky barrier Gate, defined by high-resolution stepper-based photolithography. The recessed and offset Gate structure minimizes parasitics to optimize performance, with an epitaxial structure designed for improved linearity over a range of bias conditions and i/p power levels.

TYPICAL APPLICATIONS:

- Drivers or output stages in PCS/Cellular base station transmitter amplifiers
- High intercept-point LNAs
- WLL and WLAN systems, and other types of wireless infrastructure systems.

ELECTRICAL SPECIFICATIONS:

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power at 1dB Gain Compression	P1dB	VDS = 5 V; IDS = 50% IDSS	24.5	26		dBm
Small-Signal Gain	SSG	VDS = 5 V; IDS = 50% IDSS	16	17.5		dB
Power-Added Efficiency	PAE	VDS = 5 V; IDS = 50% IDSS; POUT = P1dB		50		%
Noise Figure	NF	VDS = 5 V; IDS = 50% IDSS VDS = 5 V; IDS = 25% IDSS		0.9	1.1	dB
Output Third-Order Intercept Point (from 15 to 5 dB below P1dB)	IP3	VDS = 5V; IDS = 50% IDSS Matched for optimal power Matched for best IP3	37	39 40		dBm
Saturated Drain-Source Current	IDSS	VDS = 1.3 V; VGS = 0 V	260	320	385	mA
Maximum Drain-Source Current	IMAX	VDS = 1.3 V; VGS ≅ +1 V		520		mA
Transconductance	GM	VDS = 1.3 V; VGS = 0 V		270		mS
Gate-Source Leakage Current	IGSO	VGS = -5 V		1	15	µA
Pinch-Off Voltage	|VP|	VDS = 1.3 V; IDS = 1.05 mA	0.7	1.0	1.3	V
Gate-Source Breakdown Voltage	|VBDGS|	IGS = 1.05 mA	12	16		V
Gate-Drain Breakdown Voltage	|VBDGD|	IGD = 1.05 mA	12	16		V
Thermal Resistance	RθJC			76		°C/W

Note: $T_{AMBIENT}$ = 22°; RF specification measured at f = 1850 MHz using CW signal (except as noted)

Specifications subject to change without notice
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ABSOLUTE MAXIMUM RATING[1]:

PARAMETER	SYMBOL	TEST CONDITIONS	ABSOLUTE MAXIMUM
Drain-Source Voltage	VDS	-3V < VGS < +0V	8V
Gate-Source Voltage	VGS	0V < VDS < +8V	-3V
Drain-Source Current	IDS	For VDS > 2V	IDss
Gate Current	IG	Forward or reverse current	10mA
RF Input Power[2]	PIN	Under any acceptable bias state	260mW
Channel Operating Temperature	TCH	Under any acceptable bias state	175°C
Storage Temperature	TSTG	Non-Operating Storage	-40°C to 150°C
Total Power Dissipation	PTOT	See De-Rating Note below	2.0W
Gain Compression	Comp.	Under any bias conditions	5dB
Simultaneous Combination of Limits[3]		2 or more Max. Limits	

Notes:
[1]$T_{Ambient}$ = 22°C unless otherwise noted; exceeding any one of these absolute maximum ratings may cause permanent damage to the device
[2]Max. RF Input Limit must be further limited if input VSWR > 2.5:1
[3]Users should avoid exceeding 80% of 2 or more Limits simultaneously
[4]Total Power Dissipation defined as: $P_{TOT} \equiv (P_{DC} + P_{IN}) - P_{OUT}$,
where P_{DC}: DC Bias Power, P_{IN}: RF Input Power, P_{OUT}: RF Output Power
Total Power Dissipation to be de-rated as follows above 22°C:
P_{TOT}= 2.0 - (0.013W/°C) x T_{PACK}
where T_{PACK}= source tab lead temperature above 22°C
(coefficient of de-rating formula is the Thermal Conductivity)
Example: For a 65°C carrier temperature: P_{TOT} = 2.0W – (0.013 x (65 – 22)) = 1.44W

BIASING GUIDELINES:

- Active bias circuits provide good performance stabilization over variations of operating temperature, but require a larger number of components compared to self-bias or dual-biased. Such circuits should include provisions to ensure that Gate bias is applied before Drain bias, otherwise the pHEMT may be induced to self-oscillate
- Dual-bias circuits are relatively simple to implement, but will require a regulated negative voltage supply for depletion-mode devices.
- Self-biased circuits employ an RF-bypassed Source resistor to provide the negative Gate-Source bias voltage, and such circuits provide some temperature stabilization for the device. A nominal value for circuit development is 3.6 Ω for a 50% of I_{DSS} operating point.
- For standard Class A operation, a 50% of IDSS bias point is recommended. A small amount of RF gain expansion prior to the onset of compression is normal for this operating point. Note that pHEMTs, since they are “quasi- E/D mode” devices, exhibit Class AB traits when operated at 50% of IDSS. To achieve a larger separation between P1dB and IP3, an operating point in the 25% to 33% of IDSS range is suggested. Such Class AB operation will not degrade the IP3 performance.

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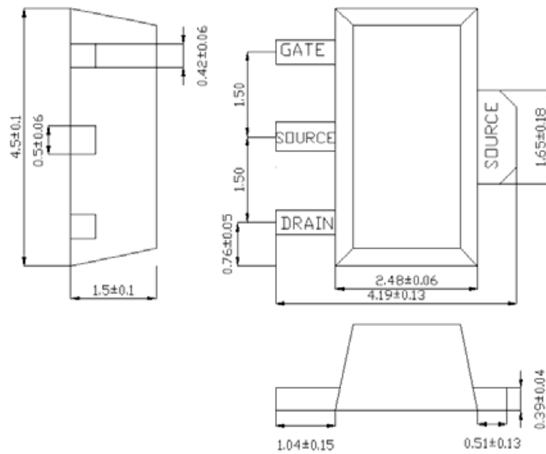
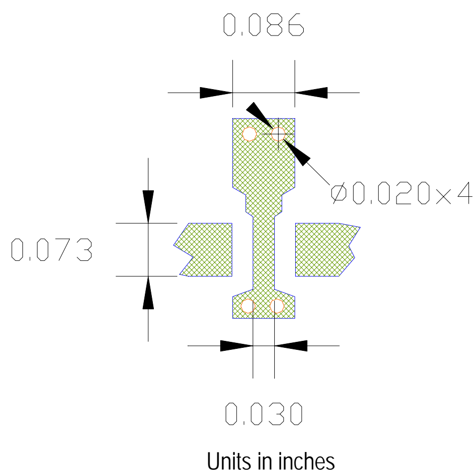
Package Outline:

(dimensions in millimeters – mm)





NOTE: Drawing available on request

Preferred Assembly Instructions:

Available on request.

Handling Precautions:

To avoid damage to the devices care should be exercised during handling. Proper Electrostatic Discharge (ESD) precautions should be observed at all stages of storage, handling, assembly, and testing. These devices should be treated as Class (0-250 V) as defined in JEDEC Standard No. 22-A114. Further information on ESD control measures can be found in MIL-STD-1686 and MIL-HDBK-263.

Application Notes & Design Data:

Application Notes and design data including S-parameters are available on request.

Disclaimers:

This product is not designed for use in any space based or life sustaining/supporting equipment.

Ordering Information:

Part Number	Description
FPD1050SOT89	Packaged pHEMT
FPD1050SOT89E	RoHS compliant Packaged pHEMT

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