Ordering number : ENA0432A

SANYO Semiconductors
DATA SHEET

LC87F06J2A — CMOS IC FROM 192K byte, RAM 8192 byte on-chip 8-bit 1-chip Microcontroller

Overview

The SANYO LC87F06J2A is an 8-bit microcomputer that, centered around a CPU running at a minimum bus cycle time of 66.6ns, integrate on a single chip a number of hardware features such as 192K-byte flash ROM (onboard rewritable), 8K-byte RAM, Onchip debugging function, two sophisticated 16-bit timers/counters (may be divided into 8-bit timers), a 16-bit timer with a prescaler (may be divided into 8-bit timers), four 8-bit timers with a prescaler, a base timer serving as a time-of-day clock, two synchronous SIO ports (with automatic block transmission/reception capabilities), an asynchronous/synchronous SIO port, two synchronous SIO ports, two UART ports (full duplex), four 12-bit PWM channels, VPS/PDC/PAL-WSS • XDS • EPG-J • VBID(Video-ID) Data-slicer, an universal remote control transmitter, an 8-bit 16-channel AD converter, a high-speed clock counter, a system clock frequency divider, and a 36-source 10-vector interrupt, ROM correction function feature.

Features

■Flash ROM
- Single 5V power supply, on-board writeable
- Block erase in 128 byte units
- 196608 × 8 bits (LC87F06J2A)

■RAM
- 8192 × 9 bits

■Bus Cycle Time
- 66.6ns (15MHz, 1/1 frequency division ratio)

Note: Bus cycle time indicates the speed to read ROM.

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■Minimum Instruction Cycle Time (tCYC)
- 200ns (15MHz, 1/1 frequency division ratio)

■Ports
- Normal withstand voltage I/O ports
  Ports whose I/O direction can be designated in 1 bit units: 75 (P1n, P2n, P3n, P70 to P73, P8n, PAn, PB0 to PB2, PCn, S2Pn, XT2, PWM0, PWM1, PEn, PFn)
  Ports whose I/O direction can be designated in 4 bit units: 8 (P0n)
- Normal withstand voltage input ports: 1 (XT1)
- Dedicated oscillator ports: 2 (CF1, CF2)
- Reset pin: 1 ($\overline{\text{RES}}$)
- Data slicer pins: 2 (PB4, PB6)
- Power pins: 11 ($V_{SS}1$ to $V_{SS}4$, $V_{DD}1$ to $V_{DD}4$, V_{SS}VCO, V_{DD}VCO, V_{DD}ODA)

■Timer
- Timer 0: 16-bit timer/counter with capture register
  Mode 0: 8-bit timer with an 8-bit programmable prescaler (with two 8-bit capture registers) × 2 channels
  Mode 1: 8-bit timer with an 8-bit programmable prescaler (with two 8-bit capture registers) + 8-bit counter (with two 8-bit capture registers)
  Mode 2: 16-bit timer with an 8-bit programmable prescaler (with two 16-bit capture registers)
  Mode 3: 16-bit counter (with two 16-bit capture registers)
- Timer 1: 16-bit timer/counter that support PWM/ toggle output
  Mode 0: 8-bit timer with an 8-bit prescaler (with toggle outputs) + 8-bit timer/counter (with toggle outputs)
  Mode 1: 8-bit PWM with an 8-bit prescaler × 2 channels
  Mode 2: 16-bit timer/counter with an 8-bit prescaler (with toggle outputs) (toggle outputs also from the lower-order 8 bits)
  Mode 3: 16-bit timer with an 8-bit prescaler (with toggle outputs) (The lower-order 8 bits can be used as PWM.)
- Timer 4: 8-bit timer with a 6-bit prescaler
- Timer 5: 8-bit timer with a 6-bit prescaler
- Timer 6: 8-bit timer with a 6-bit prescaler (with toggle outputs)
- Timer 7: 8-bit timer with a 6-bit prescaler (with toggle outputs)
- Timer 8: 16-bit timer with a prescaler (may be divided into 8-bit timers)
- Base timer
  1) The clock is selectable from the subclock (32.768kHz crystal oscillator), system clock, and timer 0 prescaler output.
  2) Interrupts programmable in 5 different time schemes.

■Day and Time Counter
1) Using with a base timer, it can be used as 65,000 days + minute + second counter.

■High-speed Clock Counter
1) Can count clocks with a maximum clock rate of 20MHz (at a main clock of 10MHz).
2) Can generate output real time.

■SIO
- SIO 0: 8 bit synchronous serial interface
  1) LSB first/MSB first mode selectable
  2) Built-in 8-bit baudrate generator (maximum transfer clock cycle = 4/3 tCYC)
  3) Automatic continuous data transmission (1 to 256 bits)
- SIO 1: 8 bit asynchronous/synchronous serial interface
  Mode 0: Synchronous 8-bit serial I/O (2- or 3-wire configuration, 2 to 512 tCYC transfer clocks)
  Mode 1: Asynchronous serial I/O (Half-duplex, 8 data bits, 1 stop bit, 8 to 2048 tCYC baudrates)
  Mode 2: Bus mode 1 (start bit, 8 data bits, 2 to 512 tCYC transfer clocks)
  Mode 3: Bus mode 2 (start detect, 8 data bits, stop detect)

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- SIO2: 8 bit synchronous serial interface
  1) LSB first mode
  2) Built-in 8-bit baudrate generator (maximum transfer clock cycle = 4/3 tCYC)
  3) Automatic continuous data transmission (1 to 32 bytes)
- SIO 7: 8 bit synchronous serial interface
  1) LSB first/MSB first mode selectable
  2) Built-in 8-bit baudrate generator (maximum transfer clock cycle = 4/3 tCYC)
- SIO 8: 8 bit synchronous serial interface
  1) LSB first/MSB first mode selectable
  2) Built-in 8-bit baudrate generator (maximum transfer clock cycle = 4/3 tCYC)

■UART: 2 channels
1) Full duplex
2) 7/8/9 bit data bits selectable
3) 1 stop bit (2 bits in continuous transmission mode)
4) Built-in baudrate generator (with baudrates of 16/3 to 8192/3 tCYC)

■AD Converter
- 8 bits × 16 channels

■PWM
- Multifrequency 12-bit PWM × 4 channels

■Remote Control Receiver Circuit (sharing pins with P73, INT3, T0IN and TOHCP)
1) Noise filtering function (noise filter time constant selectable from 1 tCYC, 32 tCYC, and 128 tCYC)
2) The noise filtering function is available for the INT3, T0IN, or T0HCP signal at P73. When P73 is read with an instruction, the signal level at that pin is read regardless of the availability of the noise filtering function.

■Small Signal Detect Function
1) Small Signal Detect Function is available in the following two terminals.
   P20/INT4/T1IN/T0LCP/T0HCP/INT6/T0LCP1/SSGI0
   P24/INT5/T1IN/T0LCP/T0HCP/INT7/T0HCP1/SSGI1
2) Capable of detecting a pulse with certain level of amplitude.
3) Input bias circuit available.

■H-Counter
1) H-counter can choose one of the following signals as count-clock.
   HCTR signal of P22/INT4/T1IN/T0LCP/T0HCP/HCTR terminal
   CSYNC signal of PB6/CVD/CSYNC terminal
   Composite sync signal detected from CVD (composite Video) signal by built-in sync-separator inputted form PB6/CVD/CSYNC terminal
2) Counter 7bit (up) + 1bit (over-flow flag)

■Field (first/second) Detect Function
1) Distinguishes a field with one of the following signals.
   CSYNC signal of PB6/CVD/CSYNC terminal
   Composite sync signal detected from CVD (composite Video) signal by built-in sync-separator inputted form PB6/CVD/CSYNC terminal
2) Outputs Field-Detect signal from PB0/DS1FLD terminal

■Watchdog Timer
1) External RC watchdog timer
2) Interrupt and reset signals selectable

■Data-Slicer
- XDS
  1) Supports XDS-1X and XDS-2X (With auto-recognition)
- VPS/PDC/PAL-WSS
  Data-slicer can choose one of the following three formats to the TV Line(VBI).
  1) PDC/UDT and other Teletext data
  2) VPS
  3) PAL-WSS
- VPS
- EPG-J
- Antiope
- VBID(VideoID)

■Universal Remote Control Transmitter Circuit
- Outputs remote control signal from PF4/IRP terminal.

■Interrupts
- 36 sources, 10 vector addresses
  1) Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control.
     Any interrupt requests of the level equal to or lower than the current interrupt are not accepted.
  2) When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address takes precedence.

No.	Vector	Selectable Level	Interrupt signal
1	00003H	X or L	INT0
2	0000BH	X or L	INT1
3	00013H	H or L	INT2/T0L/INT4
4	0001BH	H or L	INT3/INT5/Base timer0/Base timer1/Remocon transmit
5	00023H	H or L	T0H/INT6/SIO7
6	0002BH	H or L	T1L/T1H/INT7/SIO8
7	00033H	H or L	SIO0/UART1 receive/UART2 receive/T8L/T8H
8	0003BH	H or L	SIO1/SIO2/UART1 transmit/UART2 transmit
9	00043H	H or L	ADC/T6/T7/PWM4, PWM5/ Automatic transmission
10	0004BH	H or L	Port 0/T4/T5/Data slicer /PWM0, PWM1

- Priority Level: X > H > L
- Of interrupts of the same level, the one with the smallest vector address takes precedence.

■Subroutine Stack Levels
- 4096 levels maximum (the stack is allocated in RAM.)

■High-speed Multiplication/Division Instructions
- 16 bits × 8 bits (5 tCYC execution time)
- 24 bits × 16 bits (12 tCYC execution time)
- 16 bits ÷ 8 bits (8 tCYC execution time)
- 24 bits ÷ 16 bits (12 tCYC execution time)

■Oscillation Circuits
- RC oscillator circuit (internal): For system clock
- CF oscillator circuit: For system clock with internal Rf
- Crystal oscillator circuit: For low-speed system clock
- Multifrequency RC oscillator circuit (internal): For system clock

■System Clock Divider Function
- Can run on low current.
- The minimum instruction cycle selectable from 300ns, 600ns, 1.2µs, 2.4µs, 4.8µs, 9.6µs, 19.2µs, 38.4µs, and 76.8µs (at a main clock rate of 10MHz).

■Standby Function
- HALT mode: Halts instruction execution while allowing the peripheral circuits to continue operation.
  1) Oscillation is not halted automatically.
  2) Canceled by system reset or occurrence of interrupt.
- HOLD mode: Suspends instruction execution and the operation of the peripheral circuits.
  1) The CF, RC, and crystal oscillators automatically stop operation.
  2) There are three ways of resetting the HOLD mode.
     (1) Setting the Reset pin to the lower level
     (2) Setting at least one of the INT0, INT1, INT2, INT4, and INT5 pins to the specified level
     (3) Having an interrupt source established at port 0
- X'tal HOLD mode: Suspends instruction execution and the operation of the peripheral circuits except the base timer and the Day-and-time counter.
  1) The CF and RC oscillators automatically stop operation.
  2) The state of crystal oscillation established when the HOLD mode is entered is retained.
  3) There are four ways of resetting the X'tal HOLD mode.
     (1) Setting the Reset pin to the low level.
     (2) Setting at least one of the INT0, INT1, INT2, INT4, and INT5 pins to the specified level.
     (3) Having an interrupt source established at port 0.
     (4) Having an interrupt source established in the base timer circuit.

■Onchip Debugging
- Permits software debugging with the test device installed on the target board.

■ROM Correction Function
- PC match address registers: 4
- Ram for ROM correction: 128byte

■Package Form
- QIP100E(14×20): “Lead-free type”

■Development Tools
- On-chip debugger: TCB87 TypeA + LC87F06J2A
  : TCB87 TypeB + LC87F06J2A

■Flash ROM Programming Boards

Package	Programming boards
QIP100E(14×20)	W87F05256Q

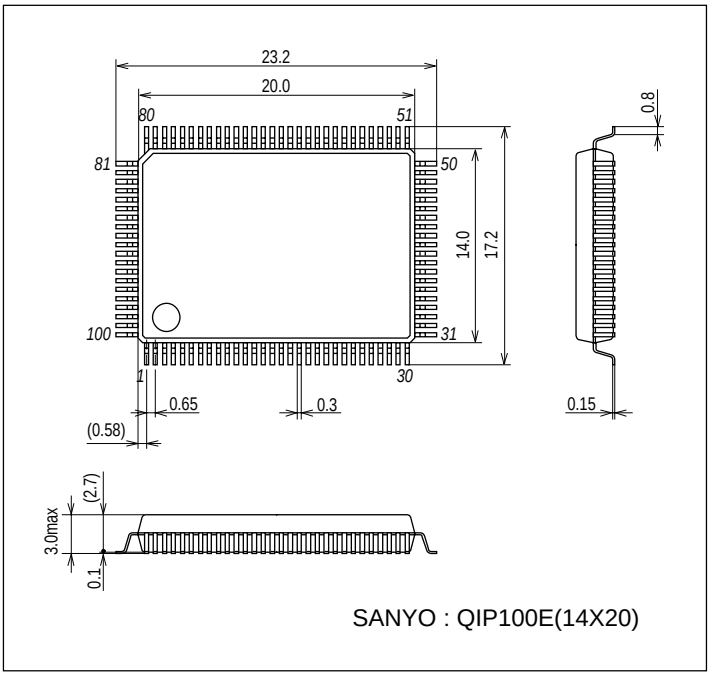
■Flash ROM Programmer

Maker	Model	Supported version	Device
Flash Support Group, Inc. (Single)	AF9708/AF9709/AF9709B (including product of Ando Electric Co.,Ltd)	Revision: After 02.61	LC87F06J2A FAST
Flash Support Group, Inc. (Gang)	AF9723(Main body) (including product of Ando Electric Co.,Ltd)	Revision: After 02.04	LC87F06J2A FAST
	AF9833(Unit) (including product of Ando Electric Co.,Ltd)	Revision: After 01.86	
SANYO	SKK(Sanyo FWS)	Application Version: After 1.03 Chip Data Version: After 2.01	LC87F06J2

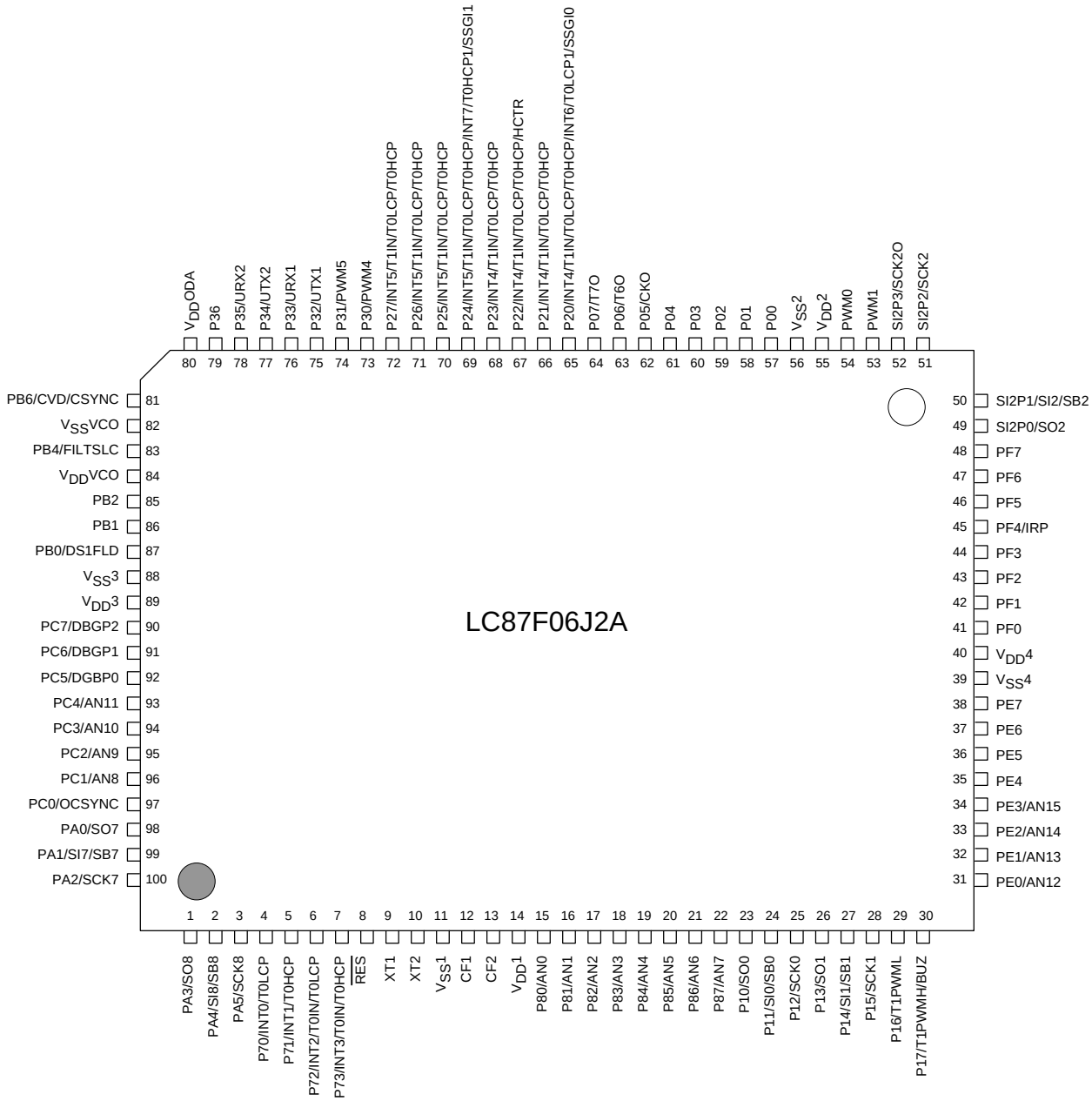
Package Dimensions

unit : mm (typ)

3151A



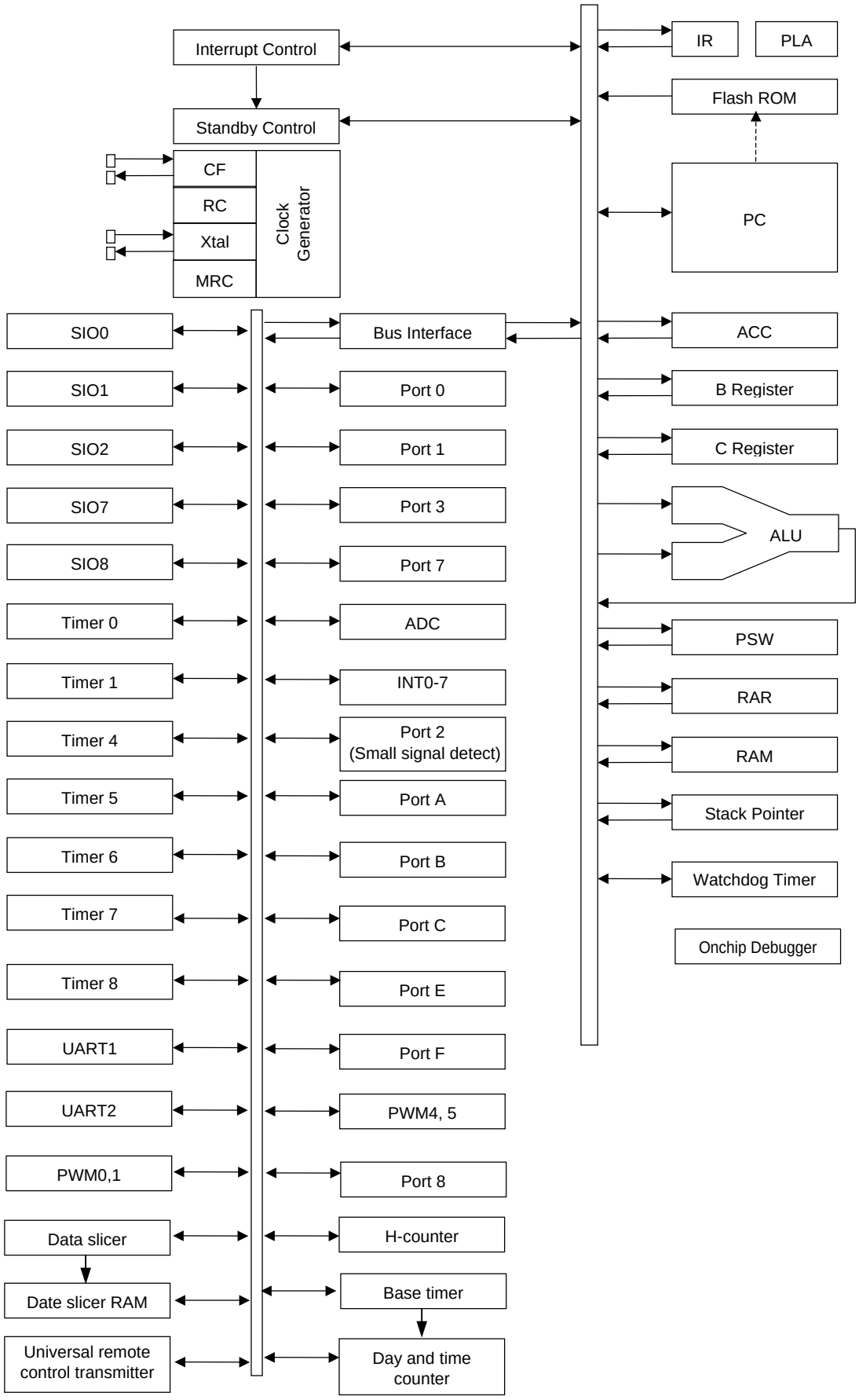
Pin Assignment



Top view

SANYO: QIP100E(14×20) “Lead-free Type”

System Block Diagram



Pin Description

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function description</th><th>Option</th></tr>
<tr><td>$V_{SS}1$, $V_{SS}2$
$V_{SS}3$, $V_{SS}4$
$V_{SS}VCO$</td><td>-</td><td>Power supply pin (-)</td><td>No</td></tr>
<tr><td>$V_{DD}1$, $V_{DD}2$
$V_{DD}3$, $V_{DD}4$
$V_{DD}VCO$,
$V_{DD}ODA$</td><td>-</td><td>Power supply pin (+)</td><td>No</td></tr>
<tr><td>Port 0
P00 to P07</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 4-bit units
• Pull-up resistor can be turned on and off in 4-bit units
• HOLD release input
• Port 0 interrupt input
• Pin functions
P05: System clock output
P06: Timer 6 toggle output
P07: Timer 7 toggle output</td><td>Yes</td></tr>
<tr><td>Port 1
P10 to P17</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 1-bit units
• Pull-up resistor can be turned on and off in 1-bit units
• Pin functions
P10: SIO0 data output
P11: SIO0 data input, bus I/O
P12: SIO0 clock I/O
P13: SIO1 data output
P14: SIO1 data input, bus I/O
P15: SIO1 clock I/O
P16: Timer 1 PWML output
P17: Timer 1 PWMH output, Beeper output</td><td>Yes</td></tr>
<tr><td>Port 2
P20 to P27</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 1-bit units
• Pull-up resistor can be turned on and off in 1-bit units
• Pin functions
P20: INT4 input/HOLD reset input/timer 1 event input/timer 0L capture input/
timer 0H capture input/INT6 input/timer 0L capture 1 input/small signal input
P21, P23: INT4 input/HOLD reset input/timer 1 event input/timer 0L capture input/
timer 0H capture input
P22: NT4 input/HOLD reset input/timer 1 event input/timer 0L capture input/
timer 0H capture input/HCTR signal input
P24: INT5 input/HOLD reset input/timer 1 event input/timer 0L capture input/
timer 0H capture input/INT7 input/timer 0H capture 1 input/small signal input
P25 to P27: INT5 input/HOLD reset input/timer 1 event input/timer 0L capture input/
Timer 0H capture input
• Interrupt acknowledge type
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising/
Falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT4</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT5</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT6</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT7</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
</table></td><td>Yes</td></tr>
<tr><td>Port 3
P30 to P36</td><td>I/O</td><td>• 7-bit I/O port
• I/O specifiable in 1-bit units
• Pull-up resistor can be turned on and off in 1-bit units
• Pin functions
P30: PWM4 output
P31: PWM5 output
P32: UART1 transmit
P33: UART1 receive
P34: UART2 transmit
P35: UART2 receive</td><td>Yes</td></tr>
</table>

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<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function description</th><th>Option</th></tr>
<tr><td>Port 7
P70 to P73</td><td>I/O</td><td>• 4-bit I/O port
• I/O specifiable in 1-bit units
• Pull-up resistor can be turned on and off in 1-bit units
• Pin functions
P70: INT0 input/HOLD release input/Timer 0L capture input/Output for watchdog timer
P71: INT1 input/HOLD release input/Timer 0H capture input
P72: INT2 input/HOLD release input/Timer 0 event input/Timer 0L capture input
P73: INT3 input with noise filter/Timer 0 event input/Timer 0H capture input
• Interrupt acknowledge type
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising/
Falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT0</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr>
<tr><td>INT1</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr>
<tr><td>INT2</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT3</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
</table></td><td>No</td></tr>
<tr><td>Port 8
P80 to P87</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 1-bit units
• Other functions
P80-P87: AD converter input port</td><td>No</td></tr>
<tr><td>Port A
PA0 to PA5</td><td>I/O</td><td>• 6-bit I/O port
• I/O specifiable in 1-bit units
• Pull-up resistor can be turned on and off in 1-bit units
• Pin functions
PA0: SIO7 data output
PA1: SIO7 data input, bus I/O
PA2: SIO7 clock I/O
PA3: SIO8 data output
PA4: SIO8 data input, bus I/O
PA5: SIO8 clock I/O</td><td>Yes</td></tr>
<tr><td>Port B
PB0 to PB2
PB4, PB6</td><td>I/O</td><td>• 5-bit I/O port
• I/O specifiable in 1-bit units
• Other functions
PB0: Output for field recognition signal
PB4: LPF connection for Slicer PLL
PB6: Input for CSYNC signal/CVD (Composite Video) signal</td><td>Yes</td></tr>
<tr><td>Port C
PC0 to PC7</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 1-bit units
• Pull-up resistor can be turned on and off in 1-bit units
• Other functions
PC0: OCSYNC output
PC1 to PC4: AD converter input port
PC5 to PC7: On-chip Debugger</td><td>Yes</td></tr>
<tr><td>Port E
PE0 to PE7</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 1-bit units
• Pull-up resistor can be turned on and off in 1-bit units
• Other functions
PE0-PE3: AD converter input port</td><td>No</td></tr>
<tr><td>Port F
PF0 to PF7</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 1-bit units
• Pull-up resistor can be turned on and off in 1-bit units
• Other functions
PF4: Remote control signal output</td><td>No</td></tr>
</table>

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Pin Name	I/O	Function description	Option
SIO2 Port SI2P0 to SI2P3	I/O	• 4-bit I/O port • I/O specifiable in 1-bit units • Other functions: SI2P0: SIO2 data output SI2P1: SIO2 data input, bus input/output SI2P2: SIO2 clock input/output SI2P3: SIO2 clock output	No
PWM0	O	• PWM0 output port • General-purpose I/O available	No
PWM1	O	• PWM1 output port • General-purpose I/O available	No
$\overline{RES}$	I	Reset pin	No
XT1	I	• Input terminal for 32.768kHz X'tal oscillation • Other functions: General-purpose input port Must be connected to $V_{DD}1$ if not to be used.	No
XT2	I/O	• Output terminal for 32.768kHz X'tal oscillation • Other functions: General-purpose I/O port Must be set for oscillation and kept open if not to be used.	No
CF1	I	Ceramic resonator input pin	No
CF2	O	Ceramic resonator output pin	No

Port Output Types

The table below lists the types of port outputs and the presence/absence of a pull-up resistor. Data can be read into any input port even if it is in the output mode.

Port	Options selected in units of	Option type	Output type	Pull-up resistor
P00 to P07	1 bit	1	CMOS	Programmable (Note 1)
		2	N-channel open drain	No
P10 to P17 P20 to P27 P30 to P36 PA0 to PA5 PC0 to PC7	1 bit	1	CMOS	Programmable
		2	N-channel open drain	Programmable
PB0 to PB2 PB4, PB6	1 bit	1	CMOS	No
		2	N-channel open drain	No
PE0 to PE7 PF0 to PF7	-	No	CMOS	Programmable
P70	-	No	N-channel open drain	Programmable
P71 to P73	-	No	CMOS	Programmable
P80 to P87	-	No	N-channel open drain	No
SI2P0, SI2P2 SI2P3 PWM0, PWM1	-	No	CMOS	No
SI2P1	-	No	CMOS (when selected as ordinary port) N-channel open drain (when SIO2 data is selected)	No
XT1	-	No	Input only	No
XT2	-	No	Output for 32.768kHz crystal oscillator N-channel open drain (when in general-purpose output mode)	No

Note 1: Programmable pull-up resistors for port 0 are controlled in 4-bit units (P00 to P03, P04 to P07).

Absolute Maximum Ratings at Ta = 25°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = V_{SS}VCO = 0V$

Parameter		Symbol	Pins/Remarks	Conditions	Specification				
					V_{DD}[V]	min	typ	max	unit
Maximum Supply voltage		$V_{DD}MAX$	$V_{DD}1$, $V_{DD}2$, $V_{DD}3$, $V_{DD}4$, $V_{DD}VCO$, $V_{DD}ODA$	$V_{DD}1=V_{DD}2=V_{DD}3=VDD4=V_{DD}VCO=V_{DD}ODA$		-0.3		+6.5	V
Input voltage		V_I(1)	XT1, CF1, $\overline{RES}$			-0.3		V_{DD}+0.3	
Input/Output Voltage		V_{IO}(1)	Ports 0, 1, 2 Ports 3, 7, 8 Ports A, B, C, E, F SI2P0 to SI2P3 PWM0, PWM1, XT2			-0.3		V_{DD}+0.3	
High level output current	Peak output current	IOPH(1)	Ports 0, 1, 2, 3 Ports A, B, C, E, F SI2P0 to SI2P3	CMOS output select per 1 application pin		-10			mA
		IOPH(2)	PWM0, PWM1	Per 1 application pin.		-20			
		IOPH(3)	P71 to P73	Per 1 application pin.		-5			
	Average output current (Note 1-1)	IOMH(1)	Ports 0, 1, 2, 3 Ports A, B, C, E, F SI2P0 to SI2P3	CMOS output select per 1 application pin		-10			
		IOMH(2)	PWM0, PWM1	Per 1 application pin.		-15			
		IOMH(3)	P71 to P73	Per 1 application pin.		-3			
	Total output current	ΣIOAH(1)	P71 to P73	Total of all applicable pins		-5			
		ΣIOAH(2)	PWM0, PWM1 SI2P0 to SI2P3	Total of all applicable pins		-20			
		ΣIOAH(3)	Ports 0, 2, 3	Total of all applicable pins		-30			
		ΣIOAH(4)	Port 0, 2, 3 PWM0, PWM1 SI2P0 to SI2P3	Total of all applicable pins		-50			
		ΣIOAH(5)	PB0 to PB2	Total of all applicable pins		-20			
		ΣIOAH(6)	Ports A, C	Total of all applicable pins		-20			
		ΣIOAH(7)	Ports A, C, PB0 to PB2	Total of all applicable pins		-40			
		ΣIOAH(8)	Port F	Total of all applicable pins		-20			
		ΣIOAH(9)	Ports 1, E	Total of all applicable pins		-20			
		ΣIOAH(10)	Ports 1, E, F	Total of all applicable pins		-40			
		ΣIOAH(11)	PB4, PB6	Total of all applicable pins		-20			
Low level output current	Peak output current	IOPL(1)	P02 to P07 Ports 1, 2, 3 Ports A, B, C, E, F SI2P0 to SI2P3 PWM0, PWM1	Per 1 application pin.				20	
		IOPL(2)	P00, P01	Per 1 application pin.				30	
		IOPL(3)	Ports 7, 8, XT2	Per 1 application pin.				10	
	Average output current (Note 1-1)	IOML(1)	P02 to P07 Ports 1, 2, 3 Ports A, B, C, E, F SI2P0 to SI2P3 PWM0, PWM1	Per 1 application pin.				15	
		IOML(2)	P00, P01	Per 1 application pin.				20	
		IOML(3)	Ports 7, 8, XT2	Per 1 application pin.				7.5	

Note 1-1: Average output current is average of current in 100ms interval.

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Parameter		Symbol	Pins/Remarks	Conditions	Specification				
					V_{DD}[V]	min	typ	max	unit
Low level output current	Total output current	ΣIOAL(1)	Port 7, XT2	Total of all applicable pins				15	mA
		ΣIOAL(2)	Port 8	Total of all applicable pins				15	
		ΣIOAL(3)	Ports 7, 8, XT2	Total of all applicable pins				30	
		ΣIOAL(4)	PWM0, PWM1 SI2P0 to SI2P3	Total of all applicable pins				40	
		ΣIOAL(5)	Ports 0, 2, 3	Total of all applicable pins				80	
		ΣIOAL(6)	Ports 0, 2, 3 PWM0, PWM1 SI2P0 to SI2P3	Total of all applicable pins				120	
		ΣIOAL(7)	PB0 to PB2	Total of all applicable pins				40	
		ΣIOAL(8)	Ports A, C	Total of all applicable pins				40	
		ΣIOAL(9)	Ports A, C PB0 to PB2	Total of all applicable pins				80	
		ΣIOAL(10)	Port F	Total of all applicable pins				40	
		ΣIOAL(11)	Ports 1, E	Total of all applicable pins				70	
		ΣIOAL(12)	Ports 1, E, F	Total of all applicable pins				110	
		ΣIOAL(13)	PB4, PB6	Total of all applicable pins				40	
Maximum power consumption		Pd max	QIP100E(14×20)					523	mW
Operating temperature range		Topr				-20		70	°C
Storage temperature range		Tstg				-55		125	

Recommended Operating Range at Ta = -20°C to +70°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = V_{SS}VCO = 0V$

Parameter	Symbol	Pins/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Operating supply voltage (Note 2-1, 2-2)	$V_{DD}(1)$	$V_{DD}1=V_{DD}2$ $=V_{DD}3=V_{DD}4$ $=V_{DD}VCO=V_{DD}ODA$	0.196µs ≤ tCYC ≤ 200µs		4.5		5.5	V
			1.47µs ≤ tCYC ≤ 200µs		2.7		5.5	
Data-slicer Operating supply voltage	$V_{DD}(2)$	$V_{DD}1=V_{DD}2$ $=V_{DD}3=V_{DD}4$ $=V_{DD}VCO=V_{DD}ODA$	0.196µs ≤ tCYC ≤ 0.340µs		4.75		5.25	
Base timer Day and time counter Operating supply voltage	$V_{DD}(3)$	$V_{DD}1$	• X'tal HOLD mode • Base timer clock is subclock. • FsX'tal=32.768kHz by crystal oscillation mode.		2.0		5.5	
Memory sustaining supply voltage	VHD	$V_{DD}1$	RAM and register contents in HOLD mode.		2.0		5.5	
High level input voltage	$V_{IH}(1)$	Ports 1, 2, 3, A PB6 SI2P0 to SI2P3 P71 to P73 P70 port input /interrupt side		2.7 to 5.5	$0.3V_{DD}$ +0.7		V_{DD}	
	$V_{IH}(2)$	Ports 0, 8 PB0 to PB2, PB4 Ports C, E, F PWM0, PWM1		2.7 to 5.5	$0.3V_{DD}$ +0.7		V_{DD}	
	$V_{IH}(3)$	P70 Watchdog timer side		2.7 to 5.5	$0.9V_{DD}$		V_{DD}	
	$V_{IH}(4)$	XT1, XT2, CF1, $\overline{RES}$		2.7 to 5.5	$0.75V_{DD}$		V_{DD}	
	$V_{IH}(5)$	P20, P24 Small signal input side		2.7 to 5.5	$0.75V_{DD}$		V_{DD}	

Note 2-1: V_{DD} must be held greater than or equal to 4.5V in the flash ROM onboard programming mode.

Note 2-2: Relationship between tCYC and oscillation frequency is 3/FmCF at a division ratio of 1/1 and 6/FmCF at a division ratio of 1/2.

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Parameter	Symbol	Pins/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Low level input voltage	V_{IL}(1)	Ports 1, 2, 3,A PB6 SI2P0 to SI2P3 P71 to P73 P70 port input /interrupt		2.7 to 5.5	V_{SS}		$0.1V_{DD}$ +0.4	V
	V_{IL}(2)	Ports 0, 8 PB0 to PB2, PB4 Ports C, E, F PWM0,PWM1		2.7 to 5.5	V_{SS}		$0.15V_{DD}$ +0.4	
	V_{IL}(3)	Port 70 Watchdog Timer		2.7 to 5.5	V_{SS}		$0.8V_{DD}$ -1.0	
	V_{IL}(4)	XT1, XT2, CF1, $\overline{RES}$		2.7 to 5.5	V_{SS}		$0.25V_{DD}$	
	V_{IL}(5)	P20, P24 Small signal input side		2.7 to 5.5	V_{SS}		$0.25V_{DD}$	
Composite video signal input voltage (Note 2-4)	VCVD(1)	PB6(CVD)	2Vp-p input mode	5.0	1.4	2.0	2.6	Vp-p
	VCVD(2)		1Vp-p input mode	5.0	0.7	1	1.3	
Instruction cycle time (Note 2-2)	tCYC		Data-slicer Operating mode	4.75 to 5.25	0.196		0.340	µs
				4.5 to 5.5	0.196		200	
				2.7 to 5.5	1.470		200	
Oscillation frequency Range (Note 2-3)	FmCF(1)	CF1, CF2	15MHz ceramic oscillation See Fig. 1.	4.5 to 5.5		15		MHz
	FmRC		Internal RC oscillation	2.7 to 5.5	0.3	1.0	2.0	
	FmMRC		Frequency variable RC oscillation source oscillation	2.7 to 5.5		16		
	FsX'tal	XT1, XT2	32.768kHz crystal oscillation. See Fig. 2.	2.7 to 5.5		32.768		kHz

Note 2-2: Relationship between tCYC and oscillation frequency is 3/FmCF at a division ratio of 1/1 and 6/FmCF at a division ratio of 1/2.

Note 2-3: See Tables 1 and 2 for the oscillation constants.

Note 2-4: When setting DSLDACT register's bit7 = 0, bit6 = 0. See diagram 9 for external circuit.

Electrical Characteristics at Ta = -20°C to +70°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = V_{SS}VCO = 0V$

Parameter	Symbol	Pins/Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
High level input current	$I_{IH}(1)$	Ports 0, 1, 2 Ports 3, 7, 8 Ports A, B, C, E, F SI2P0 to SI2P3 $\overline{RES}$ PWM0, PWM1	Output disable Pull-up resistor OFF $V_{IN}=V_{DD}$ (including the off-leak current of the output Tr.)	2.7 to 5.5			1	µA
	$I_{IH}(2)$	XT1, XT2	Using as an input port $V_{IN}=V_{DD}$	2.7 to 5.5			1	
	$I_{IH}(3)$	CF1	$V_{IN}=V_{DD}$	2.7 to 5.5			15	
	$I_{IH}(4)$	P20, P24 Small signal input side	V_{IN}=VBIAS+0.5 (VBIAS is bias voltage)	4.5 to 5.5	4.2	8.5	15	
Low level input current	$I_{IL}(1)$	Ports 0, 1, 2 Ports 3, 7, 8 Ports A, B, C, E, F SI2P0 to SI2P3 $\overline{RES}$ PWM0, PWM1	Output disable Pull-up resistor OFF $V_{IN}=V_{SS}$ (including the off-leak current of the output Tr.)	2.7 to 5.5	-1			
	$I_{IL}(2)$	XT1, XT2	Using as an input port $V_{IN}=V_{SS}$	2.7 to 5.5	-1			
	$I_{IL}(3)$	CF1	$V_{IN}=V_{SS}$	2.7 to 5.5	-15			
	$I_{IL}(4)$	P20, P24 Small signal input side	$V_{IN}=V_{BIAS}+0.5$ (V_{BIAS} is bias voltage)	4.5 to 5.5	-15	-8.5	-4.2	
High level output voltage	$V_{OH}(1)$	Ports 0, 1, 2, 3 Ports A, B, C, E, F SI2P0 to SI2P3	I_{OH}=-1.0mA	4.5 to 5.5	V_{DD}-1			V
	$V_{OH}(2)$		I_{OH}=-0.4mA	3.0 to 5.5	V_{DD}-0.4			
	$V_{OH}(3)$	Ports 71, 72, 73	I_{OH}=-0.4mA	3.0 to 5.5	V_{DD}-0.4			
	$V_{OH}(4)$	PWM0, PWM1	I_{OH}=-10mA	4.5 to 5.5	V_{DD}-1.5			
	$V_{OH}(5)$	P30, P31(PWM4, 5 output mode)	I_{OH}=-1.6mA	3.0 to 5.5	V_{DD}-0.4			
Low level output voltage	$V_{OL}(1)$	Ports 0, 1, 2, 3 Ports A, B, C, E, F SI2P0 to SI2P3 PWM0, PWM1,	I_{OL}=10mA	4.5 to 5.5			1.5	
	$V_{OL}(2)$		I_{OL}=1.6mA	3.0 to 5.5			0.4	
	$V_{OL}(3)$	P00, P01	I_{OL}=30mA	4.5 to 5.5			1.5	
	$V_{OL}(4)$		I_{OL}=5.0mA	3.0 to 5.5			0.4	
	$V_{OL}(5)$	Ports 7, 8, XT2	I_{OL}=1.6mA	3.0 to 5.5			0.4	
Pull-up resistation	Rpu(1)	Ports 0, 1, 2, 3 Port 7 Ports A, C, E, F	$V_{OH}=0.9V_{DD}$	4.5 to 5.5	15	40	70	kΩ
	Rpu(2)			2.7 to 5.5	15	40	150	
Hysteresis Voltage	VHYS(1)	$\overline{RES}$ Ports 1, 2, 3, 7, A PB6 SI2P0 to SI2P3		4.5 to 5.5		$0.1V_{DD}$		V
	VHYS(2)	P20, P24 Small signal input side		4.5 to 5.5		$0.1V_{DD}$		
Pin capacitance	CP	All pins	• For pins other than that under test: $V_{IN}=V_{SS}$ • f=1MHz • Ta=25°C	2.7 to 5.5		10		pF
Input voltage sensitivity	Vsen	P20, P24 Small signal input side		4.5 to 5.5	$0.12V_{DD}$			Vp-p
Bias Voltage	VBIAS	P20, P24 Small signal input side		5.0		$0.5V_{DD}$		V
Composite video signal input clamping voltage	VCLMP	PB6(CVD)	Pedestal voltage	5.0		1.9		V

Serial I/O Characteristics at Ta = -20°C to +70°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = V_{SS}VCO = 0V$

1. SIO0 Serial I/O Characteristics (Note 4-1-1)

Parameter			Symbol	Pins/ Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Serial clock	Input clock	Frequency	tSCK(1)	SCK0(P12)	• See Fig. 6.	2.7 to 5.5	2			tCYC
		Low level pulse width	tSCKL(1)				1			
		High level pulse width	tSCKH(1)				1			
			tSCKHA(1a)		• Continuous data transmission/reception mode • SIO2 is not in use simultaneous. • Universal remote control transmitter is not in use simultaneous. • See Fig. 6. • (Note 4-1-2)		4			
			tSCKHA(1b)		• Continuous data transmission/reception mode • SIO2 is in use simultaneous. • Universal remote control transmitter is in use simultaneous. • See Fig. 6. • (Note 4-1-2)		9			
	Output clock	Frequency	tSCK(2)	SCK0(P12)	• CMOS output selected. • See Fig. 6.	2.7 to 5.5	4/3			tSCK
		Low level pulse idth	tSCKL(2)				1/2			
		High level pulse idth	tSCKH(2)				1/2			
			tSCKHA(2a)		• Continuous data transmission/reception mode • SIO2 is not in use simultaneous. • Universal remote control transmitter is not in use simultaneous. • CMOS output selected. • See Fig. 6.e		tSCKH(2) +2tCYC		tSCKH(2) +(10/3)tCYC	tCYC
			tSCKHA(2b)		• Continuous data transmission/reception mode • SIO2 is in use simultaneous. • Universal remote control transmitter is in use simultaneous. • CMOS output selected. • See Fig. 6.		tSCKH(2) +2tCYC		tSCKH(2) +(25/3)tCYC	
Serial input	Data setup time		tsDI(1)	SI0(P11), SB0(P11)	• Must be specified with respect to rising edge of SIOCLK • See fig. 6.	2.7 to 5.5	0.03			µs
	Data hold Time		thDI(1)				0.03			

Note 4-1-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-1-2: To use serial-clock-input in continuous trans/rec mode, a time from SI0RUN being set when serial clock is "H" to the first negative edge of the serial clock must be longer than tSCKHA.

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Parameter			Symbol	Pins/ Remarks	Conditions	Specification				
						V_{DD}[V]	min	typ	max	unit
Serial output	Input clock	Output delay time	tdDO(1)	SO0(P10), SB0(P11)	• Continuous data transmission/reception mode • (Note 4-1-3)	2.7 to 5.5			(1/3)tCYC +0.05	µs
			tdDO(2)		• Synchronous 8-bit mode. • (Note 4-1-3)				1tCYC +0.05	
	Output clock		tdDO(3)		• (Note 4-1-3)				(1/3)tCYC +0.05	

Note 4-1-3: Must be specified with respect to falling edge of SIOCLK. Must be specified as the time to the beginning of output state change in open drain output mode. See Fig. 6.

2. SIO1 Serial I/O Characteristics (Note 4-2-1)

Parameter			Symbol	Pins/ Remarks	Conditions	Specification				
						V_{DD}[V]	min	typ	max	uni
Serial clock	Input clock	Frequency	tSCK(3)	SCK1(P15)	• See Fig. 6.	2.7 to 5.5	2			tCYC
		Low level pulse width	tSCKL(3)				1			
		High level pulse width	tSCKH(3)				1			
	Output clock	Frequency	tSCK(4)	SCK1(P15)	• CMOS output selected. • See Fig. 6.		2			
		Low level pulse width	tSCKL(4)			2.7 to 5.5	1/2			tSCK
		High level pulse width	tSCKH(4)				1/2			
Serial input	Data setup time		tsDI(2)	SI1(P14), SB1(P14)	• Must be specified with respect to rising edge of SIOCLK • See fig. 6.	2.7 to 5.5	0.03			µs
	Data hold time		thDI(2)				0.03			
Serial output	Output delay time		tdDO(4)	SO1(P13), SB1(P14)	• Must be specified with respect to falling edge of SIOCLK • Must be specified as the time to the beginning of output state change in open drain output mode. • See Fig. 6.	2.7 to 5.5			(1/3)tCYC +0.05	

Note 4-2-1: These specifications are theoretical values. Add margin depending on its use.

3. SIO2 Serial I/O Characteristics (Note 4-3-1)

Parameter			Symbol	Pins/ Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Serial clock	Input clock	Frequency	tSCK(5)	SCK2 (SI2P2)	• See Fig. 6.	2.7to 5.5	2			tCYC
		Low level pulse width	tSCKL(5)				1			
		High level Pulse width	tSCKH(5)				1			
			tSCKHA(5a)		• Continuous data transmission/reception mode of SIO0 is not in use simultaneous. • Universal remote control transmitter is not in use simultaneous. • See Fig. 6. • (Note 4-3-2)		4			
			tSCKHA(5b)		• Continuous data transmission/reception mode of SIO0 is in use simultaneous. • Universal remote control transmitter is in use simultaneous. • See Fig. 6. • (Note 4-3-2)		10			
	Output clock	Frequency	tSCK(6)	SCK2 (SI2P2), SCK2O (SI2P3)	• CMOS output selected. • See Fig. 6.	2.7 to 5.5	4/3			tSCK
		Low level pulse width	tSCKL(6)				1/2			
		High level pulse width	tSCKH(6)				1/2			
			tSCKHA(6a)		• Continuous data transmission/reception mode of SIO0 is not in use simultaneous. • Universal remote control transmitter is not in use simultaneous. • CMOS output selected. • See Fig. 6.		tSCKH(6) +(5/3) tCYC		tSCKH(6) +(10/3) tCYC	tCYC
			tSCKHA(6b)		• Continuous data transmission/reception mode of SIO0 is in use simultaneous. • Universal remote control transmitter is in use simultaneous. • CMOS output elected. • See Fig. 6.		tSCKH(6) +(5/3) tCYC		tSCKH(6) +(28/3) tCYC	
Serial input	Data setup time		tsDI(3)	SI2(SI2P1), SB2(SI2P1)	• Must be specified with respect to rising edge of SIOCLK • See fig. 6.	2.7 to 5.5	0.03			µs
	Data hold time		thDI(3)				0.03			
Serial output	Output delay time		tdDO(5)	SO2(SI2P0) SB2(SI2P1)	• Must be specified with respect to falling edge of SIOCLK • Must be specified as the time to the beginning of output state change in open drain output mode. • See Fig. 6.	2.7 to 5.5			(1/3)tCYC +0.05	

Note 4-3-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-3-2: To use serial-clock-input , a time from SI2RUN being set when serial clock is "H" to the first negative edge of the serial clock must be longer than tSCKHA.

4. SIO7, SIO8 Serial I/O Characteristics (Note 4-4-1)

Parameter			Symbol	Pins/ Remarks	Conditions		Specification			
						V_{DD}[V]	min	typ	max	uni
Serial clock	Input clock	Frequency	tSCK(7)	SCK7(PA2), SCK8(PA5)	• See Fig. 6. • (Note 4-4-2)	2.7 to 5.5	2			tCYC
		Low level pulse width	tSCKL(7)				1			
		High level pulse width	tSCKH(7)				1			
	Output clock	Frequency	tSCK(8)	SCK7(PA2), SCK8(PA5)	• CMOS output selected. • See Fig. 6.	2.7 to 5.5	4/3			
		Low level pulse width	tSCKL(8)				1/2			tSCK
		High level pulse width	tSCKH(8)				1/2			
			tSCKHA(8)				1.5			
Serial input	Data setup time		tsDI(4)	SI7(PA1), SB7(PA1), SI8(PA4), SB8(PA4)	• Must be specified with respect to rising edge of SIOCLK • See fig. 6.	2.7 to 5.5	0.03			µs
	Data hold time		thDI(4)				0.03			
Serial output	Input clock	Output delay time	tdDO(6)	SO7(PA0), SB7(PA1), SO8(PA3), SB8(PA4)	• Must be specified with respect to falling edge of SIOCLK • Must be specified as the time to the beginning of output state change in open drain output mode. • See Fig. 6.	2.7 to 5.5			1tCYC +0.05	
	Output clock		tdDO(7)						(1/3)tCYC +0.05	

Note 4-4-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-4-2: When starting transmission/reception of SIO7(SIO8) using serial-clock-input, a time from SI7RUN(SI8RUN) being set when serial clock is "H" to the first negative edge of the serial clock must be longer than 1tCYC.

Pulse Input Conditions at Ta = -20°C to +70°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = V_{SS}VCO = 0V$

Parameter	Symbol	Pins/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
High/low level pulse width	tPIH(1) tPIL(1)	INT0(P70), INT1(P71), INT2(P72) INT4(P20 to P23), INT5(P24 to P27), INT6(P20), INT7(P24)	• Interrupt source flag can be set. • Event inputs for timer 0 or 1 are enabled.	2.7 to 5.5	1			tCYC
	tPIH(2) tPIL(2)	INT3(P73) when noise filter time constant is 1/1.	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	2.7 to 5.5	2			
	tPIH(3) tPIL(3)	INT3(P73) (The noise rejection clock is selected to 1/32.)	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	2.7 to 5.5	64			
	tPIH(4) tPIL(4)	INT3(P73) (The noise rejection clock is selected to 1/128.)	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	2.7 to 5.5	256			
	tPIH(5) tPIL(5)	HCTR(P22) CSYNC(PB6)	• Count clock inputs for H-counter are enabled.	2.7 to 5.5	1			
	tPIL(6)	$\overline{RES}$	Reset acceptable	2.7 to 5.5	200			µs

AD Converter Characteristics at Ta = -20°C to +70°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = V_{SS}VCO = 0V$

Parameter	Symbol	Pins/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Resolution	N	AN0(P80) to AN7(P87), AN8(PC1), AN9(PC2), AN10(PC3), AN11(PC4), AN12(PE0), AN13(PE1), AN14(PE2), AN15(PE3)		3.0 to 5.5		8		bit
Absolute precision	ET		(Note 6-1)	3.0 to 5.5			±1.5	LSB
Conversion time	TCAD		AD conversion time=32 × tCYC (when ADCR2=0) (Note 6-2)	4.5 to 5.5	12.54 (tCYC= 0.396µs)		97.92 (tCYC= 3.06µs)	µs
				3.0 to 5.5	47.04 (tCYC= 1.47µs)		97.92 (tCYC= 3.06µs)	
			AD conversion time=64 × tCYC (when ADCR2=1) (Note 6-2)	4.5 to 5.5	12.54 (tCYC= 0.198µs)		97.92 (tCYC= 1.53µs)	
Analog input voltage range	VAIN			3.0 to 5.5	V_{SS}		V_{DD}	V
Analog port input current	IAINH		VAIN=V_{DD}	3.0 to 5.5			1	µA
	IAINL		VAIN=V_{SS}	3.0 to 5.5	-1			

Note 6-1: The quantization error (±1/2 LSB) is excluded from the absolute accuracy value.

Note 6-2: The conversion time refers to the interval from the time the instruction for starting the converter is issued till the complete digital value corresponding to the analog input value is loaded in the required register.

Consumption Current Characteristics

at Ta = -20°C to +70°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = V_{SS}VCO = 0V$

Parameter	Symbol	Pins/ Remarks	Conditions		Specification			
				V_{DD}[V]	min	typ	max	unit
Normal mode consumption current (Note 7-1)	IDDOP(1)	$V_{DD}1$ =$V_{DD}2$ =$V_{DD}3$ =$V_{DD}4$ =$V_{DD}ODA$ =$V_{DD}VCO$	• FmCF=15MHz ceramic oscillation mode • FsX'tal=32.768kHz by crystal oscillation mode • System clock set to 15MHz side • Internal RC oscillation stopped • frequency variable RC oscillation stopped • 1/1 frequency division ratio. • Slicer PLL is in running. • Slicer RC oscillation is in running. • Data Slicer is in running.	4.75 to 5.25		17	38	mA
	IDDOP(2)		• FmCF=15MHz ceramic oscillation mode • FsX'tal=32.768kHz by crystal oscillation mode • System clock set to 15MHz side • Internal RC oscillation stopped • frequency variable RC oscillation stopped • 1/1 frequency division ratio.	4.5 to 5.5		10	24	
	IDDOP(3)		• FmCF=0Hz(oscillation stopped) • FsX'tal=32.768kHz by crystal oscillation mode • System clock set to internal RC oscillation • frequency variable RC oscillation stopped •1/2 frequency division ratio.	4.5 to 5.5		0.7	4.5	
	IDDOP(4)			2.7 to 4.5		0.4	3	
	IDDOP(5)		• FmCF=0Hz(oscillation stopped) • FsX'tal=32.768kHz by crystal oscillation mode. • System clock set to 1MHz with frequency variable RC oscillation • Internal RC oscillation stopped • 1/2 frequency division ratio.	4.5 to 5.5		1.3	6	
	IDDOP(6)			2.7 to 4.5		0.8	4.5	
	IDDOP(7)		• FmCF=0Hz(oscillation stopped) • FsX'tal=32.768kHz by crystal oscillation mode. • System clock set to 32.768kHz side. • Internal RC oscillation stopped • frequency variable RC oscillation stopped • 1/2 frequency division ratio.	4.5 to 5.5		40	120	µA
	IDDOP(8)			2.7 to 4.5		18	80	

Note 7-1: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors

Continued on next page.

Continued from preceding page.

Parameter	Symbol	Pins/ Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
HALT mode consumption current (Note 7-1)	IDDHALT(1)	$V_{DD}1$ =$V_{DD}2$ =$V_{DD}3$ =$V_{DD}4$ =V_{DD}VCO =V_{DD}ODA	• HALT mode • FmCF=15MHz ceramic oscillation mode • FsX'tal=32.768kHz by crystal oscillation mode • System clock set to 15MHz side • Internal RC oscillation stopped • frequency variable RC oscillation stopped • 1/1 frequency division ratio.	4.5 to 5.5		5	10	mA
	IDDHALT(2)		• HALT mode • FmCF=0Hz(oscillation stopped) • FsX'tal=32.768kHz by crystal oscillation mode • System clock set to internal RC oscillation • frequency variable RC oscillation stopped •1/2 frequency division ratio.	4.5 to 5.5		0.4	1.5	
	IDDHALT(3)			2.7 to 4.5		0.2	1	
	IDDHALT(4)		• HALT mode • FmCF=0Hz(oscillation stopped) • FsX'tal=32.768kHz by crystal oscillation mode. • System clock set to 1MHz with frequency variable RC oscillation • Internal RC oscillation stopped • 1/2 frequency division ratio.	4.5 to 5.5		1.0	4.5	
	IDDHALT(5)			2.7 to 4.5		0.6	3.5	
	IDDHALT(6)		• HALT mode • FmCF=0Hz(oscillation stopped) • FsX'tal=32.768kHz by crystal oscillation mode. • System clock set to 32.768kHz side. • Internal RC oscillation stopped • frequency variable RC oscillation stopped • 1/2 frequency division ratio.	4.5 to 5.5		25	70	µA
	IDDHALT(7)			2.7 to 4.5		10	50	
Current drain during HOLD mode	IDDHOLD(1)	$V_{DD}1$	• HOLD mode • CF1=V_{DD} or open (External clock mode)	4.5 to 5.5		0.085	20	
	IDDHOLD(2)			2.7 to 4.5		0.02	15	
Current drain during time-base clock HOLD mode	IDDHOLD(3)	$V_{DD}1$	• Timer HOLD mode • CF1=V_{DD} or open (External clock mode) • FsX'tal=32.768kHz by crystal oscillation mode	4.5 to 5.5		21	60	
	IDDHOLD(4)			2.7 to 4.5		7	40	

Note 7-1: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors

F-ROM Write Characteristics at Ta = +10°C to +55°C, $V_{SS}1$ = $V_{SS}2$ = $V_{SS}3$ = $V_{SS}4$ = V_{SS}VCO = 0V

Parameter	Symbol	Pins/ Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Onboard programming current	IDDFW(1)	$V_{DD}1$	• 128-byte programming • Erasing current including	4.5 to 5.5		25	40	mA
Programming time	tFW(1)		• 128-byte programming • Erasing current including • Time for setting up 128 byte data is excluded.	4.5 to 5.5		25	35	ms

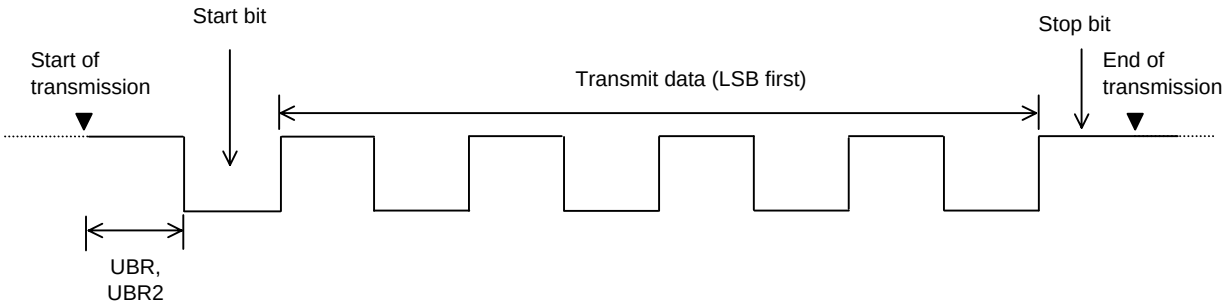
UART(Full Duplex) Operating Conditions

at Ta = -20°C to +70°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = V_{SS}VCO = 0V$

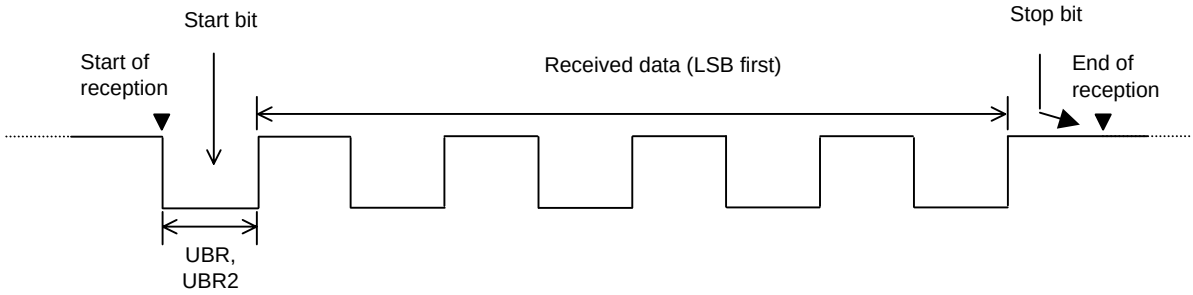
Parameter	Symbol	Pins/Remarks	Conditions	Specification				
			V_{DD}[V]	min	typ	max	unit
Clock rate	UBR,UBR2	UTX1(P32), URX1(P33), UTX2(P34), URX2(P35)	2.7 to 5.5	16/3		8192/3	tCYC

Data length: 7,8,and 9 bits (LSB first)
Stop bits: 1 bit (2-bit in continuous data transmission)
Parity bits: Non

Example of Continuous 8-bit Data Transmission Mode Processing (First Transmit Data = 55H)



Example of Continuous 8-bit Data Reception Mode Processing (First Receive Data = 55H)



Automatic transmission output characteristics

at Ta = -20°C to +70°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = V_{SS}VCO = 0V$

Parameter			Symbol	Pins/ Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Serial clock	Input clock	Frequency	tSCK(9)	SCK7(PA2),	See fig. 8. • (Note10-1)	4.5 to 5.5	4			tCYC
		Low level pulse width	tSCKL(9)				2			
			tSCKLA(9)				2			
		High level pulse width	tSCKH(9)				2			
			tSCKHA(9)				2			
			tBLKSEP(9a)		See fig. 8. • Transfer continuous data blocks • (Note10-1)		4			
			tBLKSEP(9b)		See fig. 8. • Transfer continuous data blocks with skipping S-number of data blocks • (Note10-1)		4+ (2/3) •S			
	Output clock	Frequency	tSCK(10)	SCK7(PA2),	• CMOS output selected • See fig. 8. • (Note10-1)	4.5 to 5.5	26/3			
		Low level pulse width	tSCKL(10)				1/2			tSCK
			tSCKLA(10)				1/2			
		High level pulse width	tSCKH(10)				1/2			
			tSCKHA(10)				1.5			
Serial output	Output delay time		tdDO(8)	SB7(PA1)	• Must be specified with respect to falling edge of SIOCLK • Must be specified as the time to the beginning of output state change in open drain output mode. • See fig. 8.	4.5 to 5.5			1tCYC +0.05	µs

Note10-1: When starting transmission, a time from ECST begin set when serial clock is “H” to the first negative edge of serial clock must be longer than the following.

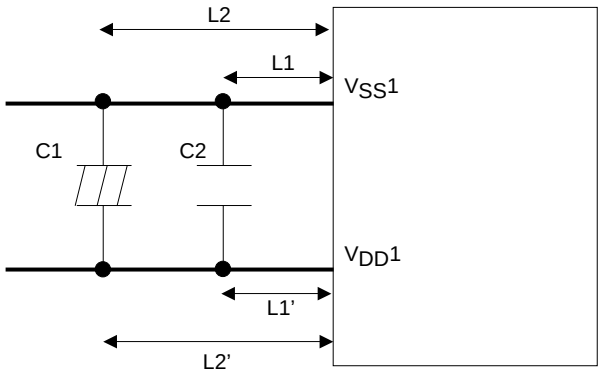
(4 + (2/3) • S) • tCYC

S: Skipping number of data block when starting transmission.

$V_{DD}1$, $V_{SS}1$ Terminal condition

It is necessary to place capacitors between $V_{DD}1$ and $V_{SS}1$ as describe below.

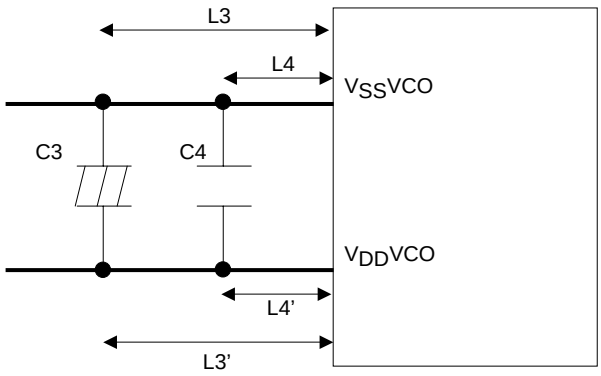
- Place capacitors as close to $V_{DD}1$ and $V_{SS}1$ as possible.
- Place capacitors so that the length of each terminal to the each leg of the capacitor be equal (L1 = L1', L2 = L2').
- Place high capacitance capacitor C1 and low capacitance capacitor C2 in parallel.
- Capacitance of C2 must be more than 0.05μF.
- Use thicker pattern for $V_{DD}1$ and $V_{SS}1$.



V_{DD}VCO, V_{SS}VCO Terminal condition

It is necessary to place capacitors between V_{DD}VCO and V_{SS}VCO as describe below.

- Place capacitors as close to V_{DD}VCO and V_{SS}VCO as possible.
- Place capacitors so that the length of each terminal to the each leg of the capacitor be equal (L3 = L3', L4 = L4').
- Place high capacitance capacitor C3 and low capacitance capacitor C4 in parallel.
- Capacitance of C4 must be more than 0.05μF.
- Use thicker pattern for V_{DD}VCO and V_{SS}VCO.



Characteristics of a Sample Main System Clock Oscillation Circuit

Given below are the characteristics of a sample main system clock oscillation circuit that are measured using a SANYO-designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation

Table 1 Characteristics of a Sample Main System Clock Oscillator Circuit with a Ceramic Oscillator

Nominal Frequency	Vendor Name	Oscillator Name	Circuit Constant			Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C1 [pF]	C2 [pF]	Rd1 [Ω]		typ [ms]	max [ms]	
15MHz	MURATA	CSTCE15M0V53-R0	(15)	(15)	470	3.0 to 5.5	0.1	0.5	Internal C1, C2 SMD-type

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized in follwing cases (see Figure 4).

- The time interval that is required for the oscillation to get stabilized after V_{DD} goes above the operating voltage lower limit.
- The time interval that is required for the oscillation to get stabilized after the instruction for starting the mainclock oscillation circuit is executed.
- The time interval that is required for the oscillation to get stabilized after the HOLD mode is reset and ocsillation is started.
- The time interval that is required for the oscillation to get stabilized after the X'tal Hold mode, under the state which the CFSTOP (bit 0 of the OCR register) = 0, is reset and ocsillation is started.

Characteristics of a Sample Subsystem Clock Oscillator Circuit

Given below are the characteristics of a sample subsystem clock oscillation circuit that are measured using a SANYO-designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 2 Characteristics of a Sample Subsystem Clock Oscillator Circuit with a Crystal Oscillator

Nominal Frequency	Vendor Name	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C3 [pF]	C4 [pF]	Rf1 [Ω]	Rd2 [Ω]		typ [s]	max [s]	
32.768kHz	EPSON TOYOCOM	MC-306	18	18	OPEN	560k	2.2 to 5.5	1.3	3.0	Applicable CL value = 12.5pF SMD-type

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized in follwing cases (see Figure 4).

- The time interval that is required for the oscillation to get stabilized after V_{DD} goes above the operating voltage lower limit.
- The time interval that is required for the oscillation to get stabilized after the instruction for starting the subclock oscillation circuit is executed.
- The time interval that is required for the oscillation to get stabilized after the Hold mode, under the state which the EXTOSC (bit 6 of the OCR register) = 1, is reset and ocsillation is started.
- The time interval that is required for the oscillation to get stabilized after the Hold mode, under the state which the DMSRUN (bit 7 of the DMSCNT register) = 1, is reset and ocsillation is started.

Note: The components that are involved in oscillation should be placed as close to the IC and to one another as possible because they are vulnerable to the influences of the circuit pattern.

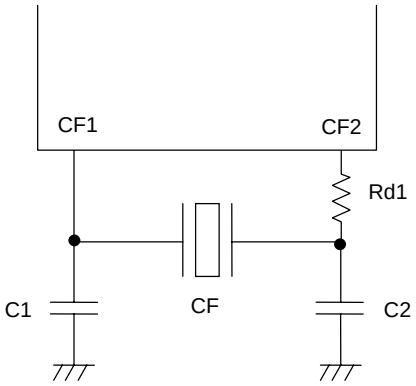


Figure 1 Ceramic Oscillation Circuit

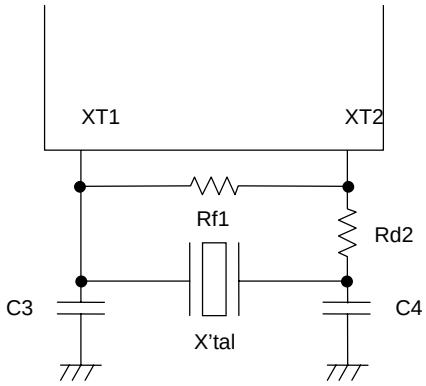


Figure 2 Crystal Oscillation Circuit

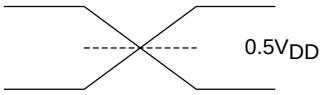
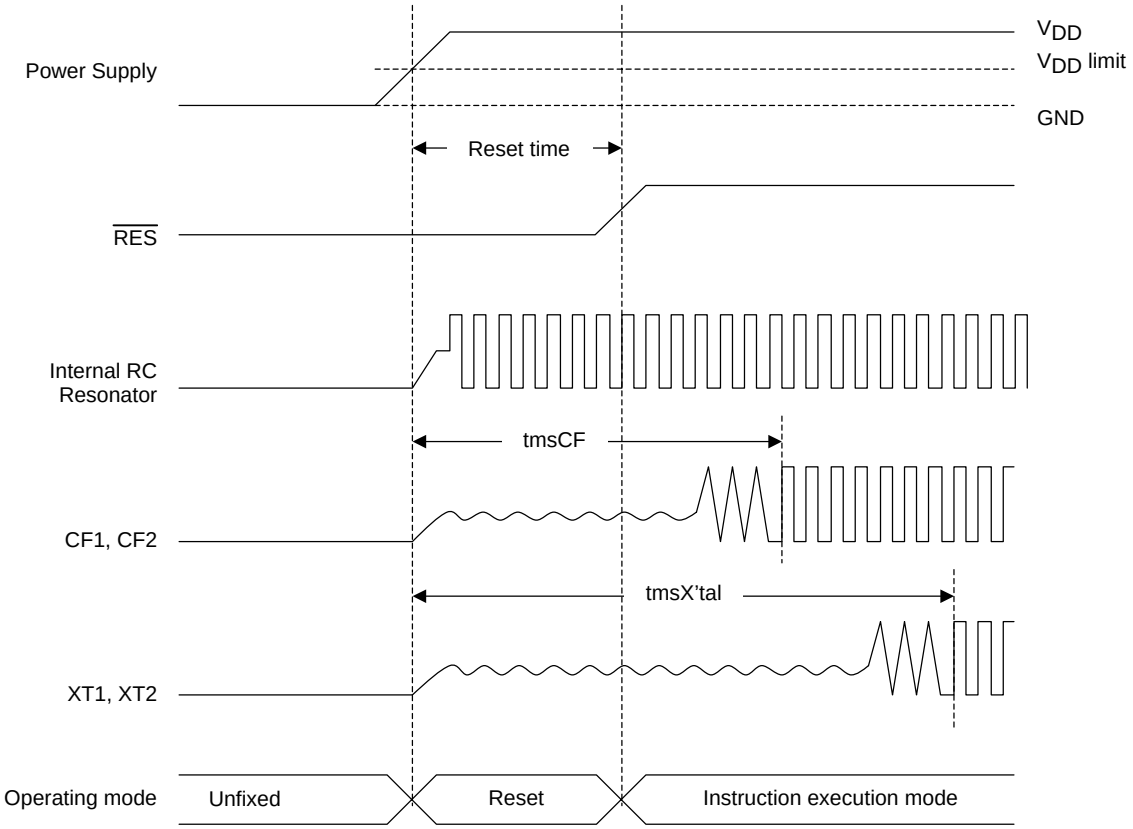
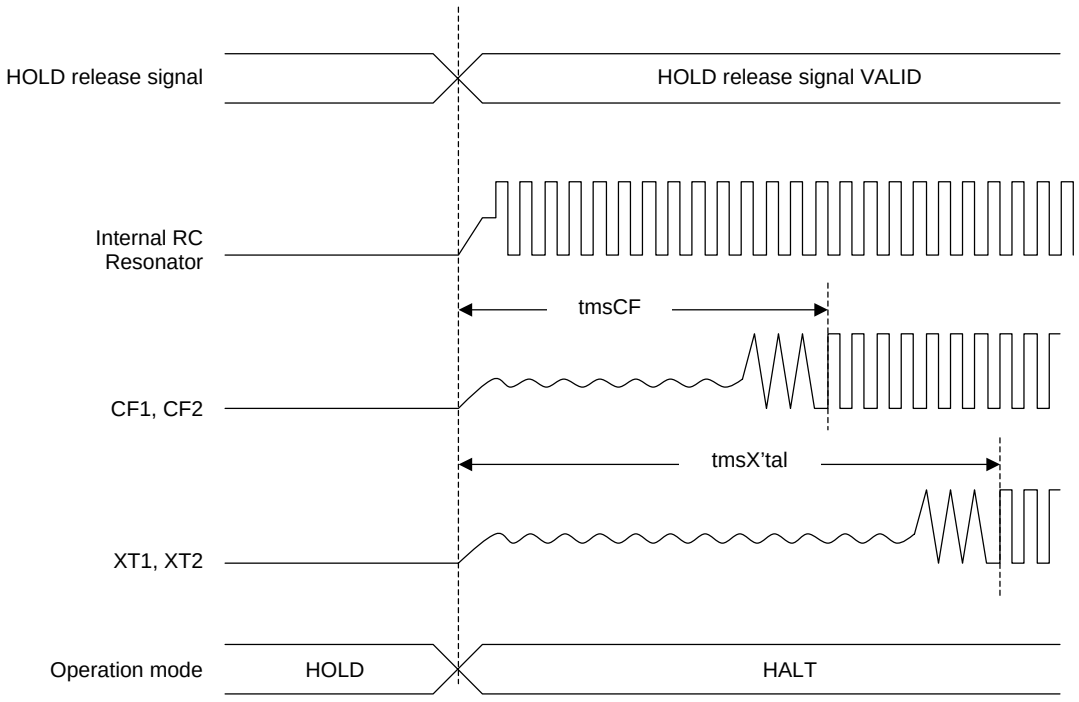


Figure 3 AC Timing Point

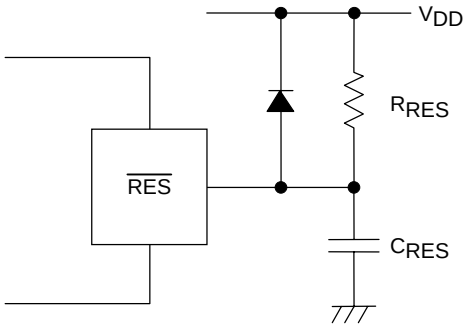


Reset Time and Oscillation Stabilization Time



HOLD Reset Signal and Oscillation Stabilization Time

Figure 4 Oscillation Stabilization Time



Note :
Select C_{RES} and R_{RES} value to assure that at least 200µs reset time is generated after the V_{DD} becomes higher than the minimum operating voltage.

Figure 5 Reset Circuit

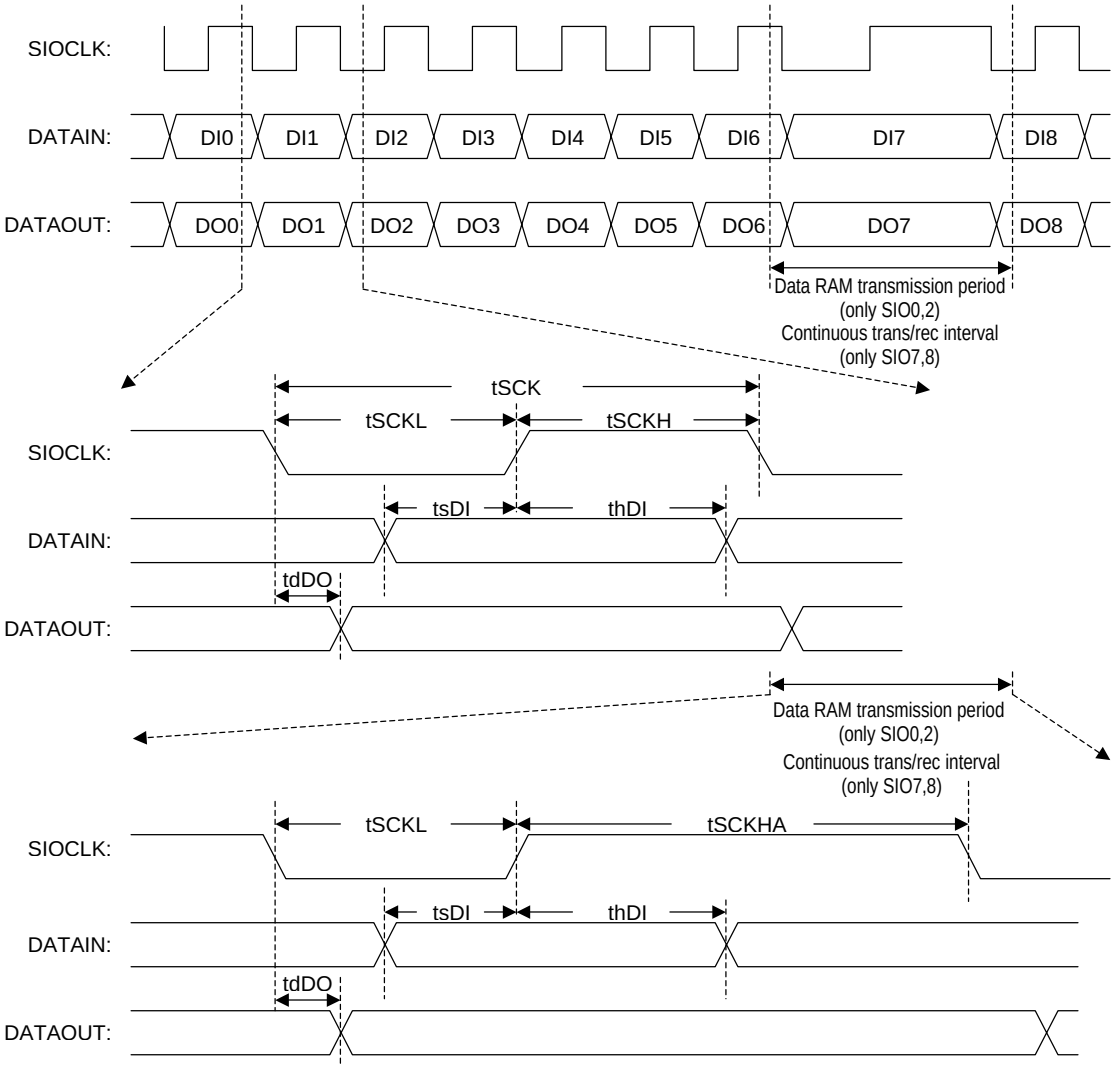


Figure 6 Serial I/O Waveforms

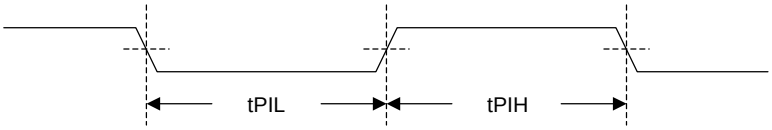


Figure 7 Pulse Input Timing Condition

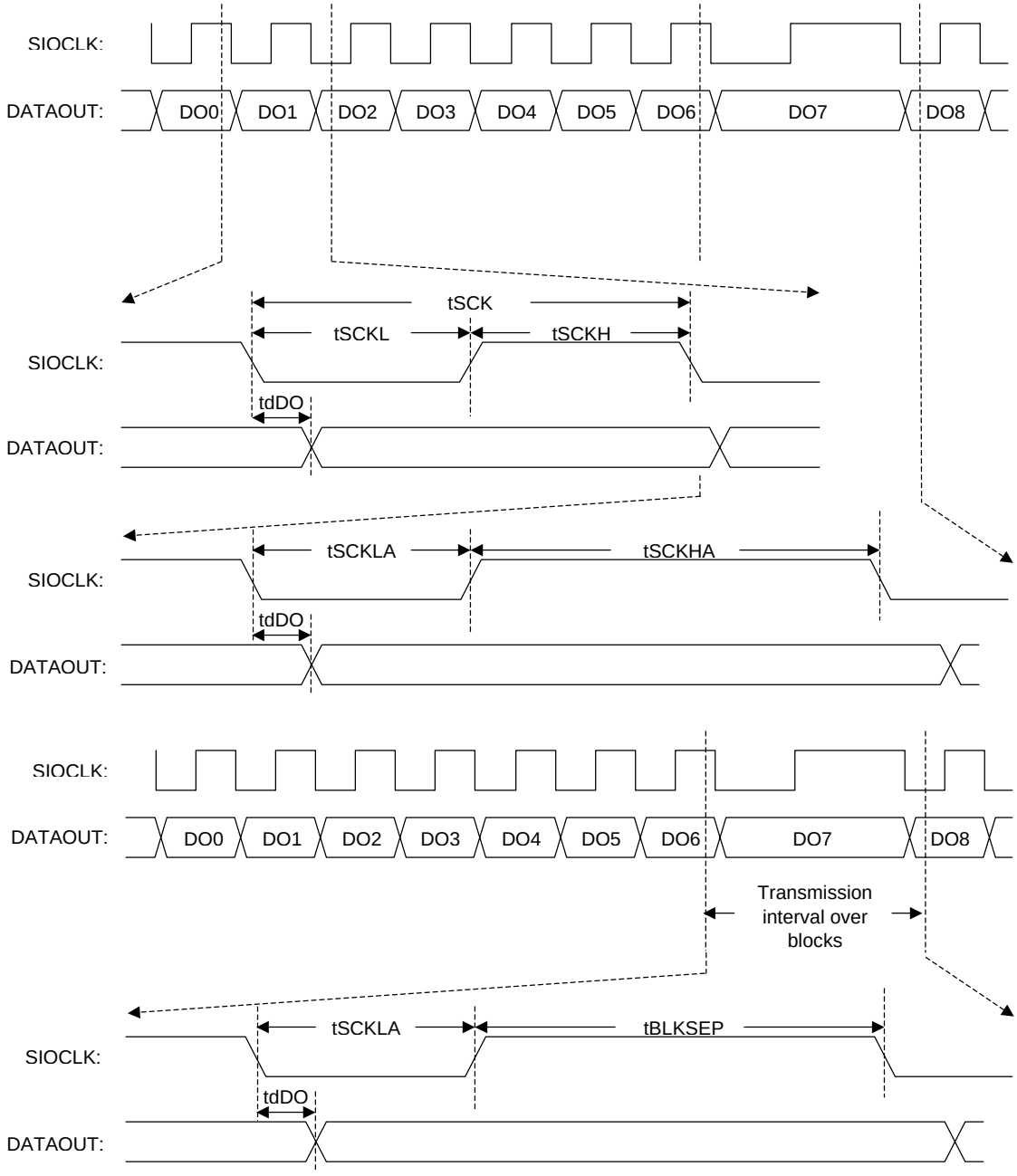


Figure 8 Automatic Transmission Output Waveforms

Table 3 Cfcvd constants

	Cfcvd
VPS/PDC/PAL-WSS Antiope EPG-J VBID	OPEN
XDS-1X XDS-2X	820pF

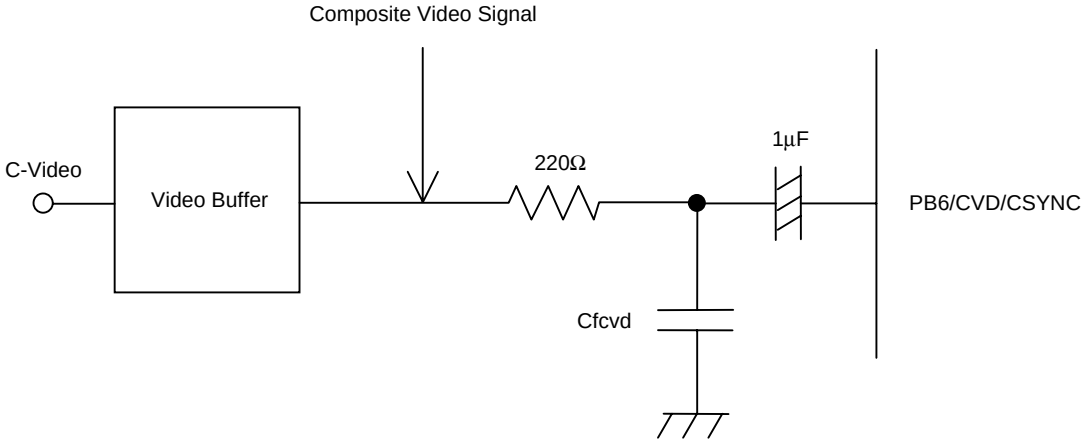


Figure 9 Recommended CVD Circuit

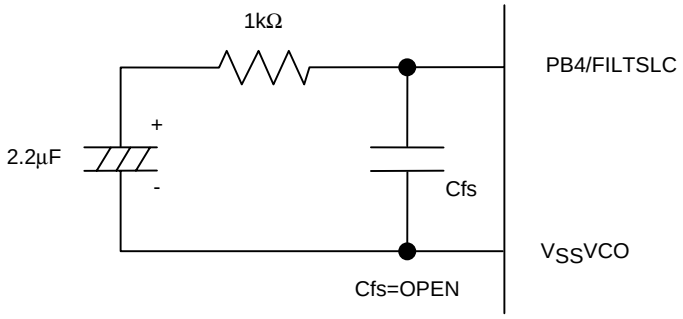


Figure 10 Recommended FILTSLC Circuit