Si5367

PRELIMINARY DATA SHEET

µP-PROGRAMMABLE PRECISION CLOCK MULTIPLIER

Description

The Si5367 is a low jitter, precision clock multiplier for applications requiring clock multiplication without jitter attenuation. The Si5367 accepts four clock inputs ranging from 10 to 707 MHz and generates five frequency-multiplied clock outputs ranging from 10 to 945 MHz and select frequencies to 1.4 GHz. The device provides virtually any frequency translation combination across this operating range. The outputs are divided down separately from a common source. The Si5367 input clock frequency and clock multiplication ratio are programmable through an I^2C or SPI interface. The Si5367 is based on Silicon Laboratories' 3rd-generation DSPLL® technology, which provides any-rate frequency synthesis in a highly integrated PLL solution that eliminates the need for external VCXO and loop filter components. The DSPLL loop bandwidth is digitally programmable, providing jitter performance optimization at the application level. Operating from a single 1.8 or 2.5 V supply, the Si5367 is ideal for providing clock multiplication in high performance timing applications.

Applications

- SONET/SDH OC-48/OC-192 line cards
- GbE/10GbE, 1/2/4/8/10GFC line cards
- ITU G.709 and custom FEC line cards
- Wireless basestations
- Data converter clocking
- xDSL
- SONET/SDH + PDH clock synthesis
- Test and measurement

Features

- Generates any frequency from 10 to 945 MHz and select frequencies to 1.4 GHz from an input frequency of 10 to 710 MHz
- Low jitter clock outputs w/jitter generation as low as 0.6 ps rms (50 kHz–80 MHz)
- Integrated loop filter with selectable loop bandwidth (30 kHz to 1.3 MHz)
- Four clock inputs w/manual or automatically controlled hitless switching
- Five clock outputs with selectable signal format (LVPECL, LVDS, CML, CMOS)
- Support for ITU G.709 FEC ratios (255/238, 255/237, 255/236)
- LOS alarm outputs
- Digitally-controlled output phase adjust
- I^2C or SPI programmable settings
- On-chip voltage regulator for 1.8 or 2.5 V ±10% operation
- Small size: 14 x 14 mm 100-pin TQFP
- Pb-free, RoHS compliant

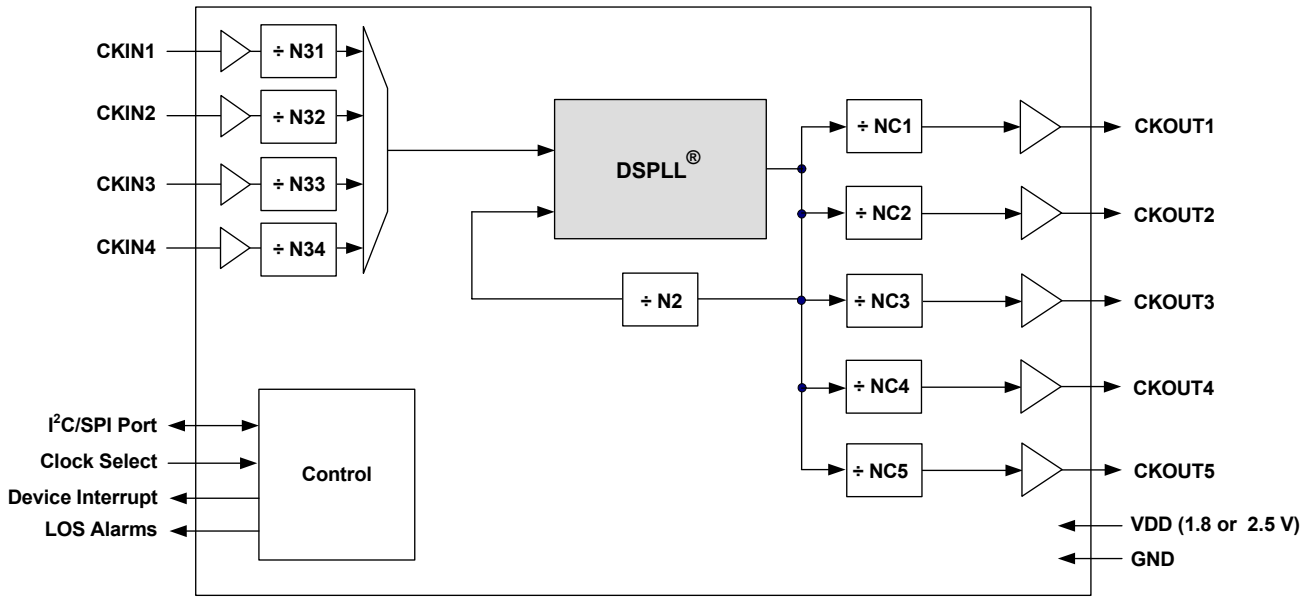


Table 1. Performance Specifications

(V_{DD} = 1.8 or 2.5 V ±10%, T_A = –40 to 85 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Temperature Range	T_A		–40	25	85	ºC
Supply Voltage	V_{DD}		2.25	2.5	2.75	V
			1.62	1.8	1.98	V
Supply Current	I_{DD}	f_{OUT} = 622.08 MHz All CKOUTs enabled LVPECL format output	—	394	435	mA
		Only CKOUT1 enabled	—	253	284	mA
		f_{OUT} = 19.44 MHz All CKOUTs enabled CMOS format output	—	278	321	mA
		Only CKOUT1 enabled	—	229	261	mA
		Tristate/Sleep Mode	—	TBD	TBD	mA
Input Clock Frequency (CKIN1, CKIN2, CKIN3, CKIN4)	CK_F	Input frequency and clock multiplication ratio determined by programming device PLL dividers. Consult Silicon Laboratories configuration software DSPLL*sim* or Any-Rate Precision Clock Family Reference Manual at www.silabs.com/timing to determine PLL divider settings for a given input frequency/clock multiplication ratio combination.	10	—	707.35	MHz
Output Clock Frequency (CKOUT1, CKOUT2, CKOUT3, CKOUT4, CKOUT5)	CK_{OF}		10 970 1213	— — —	945 1134 1417	MHz
Input Clocks (CKIN1, CKIN2, CKIN3, CKIN4)						
Differential Voltage Swing	CKN_{DPP}		0.25	—	1.9	V_{PP}
Common Mode Voltage	CKN_{VCM}	1.8 V ±10%	0.9	—	1.4	V
		2.5 V ±10%	1.0	—	1.7	V
Rise/Fall Time	CKN_{TRF}	20–80%	—	—	11	ns
Duty Cycle	CKN_{DC}	Whichever is less	40	—	60	%
			50	—		ns
Output Clocks (CKOUT1, CKOUT2, CKOUT3, CKOUT4, CKOUT5)						
Common Mode	V_{OCM}	LVPECL 100 Ω load line-to-line	V_{DD} – 1.42	—	V_{DD} – 1.25	V
Differential Output Swing	V_{OD}		1.1	—	1.9	V
Single Ended Output Swing	V_{SE}		0.5	—	0.93	V

Note: For a more comprehensive listing of device specifications, please consult the Silicon Laboratories Any-Rate Precision Clock Family Reference Manual. This document can be downloaded from www.silabs.com/timing.

Table 1. Performance Specifications (Continued)

(V_{DD} = 1.8 or 2.5 V ±10%, T_A = –40 to 85 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Rise/Fall Time	CKO_{TRF}	20–80%		230	350	ps
Duty Cycle	CKO_{DC}		45	—	55	%
PLL Performance						
Jitter Generation	J_{GEN}	f_{OUT} = 622.08 MHz, LVPECL output format 50 kHz–80 MHz	—	0.6	TBD	ps rms
		12 kHz–20 MHz	—	0.6	TBD	ps rms
		800 Hz–80 MHz	—	TBD	TBD	ps rms
Jitter Transfer	J_{PK}		—	0.05	0.1	dB
Phase Noise	CKO_{PN}	f_{OUT} = 622.08 MHz 100 Hz offset	—	TBD	TBD	dBc/Hz
		1 kHz offset	—	TBD	TBD	dBc/Hz
		10 kHz offset	—	TBD	TBD	dBc/Hz
		100 kHz offset	—	TBD	TBD	dBc/Hz
		1 MHz offset	—	TBD	TBD	dBc/Hz
Subharmonic Noise	SP_{SUBH}	Phase Noise @ 100 kHz Offset	—	TBD	TBD	dBc
Spurious Noise	SP_{SPUR}	Max spur @ n x F3 (n ≥ 1, n x F3 < 100 MHz)	—	TBD	TBD	dBc
Package						
Thermal Resistance Junction to Ambient	θ_{JA}	Still Air	—	40	—	ºC/W

Note: For a more comprehensive listing of device specifications, please consult the Silicon Laboratories Any-Rate Precision Clock Family Reference Manual. This document can be downloaded from www.silabs.com/timing.

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	–0.5 to 2.75	V
LVCMOS Input Voltage	V_{DIG}	–0.3 to (V_{DD} + 0.3)	V
Operating Junction Temperature	T_{JCT}	–55 to 150	ºC
Storage Temperature Range	T_{STG}	–55 to 150	ºC
ESD HBM Tolerance (100 pF, 1.5 kΩ)		2	kV
ESD MM Tolerance		200	V
Latch-Up Tolerance		JESD78 Compliant	

Note: Permanent device damage may occur if the Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

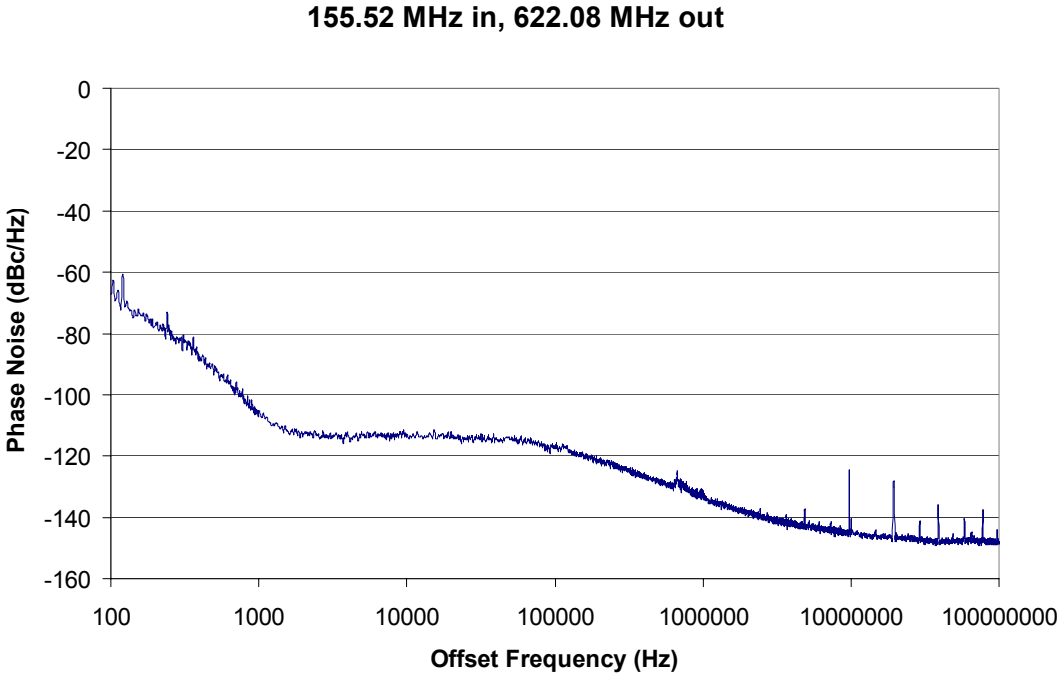
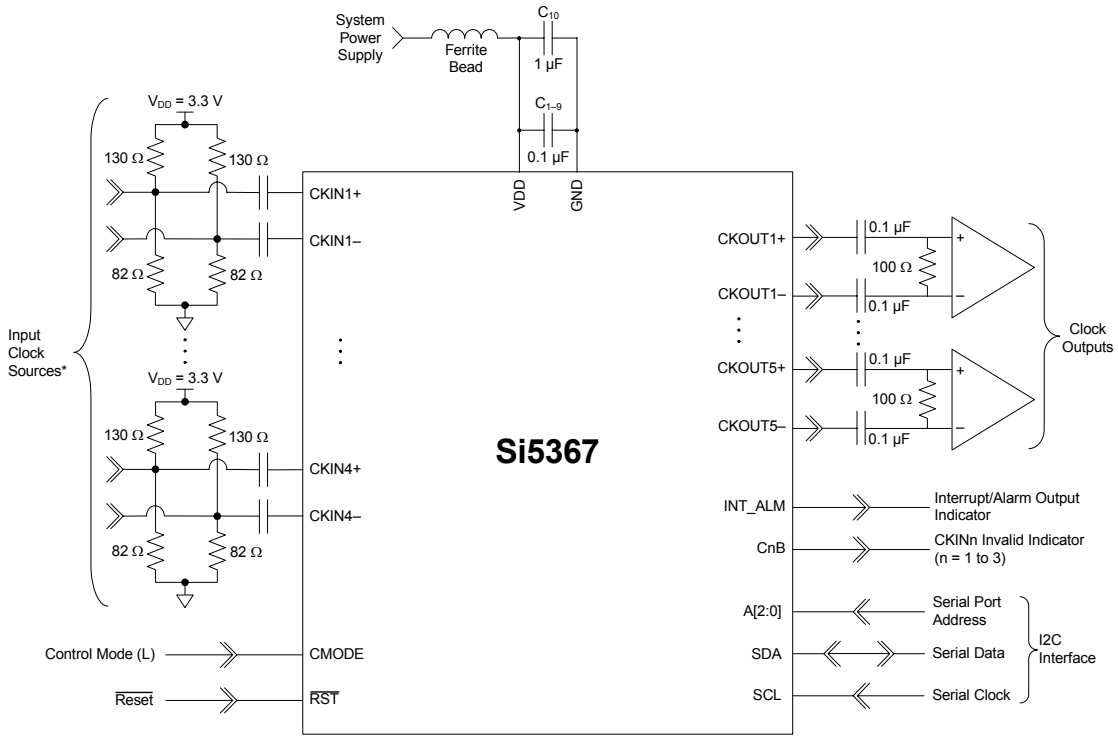
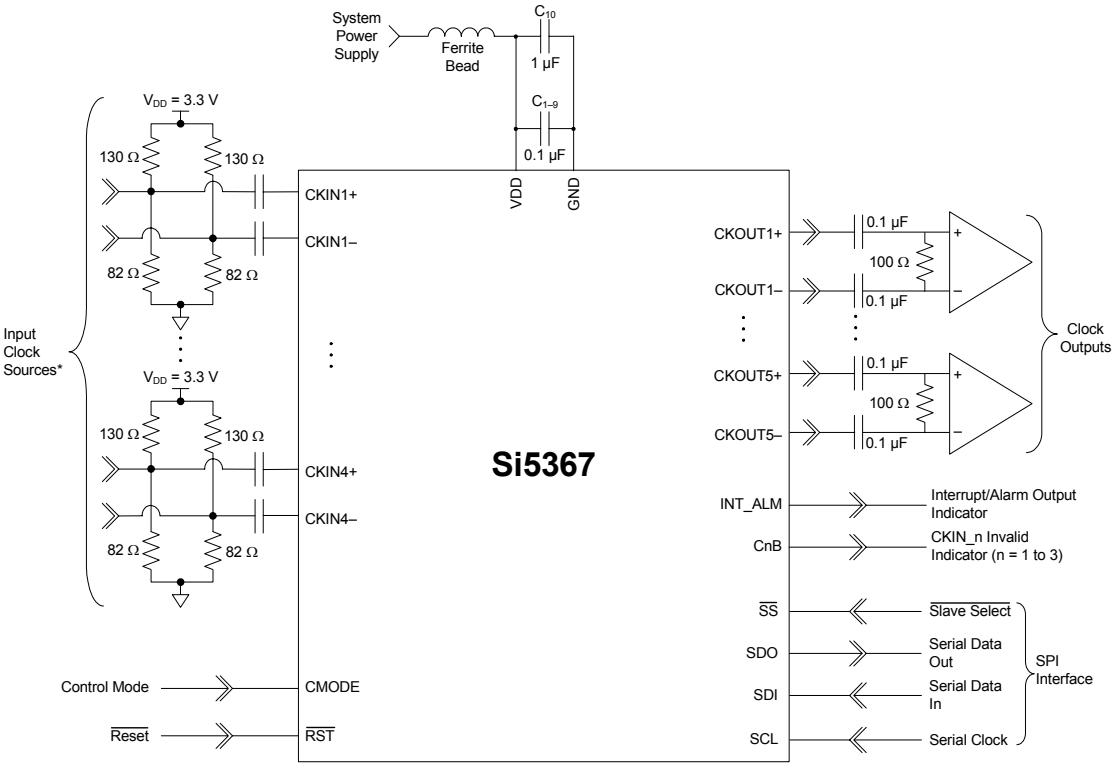


Figure 1. Typical Phase Noise Plot



***Note:** Assumes differential LVPECL termination (3.3 V) on clock inputs.

Figure 2. Si5367 Typical Application Circuit (I^2C Control Mode)



***Note:** Assumes differential LVPECL termination (3.3 V) on clock inputs.

Figure 3. Si5367 Typical Application Circuit (SPI Control Mode)

1. Functional Description

The Si5367 is a low jitter, precision clock multiplier for applications requiring clock multiplication without jitter attenuation. The Si5367 accepts four clock inputs ranging from 10 to 707 MHz and generates five frequency-multiplied clock outputs ranging from 10 to 945 MHz and select frequencies to 1.4 GHz. The device provides virtually any frequency translation combination across this operating range. Independent dividers are available for every input clock and output clock, so the Si5367 can accept input clocks at different frequencies and it can generate output clocks at different frequencies. The Si5367 input clock frequency and clock multiplication ratio are programmable through an I^2C or SPI interface. Silicon Laboratories offers a PC-based software utility, DSPLL*sim*, that can be used to determine the optimum PLL divider settings for a given input frequency/clock multiplication ratio combination that minimizes phase noise and power consumption. This utility can be downloaded from www.silabs.com/timing.

The Si5367 is based on Silicon Laboratories' 3rd-generation DSPLL® technology, which provides any-rate frequency synthesis in a highly integrated PLL solution that eliminates the need for external VCXO and loop filter components. The Si5367 PLL loop bandwidth is digitally programmable and supports a range from 30 kHz to 1.3 MHz. The DSPLL*sim* software utility can be used to calculate valid loop bandwidth settings for a given input clock frequency/clock multiplication ratio.

The Si5367 monitors all input clocks for loss-of-signal and provides a LOS alarm when it detects missing pulses on its inputs.

In the case when the input clocks enter alarm conditions, the PLL will freeze the DCO output frequency near its last value to maintain operation with an internal state close to the last valid operating state.

The Si5367 has five differential clock outputs. The signal format of the clock outputs is programmable to support LVPECL, LVDS, CML, or CMOS loads. If not required, unused clock outputs can be powered down to minimize power consumption. The phase difference between the selected input clock and the output clocks is adjustable in 200 ps increments for system skew control. In addition, the phase of each output clock may be adjusted in relation to the other output clocks. The resolution varies from 800 ps to 2.2 ns depending on the PLL divider settings. Consult the DSPLL*sim* configuration software to determine the phase offset resolution for a given input clock/clock multiplication ratio combination. For system-level debugging, a bypass mode is available which drives the output clock directly from the input clock, bypassing the internal DSPLL. The device is powered by a single 1.8 or 2.5 V supply.

1.1. Further Documentation

Consult the Silicon Laboratories Any-Rate Precision Clock Family Reference Manual (FRM) for more detailed information about the Si5367. The FRM can be downloaded from www.silabs.com/timing.

Silicon Laboratories has developed a PC-based software utility called DSPLL*sim* to simplify device configuration, including frequency planning and loop bandwidth selection. This utility can be downloaded from www.silabs.com/timing.

2. Pin Descriptions: Si5367

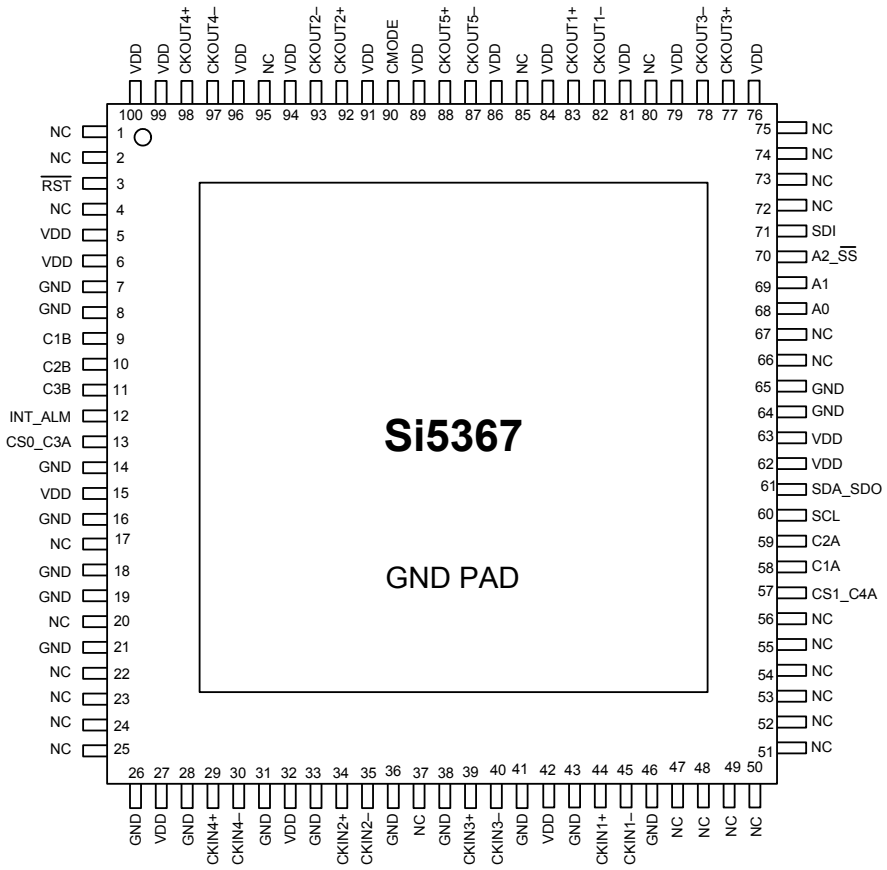


Table 3. Si5367 Pin Descriptions

Pin #	Pin Name	I/O	Signal Level	Description
1, 2, 4, 17, 20, 22, 23, 24, 25, 37, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 66, 67, 72, 73, 74, 75, 80, 85, 95	NC			**No Connect.** These pins must be left unconnected for normal operation.
3	$\overline{\text{RST}}$	I	LVCMOS	**External Reset.** Active low input that performs external hardware reset of device. Resets all internal logic to a known state and forces the device registers to their default value. Clock outputs are tristated during reset. After rising edge of $\overline{\text{RST}}$ signal, the device will perform an internal self-calibration. This pin has a weak pull-up.
Note: Internal register names are indicated by underlined italics, e.g. *INT_PIN*. See Si5368 Register Map.				

Table 3. Si5367 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Level	Description
5, 6, 15, 27, 32, 42, 62, 63, 76, 79, 81, 84, 86, 89, 91, 94, 96, 99, 100	V_{DD}	Vdd	Supply	**V_{DD}.** The device operates from a 1.8 or 2.5 V supply. Bypass capacitors should be associated with the following V_{DD} pins: Pins — Bypass Cap 5, 6 — 0.1 µF 15 — 0.1 µF 27 — 0.1 µF 62, 63 — 0.1 µF 76, 79 — 1.0 µF 81, 84 — 0.1 µF 86, 89 — 0.1 µF 91, 94 — 0.1 µF 96, 99, 100 — 0.1 µF
7, 8, 14, 16, 18, 19, 21, 26, 28, 31, 33, 36, 38, 41, 43, 46, 64, 65	GND	GND	Supply	**Ground.** This pin must be connected to system ground. Minimize the ground path impedance for optimal performance.
9	C1B	O	LVCMOS	**CKIN1 Invalid Indicator.** This pin performs the *CK1_BAD* function if *CK1_BAD_PIN* = 1 and is tristated if *CK1_BAD_PIN* = 0. Active polarity is controlled by *CK_BAD_POL*. 0 = No alarm on CKIN1. 1 = Alarm on CKIN1.
10	C2B	O	LVCMOS	**CKIN2 Invalid Indicator.** This pin performs the *CK2_BAD* function if *CK2_BAD_PIN* = 1 and is tristated if *CK2_BAD_PIN* = 0. Active polarity is controlled by *CK_BAD_POL*. 0 = No alarm on CKIN2. 1 = Alarm on CKIN2.
11	C3B	O	LVCMOS	**CKIN3 Invalid Indicator.** This pin performs the *CK3_BAD* function if *CK3_BAD_PIN* = 1 and is tristated if *CK3_BAD_PIN* = 0. Active polarity is controlled by *CK_BAD_POL*. 0 = No alarm on CKIN3. 1 = Alarm on CKIN3.
Note: Internal register names are indicated by underlined italics, e.g. *INT_PIN*. See Si5368 Register Map.				

Table 3. Si5367 Pin Descriptions (Continued)

<table>
<tr><th>Pin #</th><th>Pin Name</th><th>I/O</th><th>Signal Level</th><th>Description</th></tr>
<tr><td>12</td><td>INT_ALM</td><td>O</td><td>LVCMOS</td><td>Interrupt/Alarm Output Indicator.
This pin functions as a maskable interrupt output with active polarity controlled by the INT_POL register bit. The INT output function can be turned off by setting INT_PIN = 0. If the ALRMOUT function is desired instead on this pin, set ALRMOUT_PIN = 1 and INT_PIN = 0.
0 = ALRMOUT not active.
1 = ALRMOUT active.
The active polarity is controlled by CK_BAD_POL. If no function is selected, the pin tristates.</td></tr>
<tr><td>13
57</td><td>CS0_C3A
CS1_C4A</td><td>I/O</td><td>LVCMOS</td><td>Input Clock Select/CKIN3 or CKIN4 Active Clock Indicator.
If manual clock selection is chosen, and if CKSEL_PIN = 1, the CKSEL pins control clock selection and the CKSEL_REG bits are ignored.
<table>
<tr><th>CS[1:0]</th><th>Active Input Clock</th></tr>
<tr><td>00</td><td>CKIN1</td></tr>
<tr><td>01</td><td>CKIN2</td></tr>
<tr><td>10</td><td>CKIN3</td></tr>
<tr><td>11</td><td>CKIN4</td></tr>
</table>
If CKSEL_PIN = 0, the CKSEL_REG register bits control this function and these inputs tristate. If these pins are not functioning as the CS[1:0] inputs and auto clock selection is enabled, then they serve as the CKIN_n active clock indicator.
0 = CKIN3 (CKIN4) is not the active input clock
1 = CKIN3 (CKIN4) is currently the active input to the PLL
The CKn_ACTV_REG bit always reflects the active clock status for CKIN_n. If CKn_ACTV_PIN = 1, this status will also be reflected on the CnA pin with active polarity controlled by the CK_ACTV_POL bit. If CKn_ACTV_PIN = 0, this output tristates.
This pin has a weak pull-down.</td></tr>
<tr><td>29
30</td><td>CKIN4+
CKIN4–</td><td>I</td><td>MULTI</td><td>Clock Input 4.
Differential clock input. This input can also be driven with a single-ended signal. CKIN4 serves as the frame sync input associated with the CKIN2 clock when CK_CONFIG_REG = 1.</td></tr>
<tr><td>34
35</td><td>CKIN2+
CKIN2–</td><td>I</td><td>MULTI</td><td>Clock Input 2.
Differential input clock. This input can also be driven with a single-ended signal.</td></tr>
<tr><td colspan="5">Note: Internal register names are indicated by underlined italics, e.g. INT_PIN. See Si5368 Register Map.</td></tr>
</table>

Table 3. Si5367 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Level	Description
39 40	CKIN3+ CKIN3–	I	MULTI	**Clock Input 3.** Differential clock input. This input can also be driven with a single-ended signal. CKIN3 serves as the frame sync input associated with the CKIN1 clock when *CK_CONFIG_REG* = 1.
44 45	CKIN1+ CKIN1–	I	MULTI	**Clock Input 1.** Differential clock input. This input can also be driven with a single-ended signal.
58	C1A	O	LVCMOS	**CKIN1 Active Clock Indicator.** This pin serves as the CKIN1 active clock indicator. The *CK1_ACTV_REG* bit always reflects the active clock status for CKIN1. If *CK1_ACTV_PIN* = 1, this status will also be reflected on the C1A pin with active polarity controlled by the *CK_ACTV_POL* bit. If *CK1_ACTV_PIN* = 0, this output tristates.
59	C2A	O	LVCMOS	**CKIN2 Active Clock Indicator.** This pin serves as the CKIN2 active clock indicator. The *CK2_ACTV_REG* bit always reflects the active clock status for CKIN_2. If *CK2_ACTV_PIN* = 1, this status will also be reflected on the C2A pin with active polarity controlled by the *CK_ACTV_POL* bit. If *CK2_ACTV_PIN* = 0, this output tristates.
60	SCL	I	LVCMOS	**Serial Clock.** This pin functions as the serial port clock input for both SPI and I^2C modes. This pin has a weak pull-down.
61	SDA_SDO	I/O	LVCMOS	**Serial Data.** In I^2C microprocessor control mode (CMODE = 0), this pin functions as the bidirectional serial data port.In SPI microprocessor control mode (CMODE = 1), this pin functions as the serial data output.
68 69	A0 A1	I	LVCMOS	**Serial Port Address.** In I^2C control mode (CMODE = 0), these pins function as hardware controlled address bits. In SPI control mode (CMODE = 1), these pins are ignored. This pin has a weak pull-down.
70	A2_$\overline{SS}$	I	LVCMOS	**Serial Port Address/$\overline{\text{Slave Select}}$.** In I^2C microprocessor control mode (CMODE = 0), this pin functions as a hardware controlled address bit. In SPI microprocessor control mode (CMODE = 1), this pin functions as the slave select input. This pin has a weak pull-down.
Note: Internal register names are indicated by underlined italics, e.g. *INT_PIN*. See Si5368 Register Map.				

Table 3. Si5367 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Level	Description
71	SDI	I	LVCMOS	**Serial Data In.** In SPI microprocessor control mode (CMODE = 1), this pin functions as the serial data input. In I^2C microprocessor control mode (CMODE = 0), this pin is ignored. This pin has a weak pull-down.
77 78	CKOUT3+ CKOUT3–	O	MULTI	**Clock Output 3.** Differential clock output. Output signal format is selected by *SFOUT3_REG* register bits. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs.
82 83	CKOUT1– CKOUT1+	O	MULTI	**Clock Output 1.** Differential clock output. Output signal format is selected by *SFOUT1_REG* register bits. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs.
87 88	CKOUT5– CKOUT5+	O	MULTI	**Clock Output 5.** Differential clock output. Output signal format is selected by *SFOUT5_REG* register bits. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs.
90	CMODE	I	3-Level	**Control Mode.** Selects I^2C or SPI control mode for the device. 0 = I^2C Control Mode. 1 = SPI Control Mode.
92 93	CKOUT2+ CKOUT2–	O	MULTI	**Clock Output 2.** Differential clock output. Output signal format is selected by *SFOUT2_REG* register bits. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs.
97 98	CKOUT4– CKOUT4+	O	MULTI	**Clock Output 4.** Differential clock output. Output signal format is selected by *SFOUT4_REG* register bits. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs.
GND PAD	GND PAD	GND	Supply	**Ground Pad.** The ground pad must provide a low thermal and electrical impedance to a ground plane.

Note: Internal register names are indicated by underlined italics, e.g. *INT_PIN*. See Si5368 Register Map.

3. Ordering Guide

Ordering Part Number	Output Clock Frequency Range	Package	Temperature Range
Si5367A-B-GQ	10–945 MHz 970–1134 MHz 1.213–1.417 GHz	100-Pin 14 x 14 mm TQFP	–40 to 85 °C
Si5367B-B-GQ	10–808 MHz	100-Pin 14 x 14 mm TQFP	–40 to 85 °C
Si5367C-B-GQ	10–346 MHz	100-Pin 14 x 14 mm TQFP	–40 to 85 °C

4. Package Outline: 100-Pin TQFP

Figure 4 illustrates the package details for the Si5367. Table 4 lists the values for the dimensions shown in the illustration.

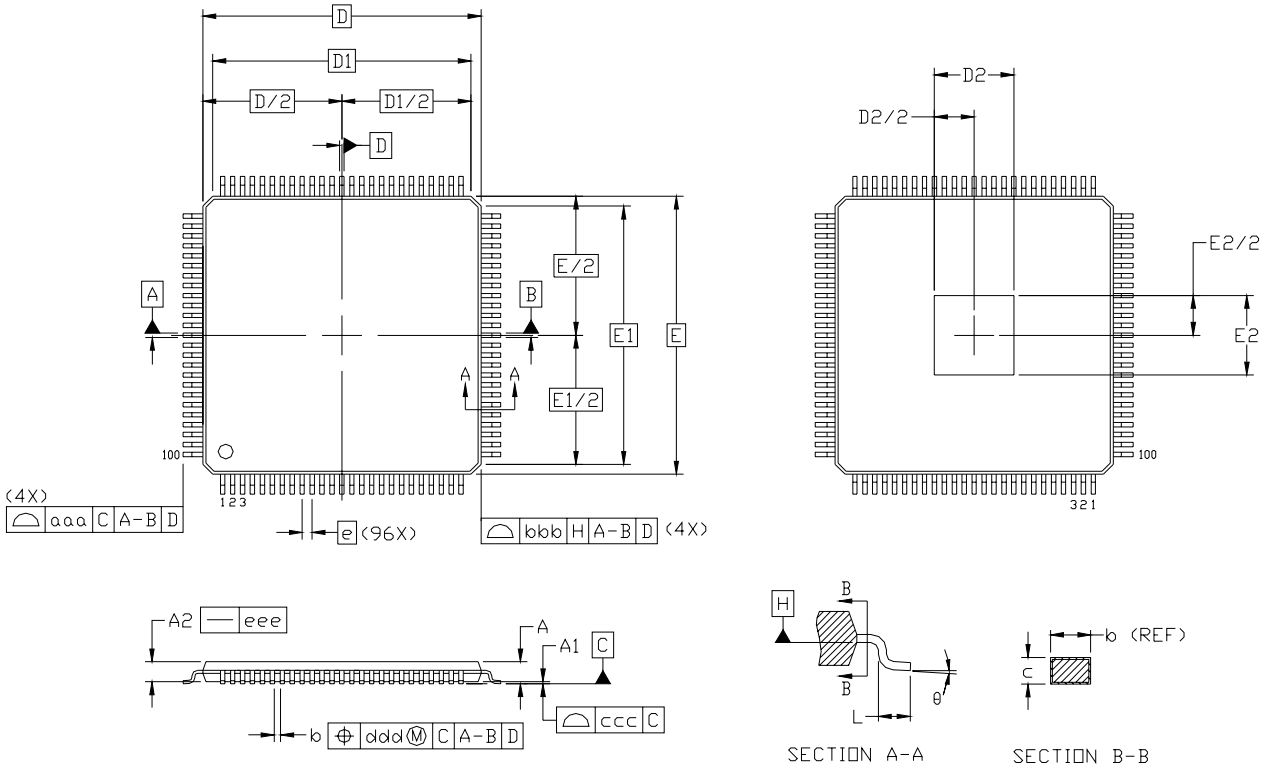


Figure 4. 100-Pin Thin Quad Flat Package (TQFP)

Table 4. 100-Pin Package Diagram Dimensions

Dimension	Min	Nom	Max
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
c	0.09	—	0.20
D	16.00 BSC.		
D1	14.00 BSC.		
D2	3.85	4.00	4.15
e	0.50 BSC.		

Dimension	Min	Nom	Max
E	16.00 BSC.		
E1	14.00 BSC.		
E2	3.85	4.00	4.15
L	0.45	0.60	0.75
aaa	—	—	0.20
bbb	—	—	0.20
ccc	—	—	0.08
ddd	—	—	0.08
θ	0º	3.5º	7º

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This package outline conforms to JEDEC MS-026, variant AED-HD.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

5. Recommended PCB Layout

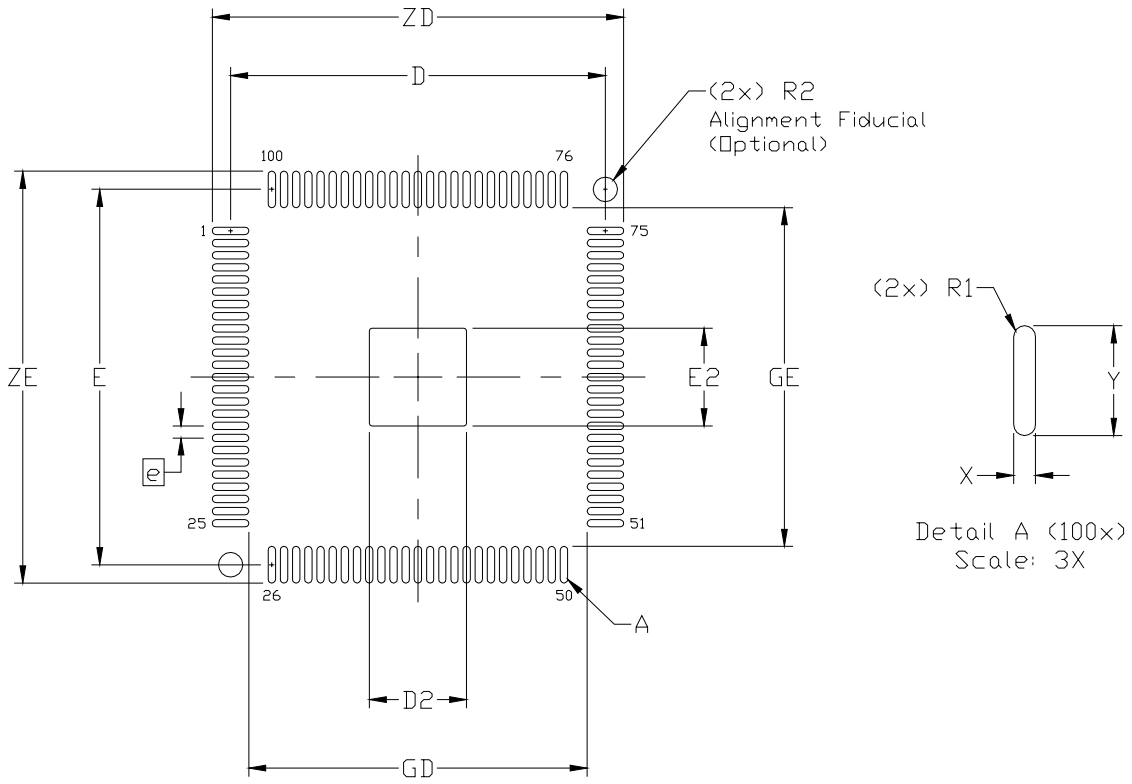


Figure 5. PCB Land Pattern Diagram

Table 5. PCB Land Pattern Dimensions

Dimension	MIN	MAX
e	0.50 BSC.	
E	15.40 REF.	
D	15.40 REF.	
E2	3.90	4.10
D2	3.90	4.10
GE	13.90	—
GD	13.90	—
X	—	0.30
Y	1.50 REF.	
ZE	—	16.90
ZD	—	16.90
R1	0.15 REF	
R2	—	1.00

Notes (General):

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Notes (Solder Mask Design):

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Notes (Stencil Design):

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads.
4. A 4 x 4 array of 0.80 mm square openings on 1.05 mm pitch should be used for the center ground pad.

Notes (Card Assembly):

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

DOCUMENT CHANGE LIST

Revision 0.1 to Revision 0.2

- Changed LVTTL to LVCMOS in Table 2, “Absolute Maximum Ratings,” on page 3.
- Updated “2. Pin Descriptions: Si5367”.
  - Changed FSOUT (pins 87 and 88) to CLKOUT5.
  - Changed FS_ALIGN (pin 21) control pin to GND.
  - Changed pin 16 to ground.

Revision 0.2 to Revision 0.3

- Removed references to latency control, INC, and DEC pins.
- Updated block diagram on page 1.
- Added Figure 1, “Typical Phase Noise Plot,” on page 4.
- Updated “2. Pin Descriptions: Si5367”.
  - Changed font of register names to *underlined italics*.
- Updated "3. Ordering Guide" on page 12.
- Added “5. Recommended PCB Layout”.

NOTES:

CONTACT INFORMATION

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