



UT2327

Power MOSFET

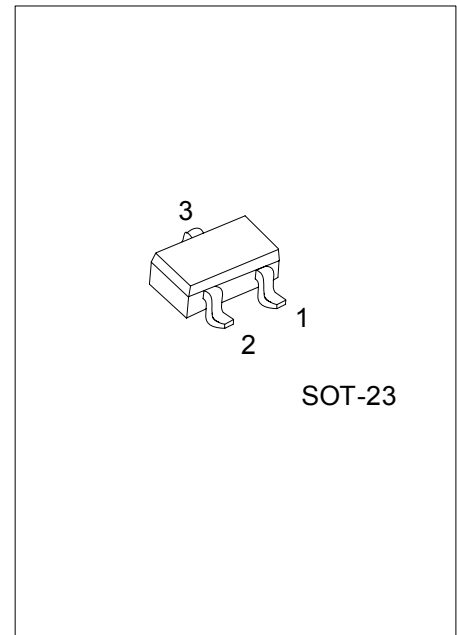
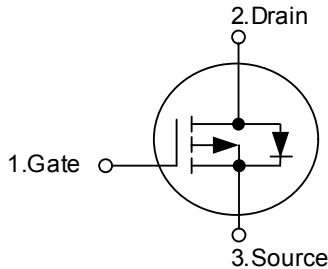
P-CHANNEL ENHANCEMENT MODE

■ DESCRIPTION

The UTC **UT2327L** is P-channel enhancement mode Power MOSFET, designed in serried ranks. with fast switching speed, low on-resistance, favorable stabilization.

Used in commercial and industrial surface mount applications and suited for low voltage applications such as DC/DC converters.

■ SYMBOL



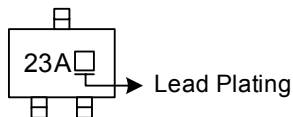
*Pb-free plating product number: UT2327L

■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Normal	Lead Free Plating		1	2	3	
UT2327-AE3-R	UT2327L-AE3-R	SOT-23	S	G	D	Tape Reel

<p>UT2327L-AE3-R</p> <p>(1)Packing Type</p> <p>(2)Package Type</p> <p>(3)Lead Plating</p>	<p>(1) R: Tape Reel</p> <p>(2) AE3: SOT-23</p> <p>(3) L: Lead Free Plating, Blank: Pb/Sn</p>
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■ MARKING



■ ABSOLUTE MAXIMUM RATINGS (Ta = 25 , unless otherwise specified)

PARAMETER	SYMBOL	RATING	UNITS	
Drain-Source Voltage	V _{DS}	- 20	V	
Gate-Source Voltage	V _{GS}	± 12	V	
Continuous Drain Current (Note 3)	I _D	Ta=25	-2.6	A
		Ta=70	-2.1	A
Pulsed Drain Current (Note 1, 2)	I _{DM}	-10	A	
Total Power Dissipation (Ta=25)	P _D	1.38	W	
Junction Temperature	T _J	+150		
Storage Temperature	T _{STG}	-55 ~ +150		

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Junction to Ambient (Note 3)	θ _{JA}			90	/W

■ ELECTRICAL CHARACTERISTICS (T_J=25 , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =-250uA	-20			V
Drain-Source Leakage Current	I _{DSS}	T _J =25			-1	uA
		T _J =70	V _{DS} =-20V, V _{GS} =0V			-10
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±12V			±100	nA
Breakdown Voltage Temperature Coefficient	ΔBV _{DSS} /ΔT _J	Reference to 25 , I _D =-1mA		-0.1		V/
ON CHARACTERISTICS						
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} =V _{GS} , I _D =-250uA	-0.5			V
Drain-Source On-State Resistance (Note 2)	R _{DS(ON)}	V _{GS} =-5V, I _D =-2.8A			130	mΩ
		V _{GS} =-2.8V, I _D =-2.0A			190	mΩ
Forward Transconductance	g _{FS}	V _{DS} =-5V, I _D =-2.8A		4.4		S
DYNAMIC CHARACTERISTICS						
Input Capacitance	C _{ISS}	V _{GS} =0V, V _{DS} =-6V, f=1.0MHz		295		pF
Output Capacitance	C _{OSS}			170		pF
Reverse Transfer Capacitance	C _{RSS}			65		pF
SWITCHING CHARACTERISTICS						
Turn-ON Delay Time (Note 2)	t _{D(ON)}	V _{DS} =-15V, V _{GS} =-10V, I _D =-1A, R _G =6Ω, R _D =15Ω		5.2		ns
Turn-ON Rise Time	t _R			9.7		ns
Turn-OFF Delay Time	t _{D(OFF)}			19		ns
Turn-OFF Fall Time	t _F			29		ns
Total Gate Charge (Note 2)	Q _G	V _{DS} =-6V, V _{GS} =-5V, I _D =-2.8A		5.2	10	nC
Gate-Source Charge	Q _{GS}			1.36		nC
Gate-Drain Charge	Q _{GD}			0.6		nC
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Drain-Source Diode Forward Voltage(Note2)	V _{SD}	T _J =25 , I _S =-1.6A, V _{GS} =0V			-1.2	V
Maximum Continuous Drain-Source Diode Forward Current	I _S	V _D =V _G =0V, V _S =-1.2V			-1	A
Maximum Pulsed Drain-Source Diode Forward Current (Note 1)	I _{SM}				-10	A

Notes: 1. Pulse width limited by T_{J(MAX)}

2. Pulse width ≤300us, duty cycle ≤2%.

3. Surface mounted on 1 in² copper pad of FR4 board; 270 /W when mounted on min.

■ TYPICAL CHARACTERISTICS

Fig 1. Typical Output Characteristics

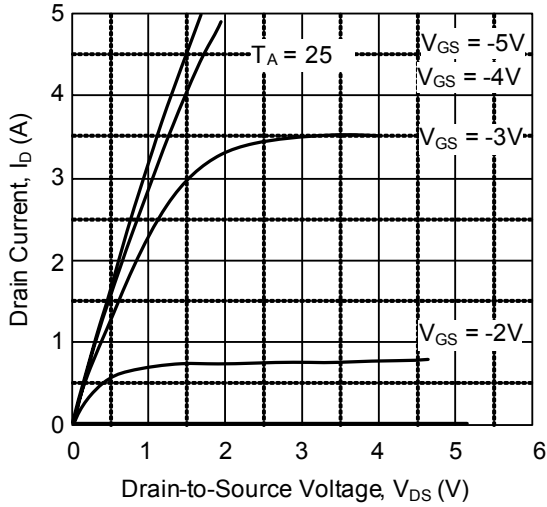


Fig 2. Typical Output Characteristics

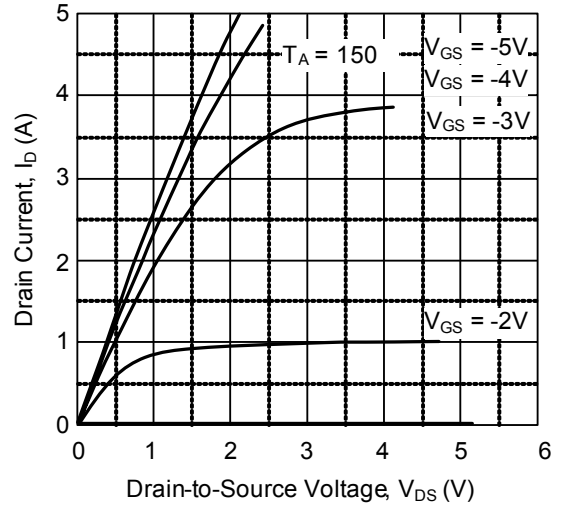


Fig 3. On-Resistance vs. Gate Voltage

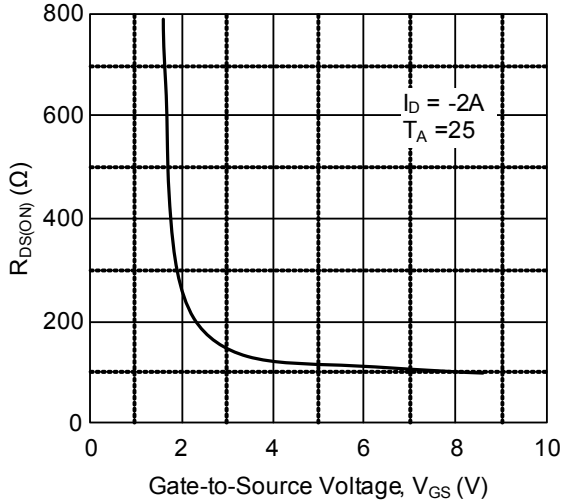


Fig 4. Normalized On-Resistance

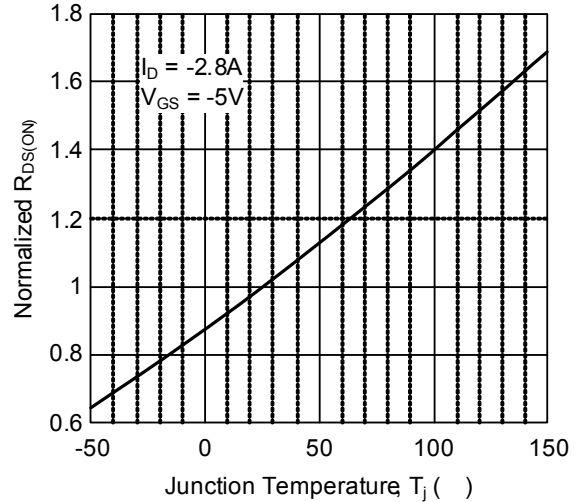


Fig 5. Forward Characteristic of Reverse Diode

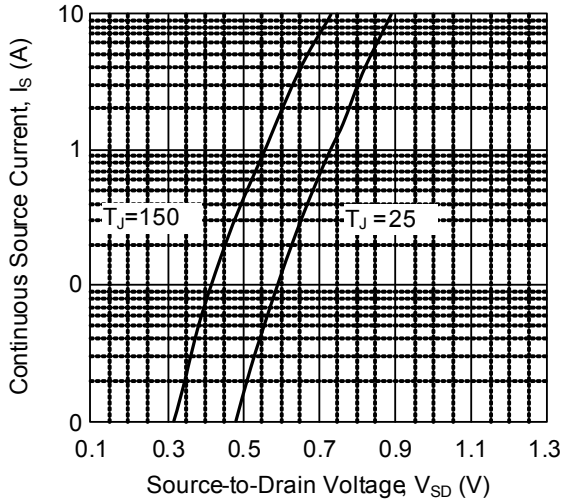
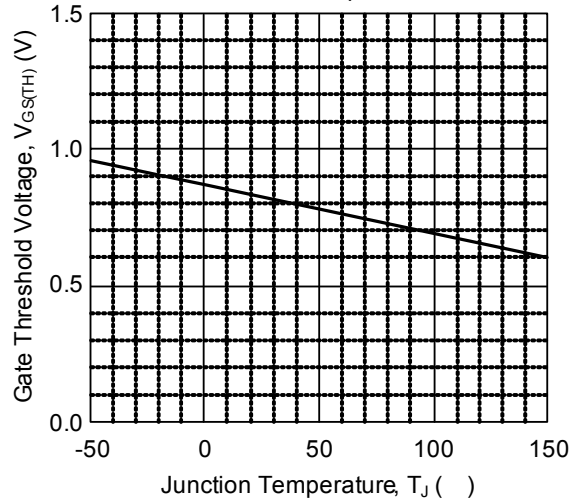


Fig 6. Gate Threshold Voltage vs Junction Temperature



■ TYPICAL CHARACTERISTICS(Cont.)

Fig 7. Gate Charge Characteristics

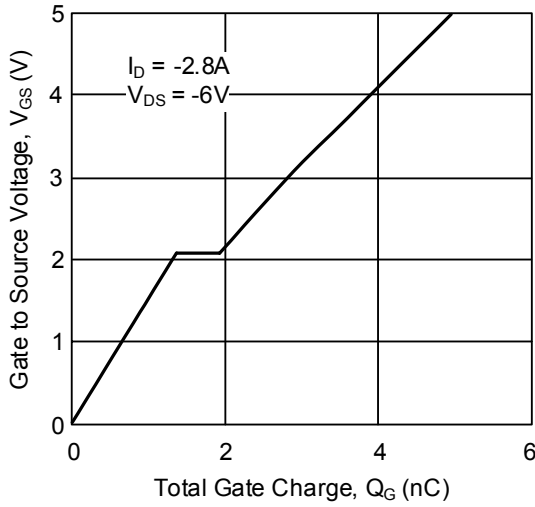


Fig 8. Typical Capacitance Characteristics

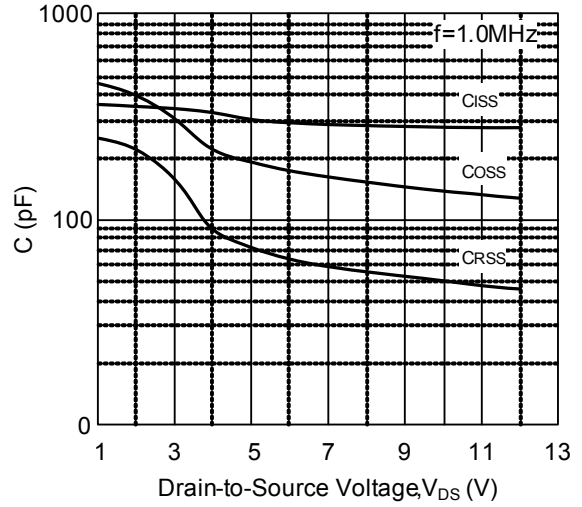


Fig 9. Maximum Safe Operating Area

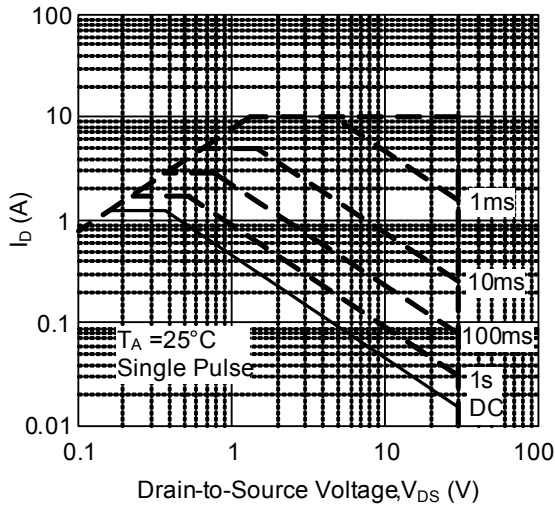


Fig 10. Effective Transient Thermal Impedance

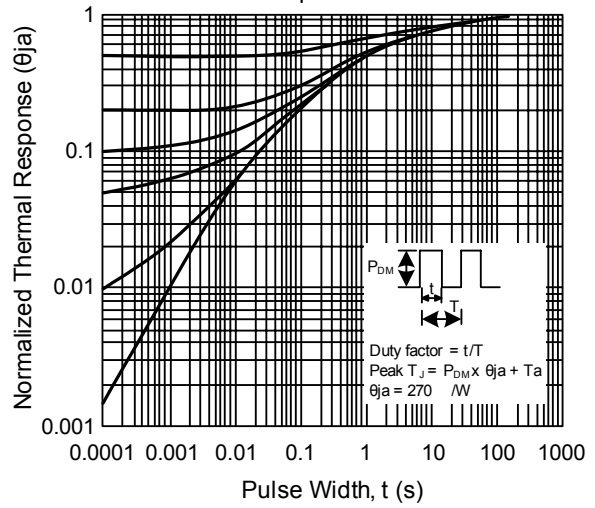


Fig 11. Switching Time Waveform

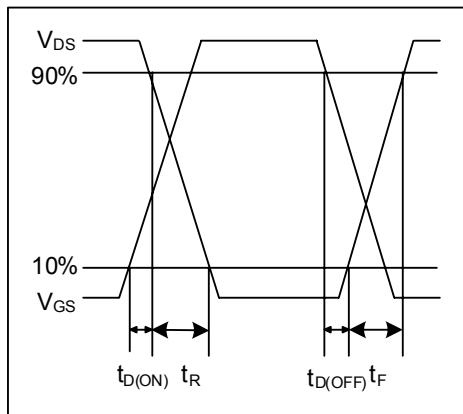
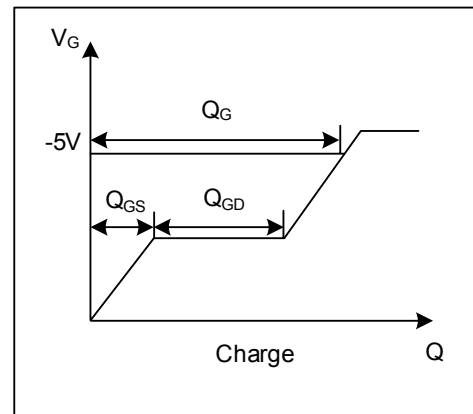


Fig 12. Gate Charge Waveform



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