# PERICOM®

# PI74LVTCH16245

## 3.3V 16-Bit Bi-Directional Transceiver with 3-State Outputs

## Product Features

· Advanced low power CMOS design for 2.7V to 3.6V Vcc operation

· Supports 5V input/output tolerance in mixed signal mode operation

· Function compatible with LVT family of products

· Balanced ±24mA output drive

· Typical $V_{OLP}$ (Output Ground Bounce) < 0.8V at $V_{CC}$=3.3V, $T_A$=25°C

· $I_{off}$ and Power Up/Down 3-State support live insertion

· Bus Hold on data inputs eliminates the need for external pull-up/down resistors

· Latch-up performance exceeds 200mA Per JESD78

· ESD protection exceeds JESD 22
  – 2000V Human-Body Model (A114-B)
  – 200V Machine Model (A115-A)

· Industrial Temperature: –40°C to +85°C

· Packaging (Pb-free & Green available):
  – 48-pin 240-mil wide plastic TSSOP (A)

## Product Description

The PI74LVTCH16245 is a non-inverting 16-bit Bidirectional Transceiver designed for low-voltage 2.7V to 3.6V $V_{CC}$ operation, with the capability of interfacing to the 5V system environment. This tranceiver is designed for asynchronous two-way communication between data buses. The direction control input pin (xDIR) determines the direction of the data flow through the bidirectional transceiver. The Direction and Output Enable controls are designed to operate this device as either two independent 8-bit tranceivers or one 16-bit transceiver. The output enable (x$\overline{OE}$) input, when HIGH, disables both A and B ports by placing them in HIGH Z condition.

The PI74LVTCH16245 has "Bus Hold" which retains the data input's last valid logic state whenever the data input goes to high-impedance, preventing "floating" inputs and eliminating the need for pull-up/down resistors.

When $V_{CC}$ is between 0 to 1.5V during power up or power down, the outputs of the device are in the high-impedance state. To ensure the high-impedance state above 1.5V, $\overline{OE}$ should be tied to Vcc through a pullup resistor; the minimum value of the resistor is determined by the current sinking capability of the driver.

The device fully supports live-insertion with its $I_{off}$ and power-up/down 3-state. The $I_{off}$ circuitry disables the outputs when the power is off, preventing the backflow of damaging current through the device. Power-up/down 3-state places the outputs in the high-impedance state during power up or power down, preventing driver conflict.

## Logic Block Diagram
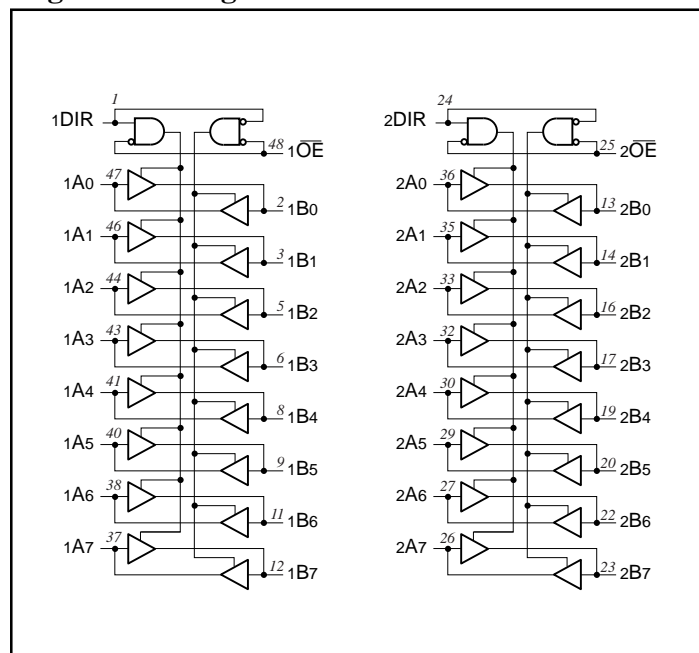
## Maximum Ratings

(Above which the useful life may be impaired.
For user guidelines, not tested.)

| | |
|---|---|
| Supply voltage range, $V_{CC}$ .............................. | $-0.5V$ to $+6.5V$ |
| Input voltage range, $V_I$[1] .............................. | $-0.5V$ to $+6.5V$ |
| Voltage range applied to any output in the high-impedance or power-off state, $V_O$[1] ....... | $-0.5V$ to $+6.5V$ |
| Voltage range applied to any output in the active state, $V_O$[1,2] .............................. | $-0.5V$ to $V_{CC}+0.5V$ |
| Input clamp current, $I_{IK}$ ($V_I < 0$) .................................... | $-50mA$ |
| Output clamp current, $I_{OK}$ ($V_O < 0$) .............................. | $-50mA$ |
| Continous Output Current $I_O$ ....................................... | $\pm 50mA$ |
| Continous Current through each VCC or GND pin .............. | $\pm 100mA$ |
| Package thermal impedance, $\theta_{JA}$[3] ................................. | $104°C/W$ |
| Storage Temperature range, $T_{stg}$ ..................... | $-65°C$ to $150°C$ |

**Notes:**

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

1. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.
2. This value is limited to 6.5V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51.

## Truth Table[1]

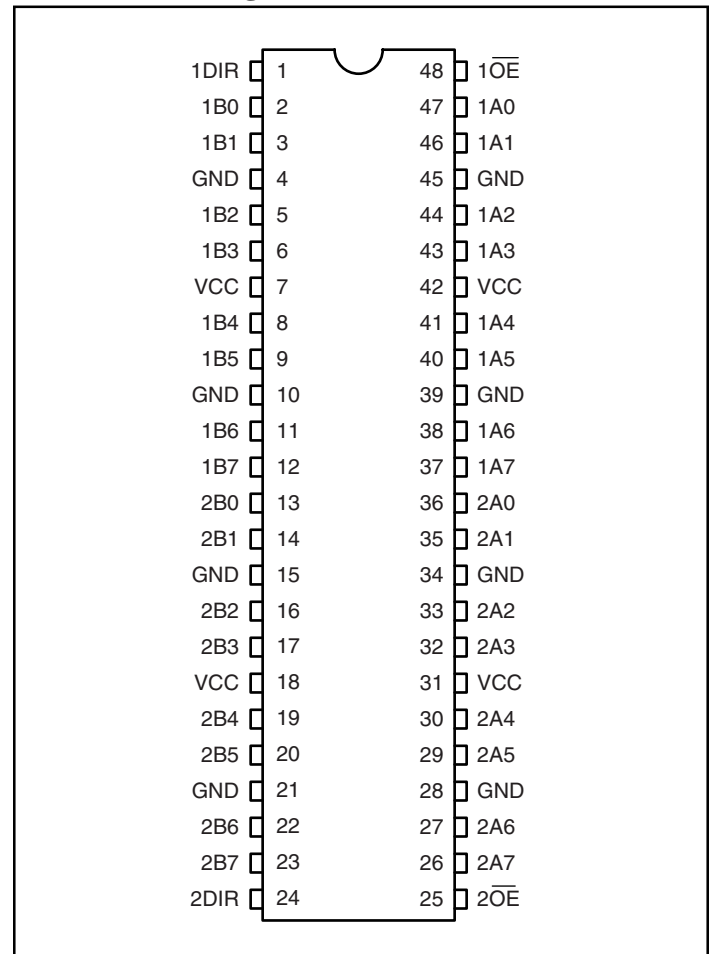| Inputs | | Outputs |
|---|---|---|
| $x\overline{OE}$ | xDIR | |
| L | L | Bus B Data to Bus A |
| L | H | Bus A Data to Bus B |
| H | X | Z |

**Notes:**
1. H = High Signal Level
   L = Low Signal Level
   X = Don't Care or Irrelevant
   Z = High Impedance

## Product Pin Description

| Pin Name | Description |
|---|---|
| $x\overline{OE}$ | 3-State Output Enable Inputs (Active LOW) |
| xDIR | Direction Control Inputs (Active HIGH) |
| xAx | Side A Inputs or 3-State Outputs |
| xBx | Side B Inputs or 3-State Outputs |
| GND | Ground |
| $V_{CC}$ | Power |

## Product Pin Configuration

| | | | |
|---|---|---|---|
| 1DIR | 1 | 48 | 1$\overline{OE}$ |
| 1B0 | 2 | 47 | 1A0 |
| 1B1 | 3 | 46 | 1A1 |
| GND | 4 | 45 | GND |
| 1B2 | 5 | 44 | 1A2 |
| 1B3 | 6 | 43 | 1A3 |
| VCC | 7 | 42 | VCC |
| 1B4 | 8 | 41 | 1A4 |
| 1B5 | 9 | 40 | 1A5 |
| GND | 10 | 39 | GND |
| 1B6 | 11 | 38 | 1A6 |
| 1B7 | 12 | 37 | 1A7 |
| 2B0 | 13 | 36 | 2A0 |
| 2B1 | 14 | 35 | 2A1 |
| GND | 15 | 34 | GND |
| 2B2 | 16 | 33 | 2A2 |
| 2B3 | 17 | 32 | 2A3 |
| VCC | 18 | 31 | VCC |
| 2B4 | 19 | 30 | 2A4 |
| 2B5 | 20 | 29 | 2A5 |
| GND | 21 | 28 | GND |
| 2B6 | 22 | 27 | 2A6 |
| 2B7 | 23 | 26 | 2A7 |
| 2DIR | 24 | 25 | 2$\overline{OE}$ |

## Recommended Operating Conditions[(1)]

| | | Min. | Max. | Units |
|---|---|---|---|---|
| $V_{CC}$     Supply Voltage | Operating | 2.7 | 3.6 | |
| $V_{IH}$     High-level Input Voltage | $V_{CC}$ = 2.7V to 3.6V | 2.0 | | |
| $V_{IL}$     Low-level Input Voltage | $V_{CC}$ = 2.7V to 3.6V | | 0.8 | |
| $V_I$     Input Voltage | | 0 | 5.5 | V |
| $V_O$     Output Voltage | High or Low State | 0 | $V_{CC}$ | |
| | 3-State | 0 | 5.5 | |
| $I_{OH}$ High-level output current | $V_{CC}$ = 2.7V | | − 12 | |
| | $V_{CC}$ = 3.0V to 3.6V | | − 24 | |
| $I_{OL}$ Low-level output current | $V_{CC}$ = 2.7V | | 12 | mA |
| | $V_{CC}$ = 3.0V to 3.6V | | 24 | |
| $\Delta t/\Delta v$    Input transition rise or fall rate | | | 10 | ns/V |
| $\Delta t/\Delta V_{CC}$   Power-up ramp rate | | 150 | | μs/V |
| $T_A$     Operating free-air temperature | | − 40 | +85 | °C |

**Notes:**
1. All unused inputs must be held at $V_{CC}$ or GND to ensure proper device operation.

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## DC Electrical Characteristics (Over the Operating Range, $T_A = -40°C$ to $+85°C$)

| Parameters | Description | | Test Conditions | | Min. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{IK}$ | Clamp Diode Voltage | | $V_{CC} = 2.7V$ | $I_I = -18mA$ | | $-1.2V$ | V |
| $V_{OH}$ | Output High Voltage | | $V_{CC} = 2.7V$ to $3.6V$ | $I_{OH} = -100\mu A$ | $V_{CC} -0.2V$ | | |
| | | | $V_{CC} = 2.7V$ | $I_{OH} = -12mA$ | 2.2 | | |
| | | | $V_{CC} = 3V$ | $I_{OH} = -12mA$ | 2.4 | | |
| | | | | $I_{OH} = -24mA$ | 2.2 | | |
| $V_{OL}$ | Output Low Voltage | | $V_{CC} = 2.7V$ to $3.6V$ | $I_{OL} = 100\mu A$ | | 0.2 | |
| | | | $V_{CC} = 2.7V$ | $I_{OL} = 12mA$ | | 0.4 | |
| | | | $V_{CC} = 3V$ | $I_{OL} = 12mA$ | | 0.4 | |
| | | | | $I_{OL} = 24mA$ | | 0.55 | |
| $I_I$ | Input Leakage Current | Control Inputs | $V_{CC} = 0V$ to $3.6V$ | $V_I = 0V$ to $5.5V$ | | $\pm 5$ | $\mu A$ |
| | | A or B Ports [1] | $V_{CC} = 3.6V$ | $V_I = 5.5V$ | | $\pm 5$ | |
| | | | | $V_I = V_{CC}$ | | | |
| | | | | $V_I = GND$ | | | |
| $I_{I(HOLD)}$ | Data Input Hold Current (A or B ports) | | $V_{CC} = 3V$ | $V_I = 0.8V$ | 75 | | |
| | | | | $V_I = 2V$ | $-75$ | | |
| | | | $V_{CC} = 3.6V$ [2] | $V_I = 0$ to $3.6V$ | | $\pm 500$ | |
| $I_{OFF}$ | Power Off Output Leakage Current | | $V_{CC} = 0V$ | $V_I$ or $V_O = 0V$ to $5.5V$ | | $\pm 5$ | |
| $I_{OZPU}$ | Power-Up 3-State Current | | $V_{CC} = 0V$ to $1.5V$ | $V_O = 0.5V$ to $5.5V$, OE = don't care | | $\pm 5$ | |
| $I_{OZPD}$ | Power-Down 3-State Current | | $V_{CC} = 1.5V$ to $0V$ | $V_O = 0.5V$ to $5.5V$, OE = don't care | | $\pm 5$ | |
| $I_{CC}$ | Quiescent Power Supply Current | | $V_{CC} = 2.7V$ to $3.6V$ | $V_I = V_{CC}$ or GND     $I_O = 0$ | | 60 | |
| | | | | $3.6V \le V_I \le 5.5V$ [3] | | | |
| $\Delta I_{CC}$ | Increase in $I_{CC}$ | | $V_{CC} = 2.7V$ to $3.6V$ | One input at $V_{CC} - 0.6V$ [4] Other inputs at $V_{CC}$ or GND | | 500 | |

**Notes:**
1. For I/O ports, Input Leakage Current ($I_I$) includes the 3-state Output Leakage Current. Unused pins are at $V_{CC}$ or GND.
2. This is the maximum bus-hold dynamic current. It is the minimum overdrive current required to switch the input from one state to another.
3. This applies in the diabled stae only.
4. This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.

## Capacitance

| Parameters | Description | Test Conditions | Typ.[1] | Units |
|---|---|---|---|---|
| $C_I$ | Control Input Capacitance | $V_{CC} = 3.3V$, $V_I = V_{CC}$ or GND | 3.4 | pF |
| $C_{IO}$ | Output/Capacitance | $V_{CC} = 3.3V$, $V_O = V_{CC}$ or GND | 8 | |
| $C_{PD}$ | Power Dissipation Capacitance [2] | $V_{CC} = 3.3V$, $V_I = 0V$ or $V_{CC}$, f =10 MHz | 23 | |

**Notes:**

1. All typical values are measured at $V_{CC} = 3.3V$, $T_A = 25°C$.
2. $C_{PD}$ is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption ($I_{CCD}$) at no output loading, and operating at 50% duty cycle, $C_{PD}$ is related to $I_{CCD}$ dynamic operating current by the expression: $I_{CCD} = (C_{PD})(V_{CC})(f_{IN}) + (I_{CC}static)$

## Switching Characteristics Over Operating Range

| Parameters | Description | From (Input) | To (Output) | $V_{CC} = 3.3V \pm 0.3V$ $C_L = 50pF$, $R_L = 500$-ohm | | | $V_{CC} = 2.7V$ $C_L = 50pF$, $R_L = 500$-ohm | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ.[1] | Max. | Min. | Max. | |
| $t_{PLH}$ | Propagation Delay | A or B | B or A | 1.0 | 2.5 | 3.5 | | 3.9 | ns |
| $t_{PHL}$ | | | | 1.0 | 2.5 | 3.5 | | 3.9 | |
| $t_{PZH}$ | Output Enable Time | $\overline{OE}$ | A or B | 1.0 | 2.8 | 4.9 | | 5.3 | |
| $t_{PZL}$ | | | | 1.0 | 2.8 | 4.9 | | 5.3 | |
| $t_{PHZ}$ | Output Disable Time | $\overline{OE}$ | A or B | 1.0 | 2.7 | 4.3 | | 4.8 | |
| $t_{PLZ}$ | | | | 1.0 | 2.6 | 4.3 | | 4.8 | |
| $t_{SK(O)}$ | Output to Output Skew[2] | | | | | 0.5 | | | |

**Notes:**

1. All typical values are measured at $V_{CC} = 3.3V$, $T_A = 25°C$.
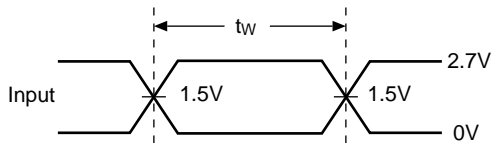2. Skew between any two outputs, switching in the same direction.

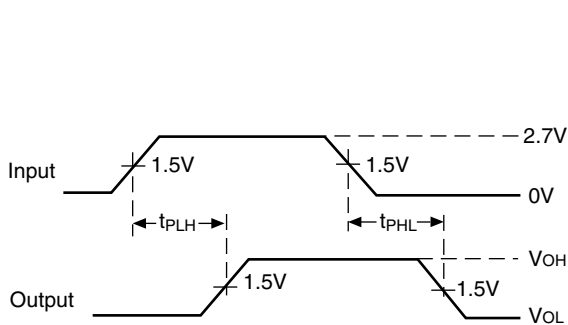## PARAMETER MEASUREMENT INFORMATION
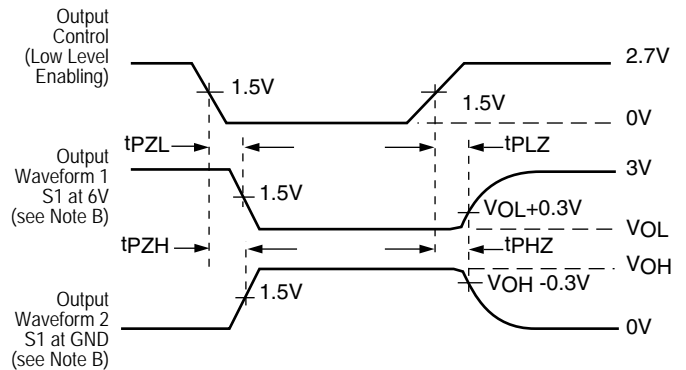### $V_{CC} = 2.7V$ and $3.3V \pm 0.3V$
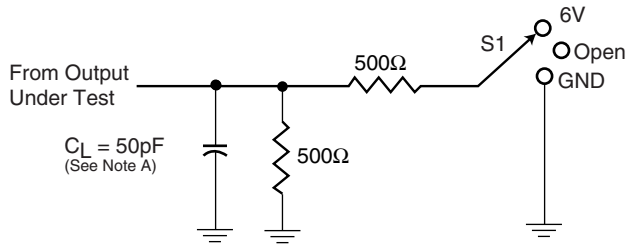
**Load Circuit**

| Test | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 6V |
| $t_{PHZ}/t_{PZH}$ | GND |

**Voltage Waveforms**
**Pulse Duration**

**Voltage Waveforms**
**Propagation Delay Times**

**Voltage Waveforms**
**Enable and Disable Times**

**Figure 1. Load Circuit and Voltage Waveforms**

**Notes:**

A.  $C_L$ includes probe and jig capacitance.

B.  Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
    Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

•  All input impulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50\Omega$, $t_R \leq 2.5$ns, $t_F \leq 2.5$ns.

•  The outputs are measured one at a time with one transition per measurement.

**48-pin TSSOP (A) Package**
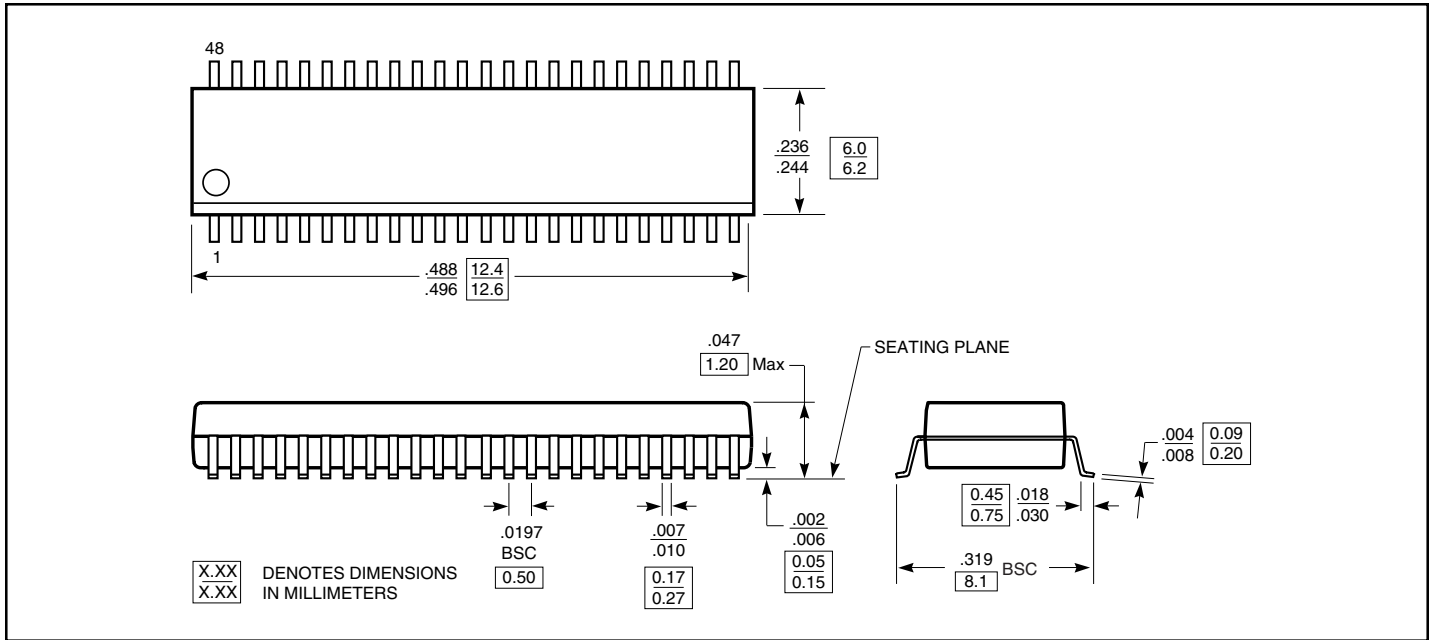


## Ordering Information

| Ordering Data | Packaging Code | Packaging Type |
|---|---|---|
| PI74LVTCH16245A | A | 48-pin, 240-mil wide plastic TSSOP |
| PI74LVTCH16245AE | A | Pb-free & Green, 48-pin, 240-mil wide plastic TSSOP |

**Notes:**

• Thermal characteristics can be found on the company web site at www.pericom.com/packaging/

• E = Pb-free & Green

• Adding an X suffix = Tape/Reel