FAIRCHILD

SEMICONDUCTOR®

September 2007

UniFET™

# FDP80N06
N-Channel MOSFET
60V, 80A, 10mΩ

Features

- $R_{DS(on)}$ = 8.5mΩ (Typ.)@ V_{GS} = 10V, I_D = 40A
- Low gate charge(Typ. 57nC)
- Low C_{rss}(Typ. 145pF)
- Fast switching
- Improved dv/dt capability
- RoHS compliant

Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pluse in the avalanche and commutation mode. These devices are well suited for high efficient switched mode power supplies,active power factor correction, electronic lamp ballast based on half bridge topology.

100% LEAD-FREE IMPLEMENTATION

TO-220

G D S
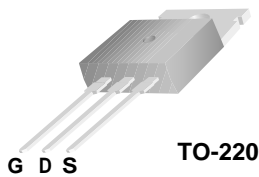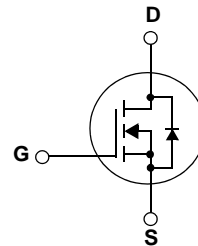
MOSFET Maximum Ratings T_C = 25°C unless otherwise noted*

Symbol	Parameter			Ratings	Units
V_{DSS}	Drain to Source Voltage			60	V
V_{GSS}	Gate to Source Voltage			±20	V
I_D	Drain Current	-Continuous (T_C = 25°C)		80	A
		-Continuous (T_C = 100°C)		65	
I_{DM}	Drain Current	- Pulsed	(Note 1)	320	A
E_{AS}	Single Pulsed Avalanche Energy		(Note 2)	480	mJ
I_{AR}	Avalanche Current		(Note 1)	80	A
E_{AR}	Repetitive Avalanche Energy		(Note 1)	17.6	mJ
dv/dt	Peak Diode Recovery dv/dt		(Note 3)	4.5	V/ns
P_D	Power Dissipation	(T_C = 25°C)		176	W
		- Derate above 25°C		1.17	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range			-55 to +175	°C
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds			300	°C

*Drain current limited by maximum junction temperature

Thermal Characteristics

Symbol	Parameter	Ratings	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.85	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	62.5	

Package Marking and Ordering Information $T_C = 25^oC$ unless otherwise noted

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDP80N06	FDP80N06	TO-220	-	-	50

Electrical Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu A$, $V_{GS} = 0V$, $T_J = 25^oC$	60	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu A$, Referenced to 25°C	-	0.075	-	V/^oC
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 60V$, $V_{GS} = 0V$	-	-	1	μA
		$V_{DS} = 48V$, $T_C = 150^oC$	-	-	10	
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 20V$, $V_{DS} = 0V$	-	-	± 100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\mu A$	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10V$, $I_D = 40A$	-	8.5	10	$m\Omega$
g_{FS}	Forward Transconductance	$V_{DS} = 25V$, $I_D = 40A$ (Note 4)	-	67	-	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 25V$, $V_{GS} = 0V$ f = 1MHz	-	2450	3190	pF
C_{oss}	Output Capacitance		-	910	1190	pF
C_{rss}	Reverse Transfer Capacitance		-	145	190	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 30V$, $I_D = 80A$ $R_G = 25\Omega$	-	32	75	ns
t_r	Turn-On Rise Time		-	259	528	ns
$t_{d(off)}$	Turn-Off Delay Time		-	136	282	ns
t_f	Turn-Off Fall Time	(Note 4, 5)	-	113	236	ns
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 48V$, $I_D = 80A$ $V_{GS} = 10V$	-	57	74	nC
Q_{gs}	Gate to Source Gate Charge		-	15	-	nC
Q_{gd}	Gate to Drain "Miller" Charge	(Note 4, 5)	-	24	-	nC
Drain-Source Diode Characteristics						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	80	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	320	A
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0V$, $I_{SD} = 80A$	-	-	1.4	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0V$, $I_{SD} = 80A$ $dI_F/dt = 100A/\mu s$	-	64	-	ns
Q_{rr}	Reverse Recovery Charge	(Note 4)	-	127	-	nC

Notes:
1: Repetitive Rating: Pulse width limited by maximum junction temperature
2: L = 0.15mH, $I_{AS} = 80A$, $V_{DD} = 50V$, $R_G = 25\Omega$, Starting $T_J = 25°C$
3: $I_{SD} \leq 80A$, di/dt $\leq 200A/\mu s$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25°C$
4: Pulse Test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$
5: Essentially Independent of Operating Temperature Typical Characteristics

Typical Performance Characteristics
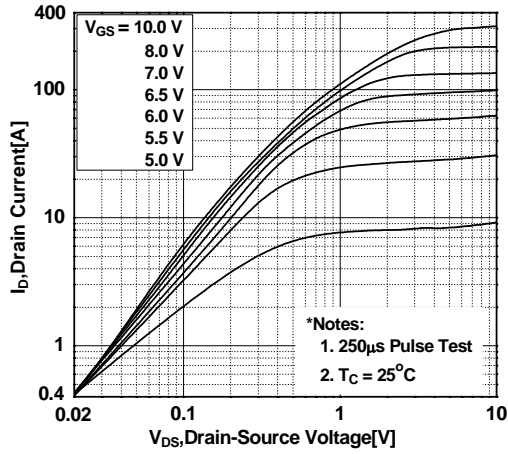
Figure 1. On-Region Characteristics
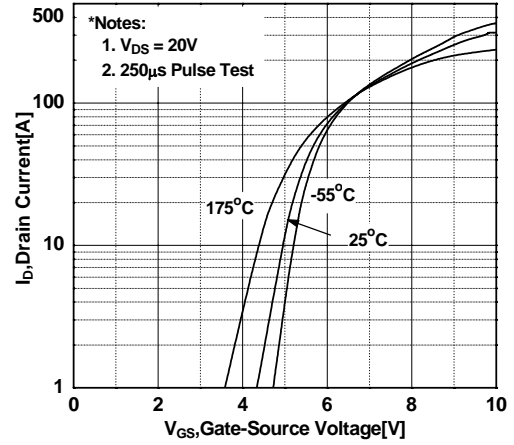

Figure 1. On-Region Characteristics

V_{GS} = 10.0 V
8.0 V
7.0 V
6.5 V
6.0 V
5.5 V
5.0 V

I_D, Drain Current [A]

V_{DS}, Drain-Source Voltage [V]

*Notes:
1. 250μs Pulse Test
2. T_C = 25°C

Figure 2. Transfer Characteristics

*Notes:
1. V_{DS} = 20V
2. 250μs Pulse Test

175°C   -55°C
25°C

I_D, Drain Current [A]

V_{GS}, Gate-Source Voltage [V]

Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

V_{GS} = 10V
V_{GS} = 20V

*Note: T_J = 25°C

$R_{DS(ON)}$ [Ω], Drain-Source On-Resistance

I_D, Drain Current [A]
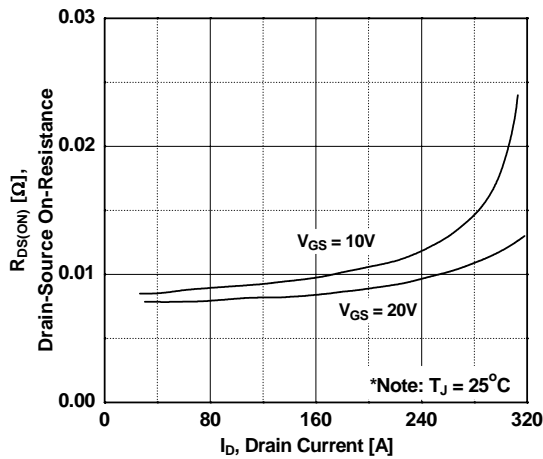
Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

175°C   25°C

*Notes:
1. V_{GS} = 0V
2. 250μs Pulse Test

I_S, Reverse Drain Current [A]

V_{SD}, Body Diode Forward Voltage [V]
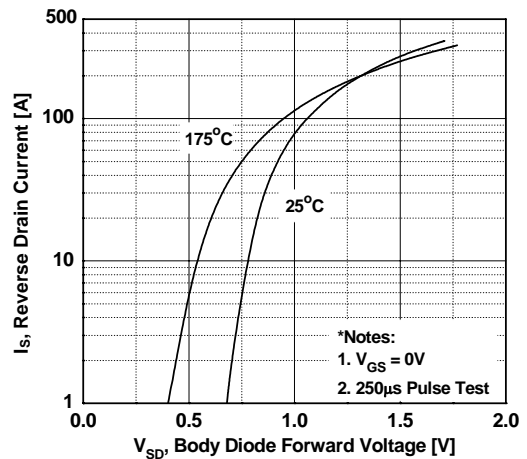
Figure 5. Capacitance Characteristics

C_{iss}
C_{oss}
C_{rss}

C_{iss} = C_{gs} + C_{gd} (C_{ds} = shorted)
C_{oss} = C_{ds} + C_{gd}
C_{rss} = C_{gd}

*Note:
1. V_{GS} = 0V
2. f = 1MHz

Capacitances [pF]

V_{DS}, Drain-Source Voltage [V]
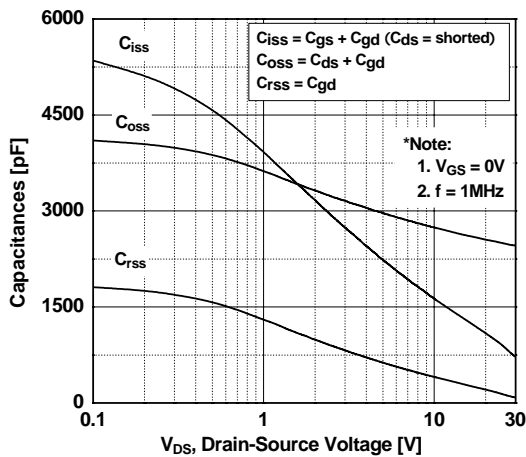
Figure 6. Gate Charge Characteristics

V_{DS} = 15V
V_{DS} = 30V
V_{DS} = 48V

*Note: I_D = 80A

V_{GS}, Gate-Source Voltage [V]

Q_g, Total Gate Charge [nC]
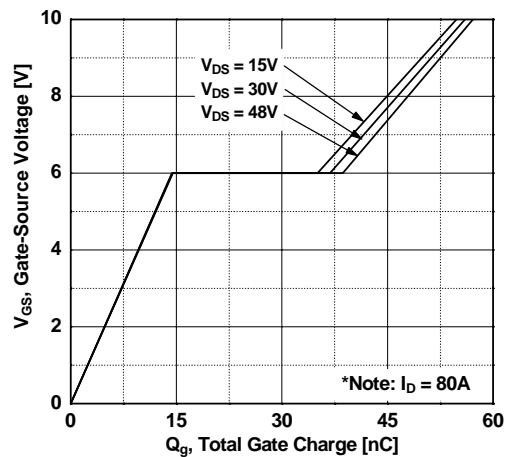
Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

*Notes:
1. V_{GS} = 0V
2. I_D = 1mA

Y-axis: BV_{DSS}, [Normalized] Drain-Source Breakdown Voltage
X-axis: T_J, Junction Temperature [°C]
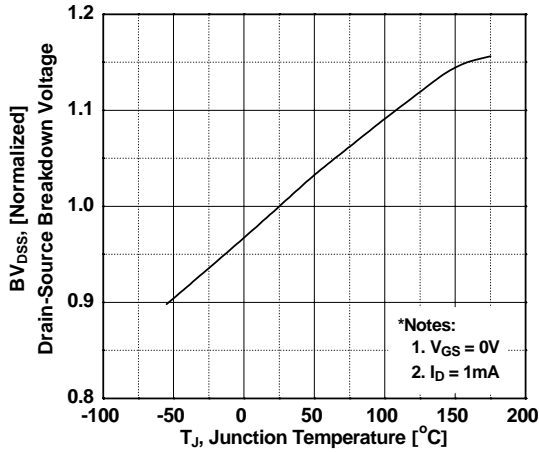
Figure 8. On-Resistance Variation vs. Temperature

*Notes:
1. V_{GS} = 10V
2. I_D = 40A

Y-axis: $R_{DS(on)}$, [Normalized] Drain-Source On-Resistance
X-axis: T_J, Junction Temperature [°C]
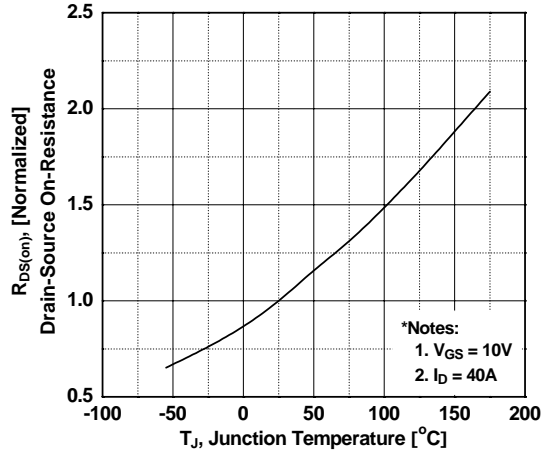
Figure 9. Maximum Safe Operating Area

30µs
100µs
1ms
10ms
DC

Operation in This Area is Limited by $R_{DS(on)}$

*Notes:
1. T_C = 25°C
2. T_J = 175°C
3. Single Pulse

Y-axis: I_D, Drain Current [A]
X-axis: V_{DS}, Drain-Source Voltage [V]
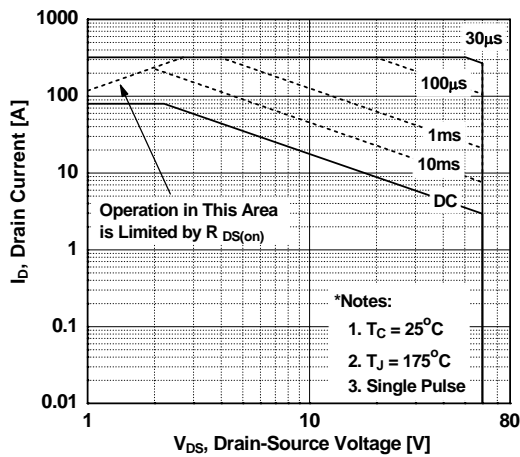
Figure 10. Maximum Drain Current vs. Case Temperature
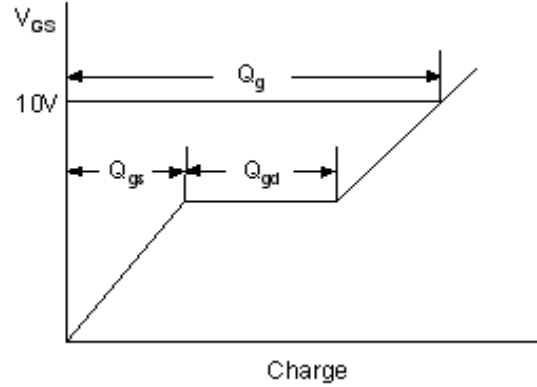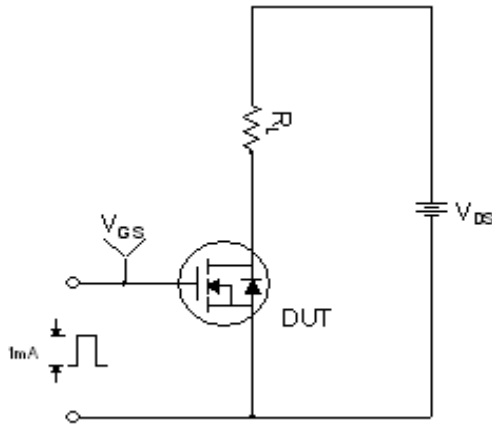

Y-axis: I_D, Drain Current [A]
X-axis: T_C, Case Temperature [°C]
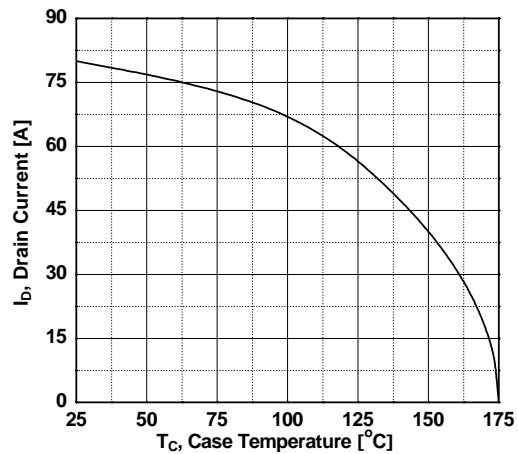
Figure 11. Transient Thermal Response Curve

0.5
0.2
0.1
0.05
0.02
0.01
Single pulse

P_{DM}
t_1
t_2

*Notes:
1. $Z_{\theta JC}(t)$ = 0.85°C/W Max.
2. Duty Factor, D= t_1/t_2
3. T_{JM} - T_C = $P_{DM} * Z_{\theta JC}(t)$

Y-axis: Thermal Response [$Z_{\theta JC}$]
X-axis: Rectangular Pulse Duration [sec]
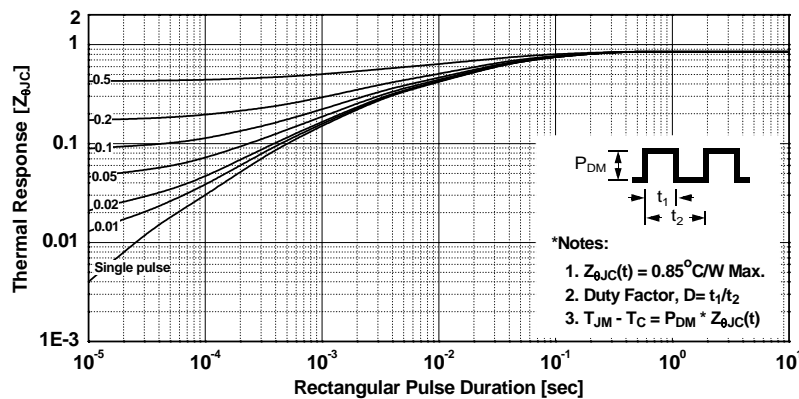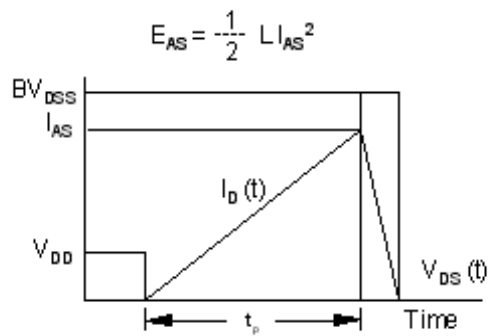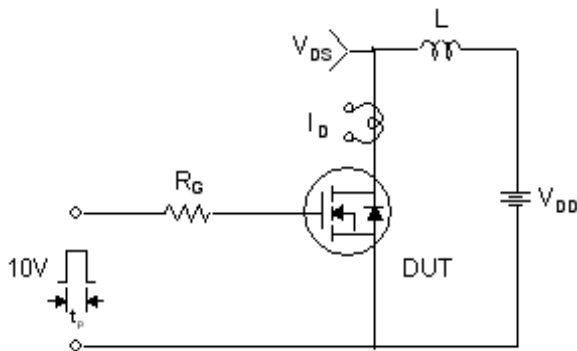
Gate Charge Test Circuit & Waveform

Resistive Switching Test Circuit & Waveforms
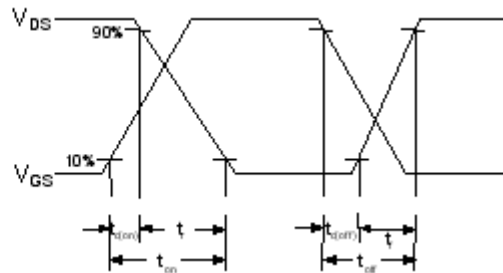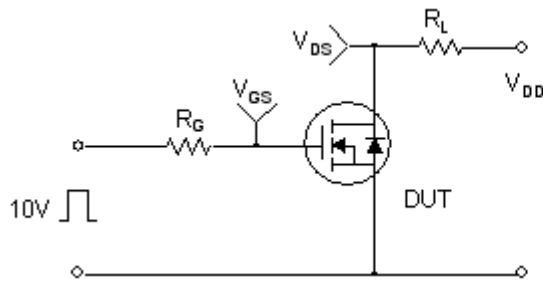
Unclamped Inductive Switching Test Circuit & Waveforms

$$E_{AS} = \frac{1}{2} L I_{AS}^2$$

Peak Diode Recovery dv/dt Test Circuit & Waveforms

$$D = \frac{\text{Gate Pulse Width}}{\text{Gate Pulse Period}}$$

Mechanical Dimensions

TO-220
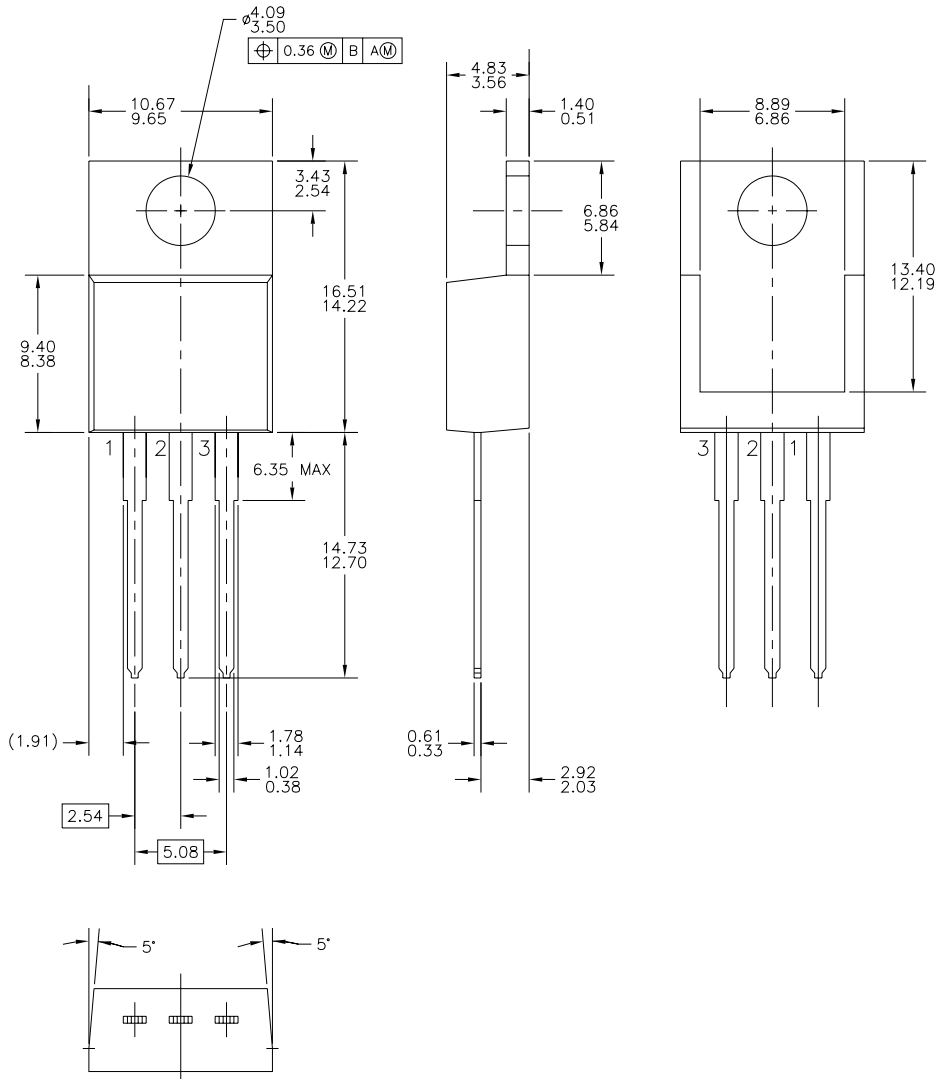
Dimensions in Millimeters

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