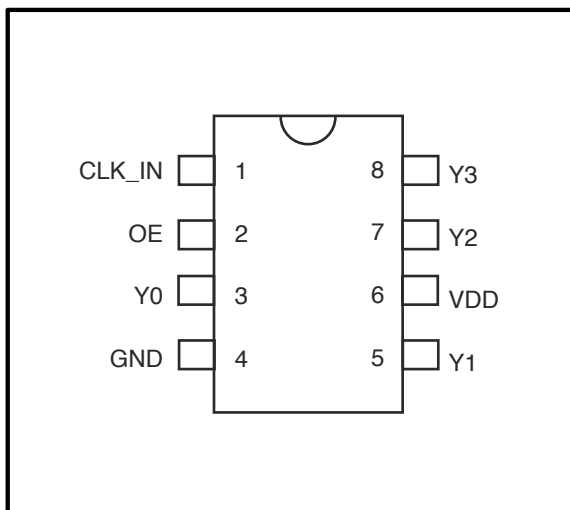


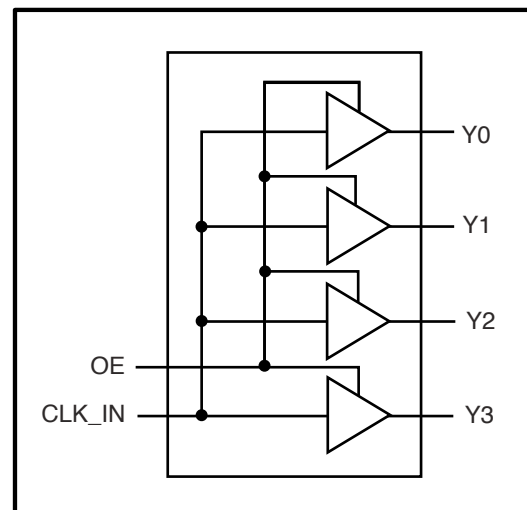
700MHz TTL/CMOS Potato Chip

FEATURES:	DESCRIPTION:
<ul style="list-style-type: none"> • Patented technology • Operating frequency up to 700MHz with 2pf load • Operating frequency up to 650MHz with 5pf load • Operating frequency up to 450MHz with 15pf load • Operating frequency up to 100MHz with 50pf load • Very low output pin to pin skew < 100ps • Very low pulse skew < 150ps • VCC = 1.65V to 3.6V • Propagation delay < 2.1ns max with 15pf load • Low input capacitance: 3pf typical • 1:4 fanout • Packaging (Pb-free & Green available) • Available in 8-pin TSSOP package 	<p>Potato Semiconductor's PO74G304A is designed for world top performance using submicron CMOS technology to achieve 700MHz TTL output frequency with less than 100ps output pin to pin skew.</p> <p>PO74G304A is a 3.3V CMOS 1 input to 4 outputs Buffered driver to achieve 700MHz output frequency. Typical applications are clock and signal distribution. They are used for networking and communications applications.</p> <p>Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of these devices as translators in a mixed 3.3V/5V system environment.</p>

Pin Configuration



Logic Block Diagram



Pin Description

Pin#	Description
1	5V Tolerant clock input
2	Active High Output Enable.
3,5,7,8	LVC MOS level outputs
4	Ground
6	3.3V power

FUNCTION TABLE

INPUTS		OUTPUT
CLKIN	OE	1Y (0:3)
L	L	L
H	L	L
L	H	L
H	H	H

700MHz TTL/CMOS Potato Chip

Maximum Ratings

Description	Max	Unit
Storage Temperature	-65 to 150	°C
Operation Temperature	-40 to 85	°C
Operation Voltage	-0.5 to +4.6	V
Input Voltage	-0.5 to +5.5	V
Output Voltage	-0.5 to Vcc+0.5	V

Note:

stresses greater than listed under Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability specification is not implied.

DC Electrical Characteristics

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output High voltage	Vcc=3V Vin=V _{IH} or V _{IL} , I _{OH} = -12mA	2.4	3	-	V
V_{OL}	Output Low voltage	Vcc=3V Vin=V _{IH} or V _{IL} , I _{OH} =12mA	-	0.4	0.5	V
V_{IH}	Input High voltage	Guaranteed Logic HIGH Level (Input Pin)	2	-	5.5	V
V_{IL}	Input Low voltage	Guaranteed Logic LOW Level (Input Pin)	-0.5	-	0.8	V
I_{IH}	Input High current	Vcc = 3.6V and Vin = 5.5V	-	-	50	uA
I_{IL}	Input Low current	Vcc = 3.6V and Vin = 0V	-	-	-50	uA
V_{IK}	Clamp diode voltage	Vcc = Min. And I _{IN} = -18mA	-	-0.7	-1.2	V

Notes:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 3.3V, 25 °C ambient.
3. This parameter is guaranteed but not tested.
4. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
5. V_{oH} = Vcc – 0.6V at rated current

700MHz TTL/CMOS Potato Chip

Power Supply Characteristics

Symbol	Description	Test Conditions (1)	Min	Typ	Max	Unit
IccQ	Quiescent Power Supply Current	Vcc=Max, Vin=Vcc or GND	-	0.1	30	uA
ΔIcc	Power Supply Current per Input High	Vcc=Max, Vin= Vcc-0.6V	-	50	300	uA

Notes:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 3.3V, 25°C ambient.
3. This parameter is guaranteed but not tested.
4. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
5. VoH = Vcc – 0.6V at rated current

Capacitance

Parameters (1)	Description	Test Conditions	Typ	Max	Unit
Cin	Input Capacitance	Vin = 0V	3	4	pF
Cout	Output Capacitance	Vout = 0V	-	6	pF

Notes:

- 1 This parameter is determined by device characterization but not production tested.

Switching Characteristics

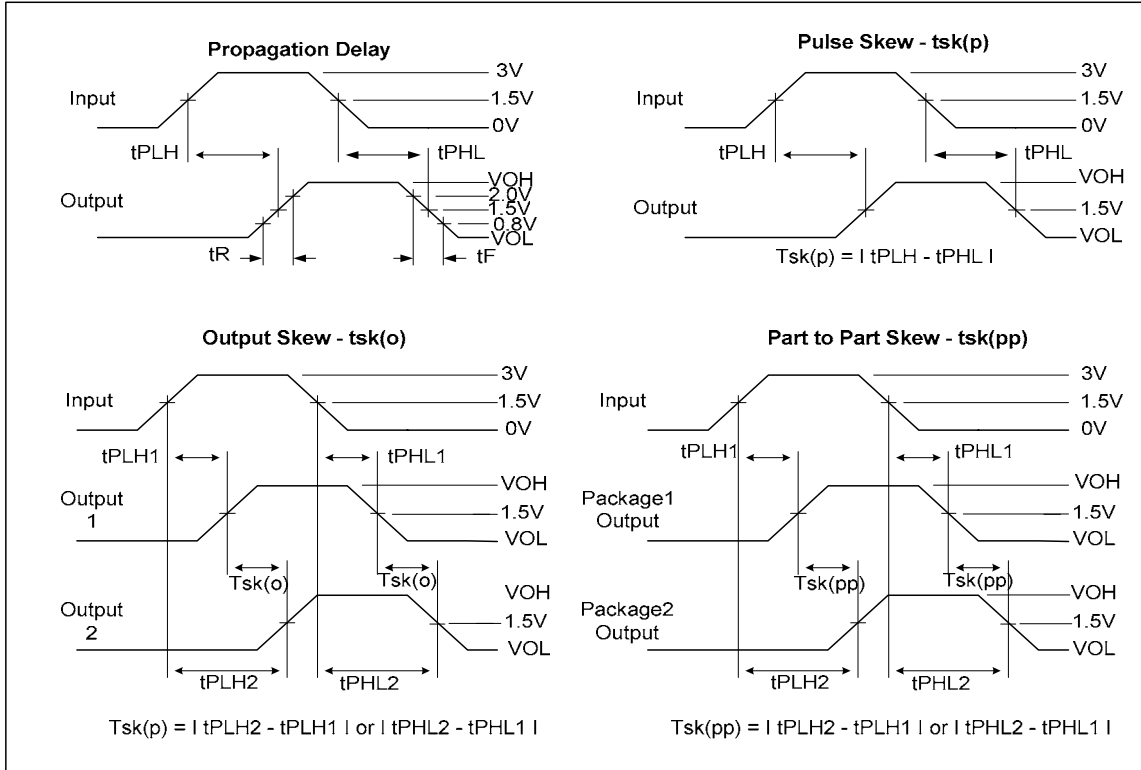
Symbol	Description	Test Conditions (1)	Max	Unit
tPLH	Propagation Delay A to Bn	CL = 15pF	2.1	ns
tPHL	Propagation Delay A to Bn	CL = 15pF	2.1	ns
tr/tf	Rise/Fall Time	0.8V – 2.0V	0.8	ns
tsk(p)	Pulse Skew (Same Package)	CL = 15pF, 125MHz	150	ps
tsk(o)	Output Pin to Pin Skew (Same Package)	CL = 15pF, 125MHz	100	ps
tsk(pp)	Output Skew (Different Package)	CL = 15pF, 125MHz	400	ps
fmax	Input Frequency	CL = 50pF	100	MHz
fmax	Input Frequency	CL = 15pF	450	MHz
fmax	Input Frequency	CL = 5pF	650	MHz
fmax	Input Frequency	CL = 2pF	700	MHz

Notes:

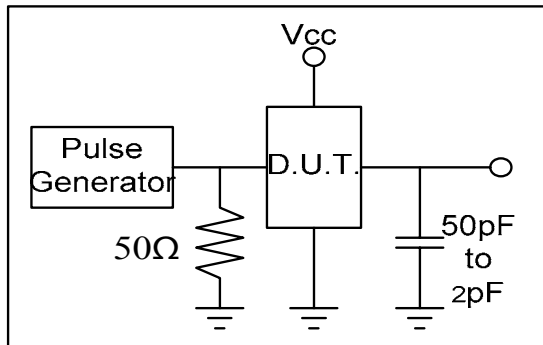
1. See test circuits and waveforms.
2. tPLH, tPHL, tsk(p), and tsk(o) are production tested. All other parameters guaranteed but not production tested.
3. Airflow of 1m/s is recommended for frequencies above 133MHz

700MHz TTL/CMOS Potato Chip

Test Waveforms

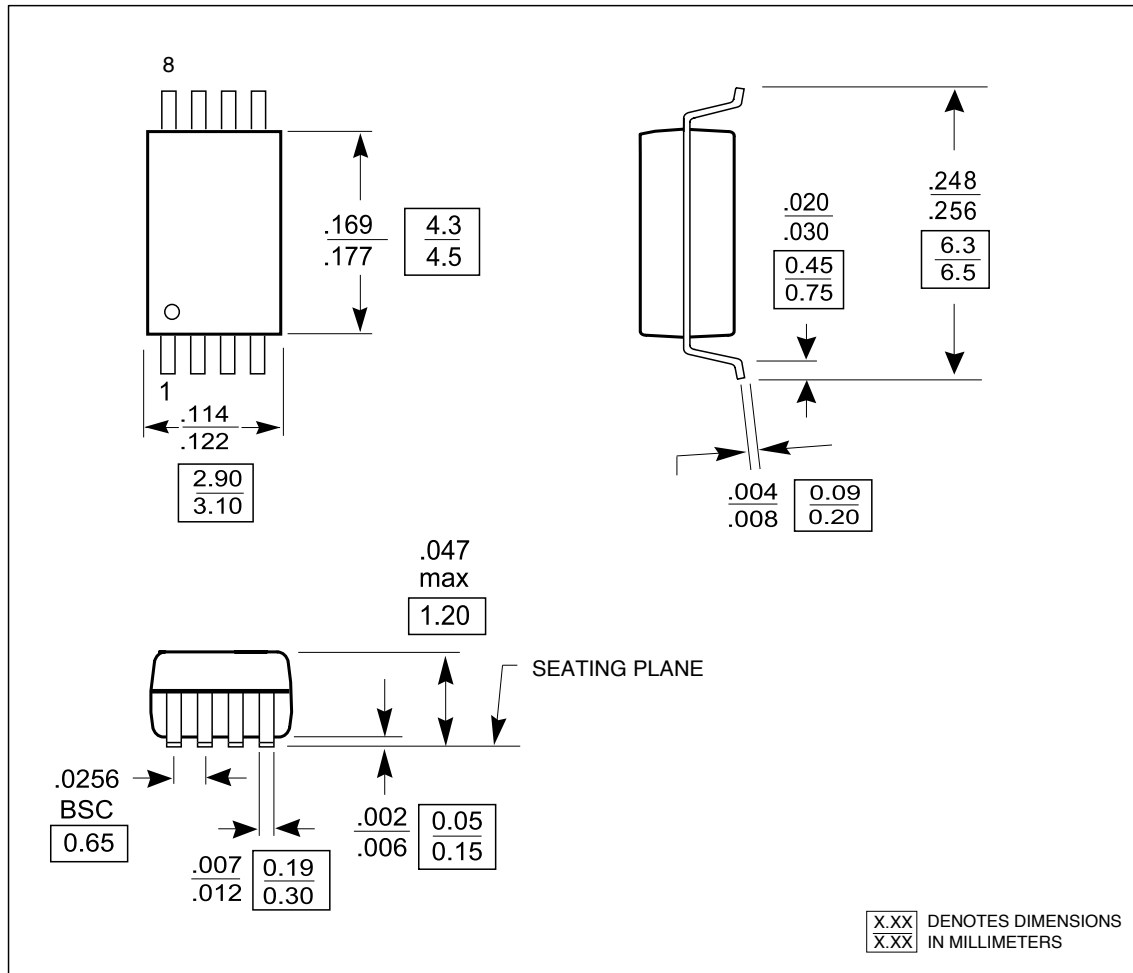


Test Circuit



700MHz TTL/CMOS Potato Chip

Packaging Mechanical Drawing: 8 pin TSSOP



700MHz TTL/CMOS Potato Chip

Ordering Information

Ordering Code	Package			Top-Marking	T _A
PO74G304ATU	8pin TSSOP	Tube	Pb-free & Green	PO74G304AT	-40°C to 85°C
PO74G304ATR	8pin TSSOP	Tape and reel	Pb-free & Green	PO74G304AT	-40°C to 85°C