

## High voltage fast-switching NPN power transistor

### General features

- Medium voltage capability
- Low spread of dynamic parameters
- Minimum lot-to-lot spread for reliable operation
- Very high switching speed

### Applications

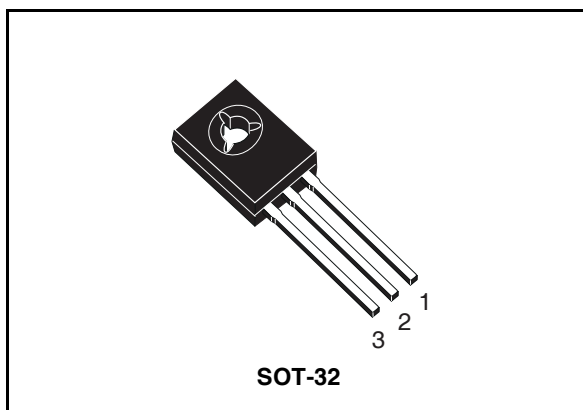
- Electronic ballast for fluorescent lighting (CFL)

### Description

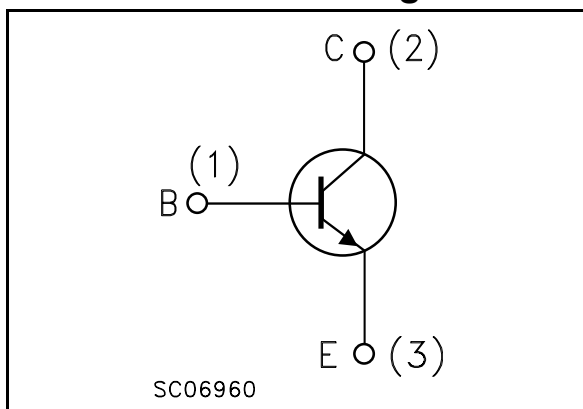
The device is manufactured using high voltage Multi-Epitaxial Planar technology for high switching speeds and medium voltage capability.

It uses a Cellular Emitter structure with planar edge termination to enhance switching speeds while maintaining the wide RBSOA.

The device is designed for use in lighting applications.



### Internal schematic diagram



### Order codes

Part Number	Marking	Package	Packaging
ST13003-K	13003	SOT-32	Bag

# 1 Electrical ratings

**Table 1. Absolute maximum rating**

Symbol	Parameter	Value	Unit
$V_{CES}$	Collector-emitter voltage ( $V_{BE} = 0$ )	700	V
$V_{CEO}$	Collector-emitter voltage ( $I_B = 0$ )	400	V
$V_{EBO}$	Emitter-base voltage ( $I_C = 0$ , $I_B = 0.75A$ , $t_p < 10\mu s$ , $T_j < 150^\circ C$ )	$V_{(BR)EBO}$	V
$I_C$	Collector current	1.5	A
$I_{CM}$	Collector peak current ( $t_p < 5ms$ )	3	A
$I_B$	Base current	0.75	A
$I_{BM}$	Base peak current ( $t_p < 5ms$ )	1.5	A
$P_{tot}$	Total dissipation at $T_c = 25^\circ C$	40	W
$T_{stg}$	Storage temperature	-55 to 150	$^\circ C$
$T_J$	Max. operating junction temperature	150	$^\circ C$

## 2 Electrical characteristics

( $T_{\text{case}} = 25^{\circ}\text{C}$  unless otherwise specified)

**Table 2. Electrical characteristics**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{\text{CEV}}$	Collector cut-off current ( $V_{\text{BE}} = -1.5\text{V}$ )	$V_{\text{CE}} = 700\text{V}$ $V_{\text{CE}} = 700\text{V}$ $T_{\text{J}} = 125^{\circ}\text{C}$			1 5	mA mA
$V_{(\text{BR})\text{EBO}}$	Emitter-Base breakdown voltage ( $I_{\text{C}} = 0$ )	$I_{\text{E}} = 10\text{mA}$	9		18	V
$V_{\text{CEO(sus)}}^{(1)}$	Collector-emitter sustaining voltage ( $I_{\text{B}} = 0$ )	$I_{\text{C}} = 10\text{mA}$ $L = 25\text{mH}$	400			V
$V_{\text{CE(sat)}}^{(1)}$	Collector-emitter saturation voltage	$I_{\text{C}} = 0.5\text{A}$ $I_{\text{B}} = 0.1\text{A}$ $I_{\text{C}} = 1\text{A}$ $I_{\text{B}} = 0.25\text{A}$ $I_{\text{C}} = 1.5\text{A}$ $I_{\text{B}} = 0.5\text{A}$			0.5 1 3	V V V
$V_{\text{BE(sat)}}^{(1)}$	Base-emitter saturation voltage	$I_{\text{C}} = 0.5\text{A}$ $I_{\text{B}} = 0.1\text{A}$ $I_{\text{C}} = 1\text{A}$ $I_{\text{B}} = 0.25\text{A}$			1 1.2	V V
$h_{\text{FE}}$	DC current gain	$I_{\text{C}} = 0.5\text{A}$ $V_{\text{CE}} = 2\text{V}$ $I_{\text{C}} = 1\text{A}$ $V_{\text{CE}} = 2\text{V}$	8 5		20 25	
$t_{\text{r}}$ $t_{\text{s}}$ $t_{\text{f}}$	RESISTIVE LOAD Rise time Storage time Fall time	$V_{\text{CC}} = 125\text{V}$ $I_{\text{C}} = 1\text{A}$ $I_{\text{B1}} = 0.2\text{A}$ $I_{\text{B2}} = -0.2\text{A}$ $T_{\text{p}} = 25\mu\text{s}$			1 4 0.7	$\mu\text{s}$ $\mu\text{s}$ $\mu\text{s}$
$t_{\text{s}}$	INDUCTIVE LOAD Storage time	$I_{\text{C}} = 1\text{A}$ $I_{\text{B1}} = 0.2\text{A}$ $V_{\text{BE}} = -5\text{V}$ $L = 50\text{mH}$ $V_{\text{Clamp}} = 300\text{V}$		0.8		$\mu\text{s}$

Note (1) Pulsed duration = 300  $\mu\text{s}$ , duty cycle  $\leq 1.5\%$

2.1 Electrical characteristics (curves)

Figure 1. Safe operating areas

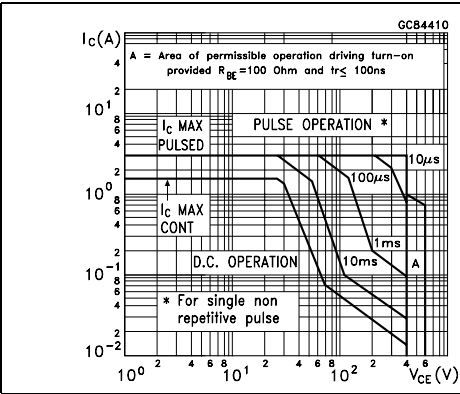


Figure 2. Derating curves

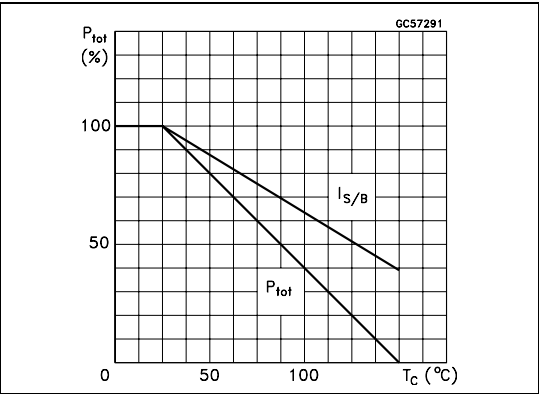


Figure 3. Output characteristics

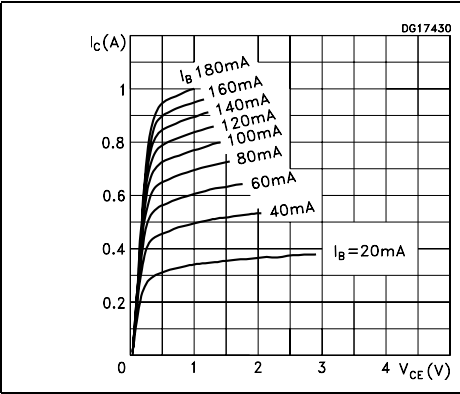


Figure 4. Reverse biased safe operating areas

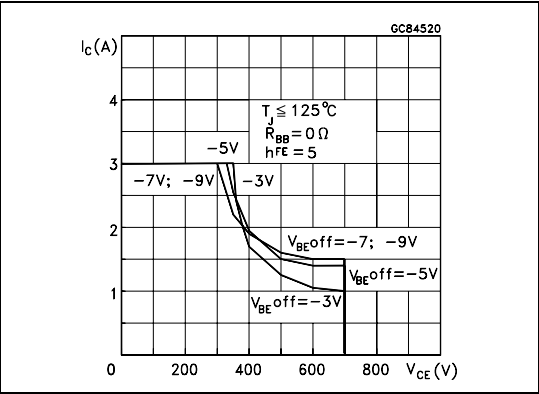


Figure 5. DC current gain

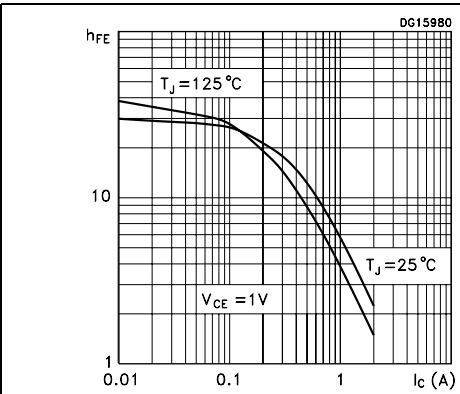
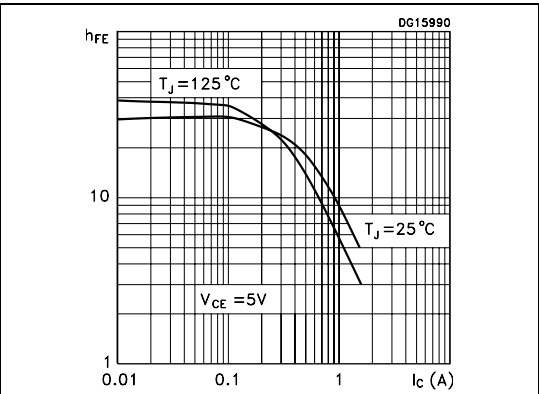
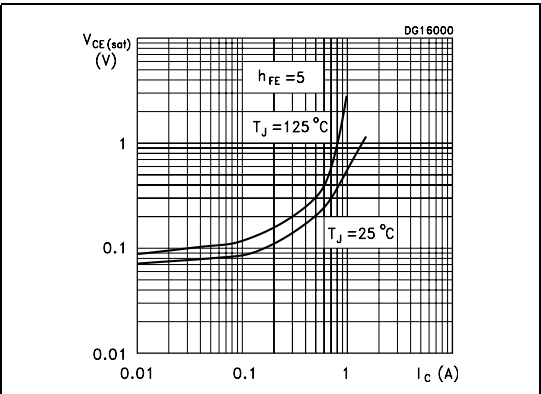


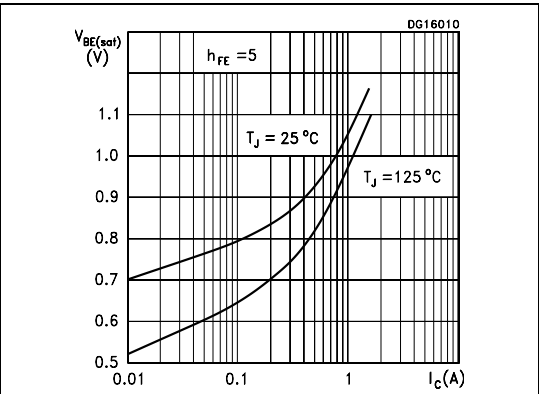
Figure 6. DC current gain



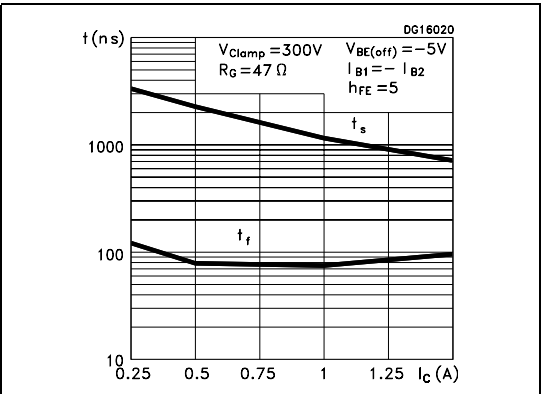
**Figure 7. Collector-emitter saturation voltage**



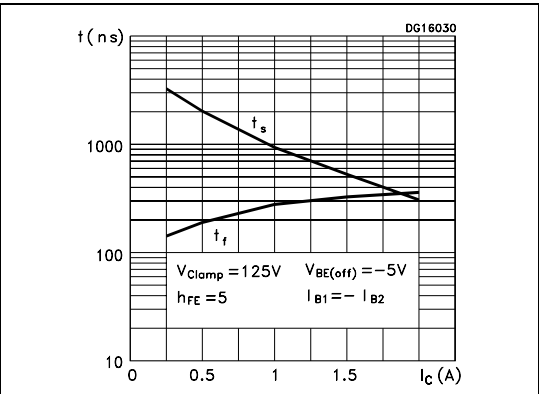
**Figure 8. Base-emitter saturation voltage**



**Figure 9. Inductive load switching time**

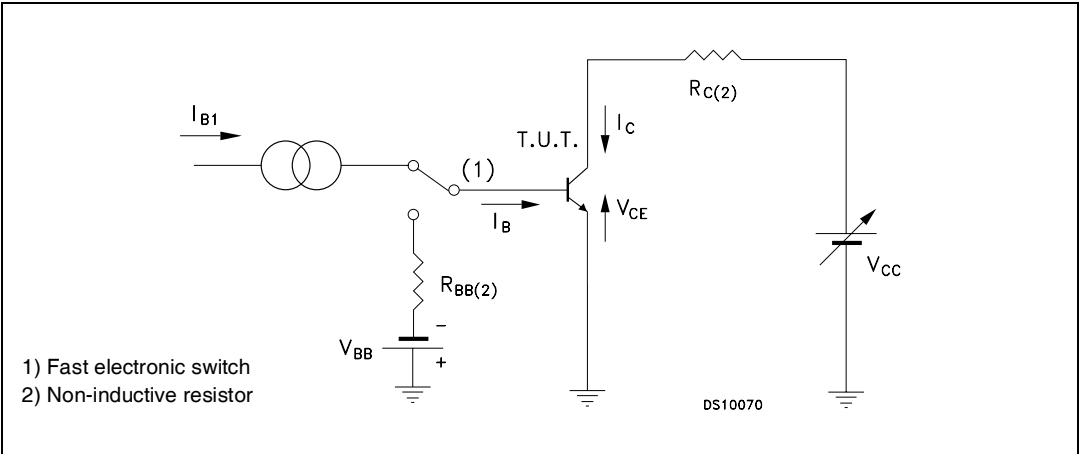


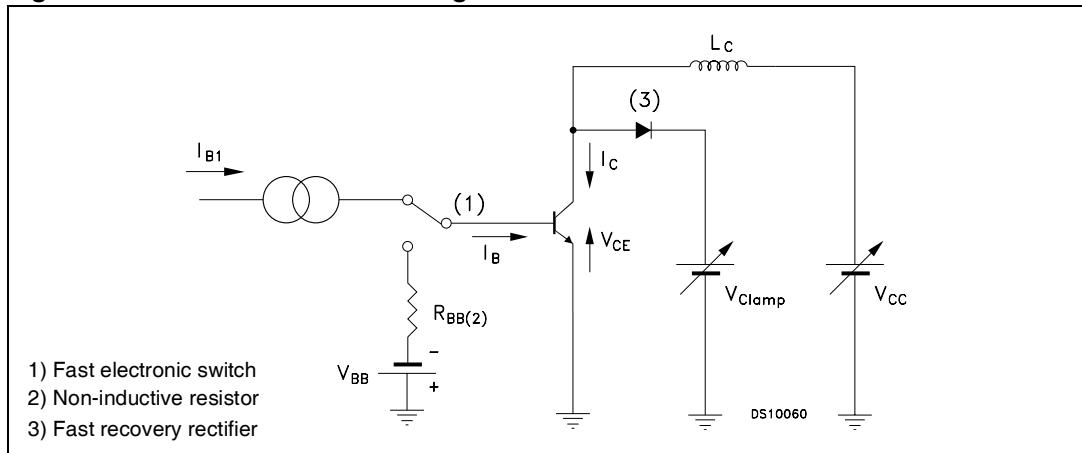
**Figure 10. Resistive load switching time**



## 2.2 Test circuits

**Figure 11. Resistive load switching test circuit**



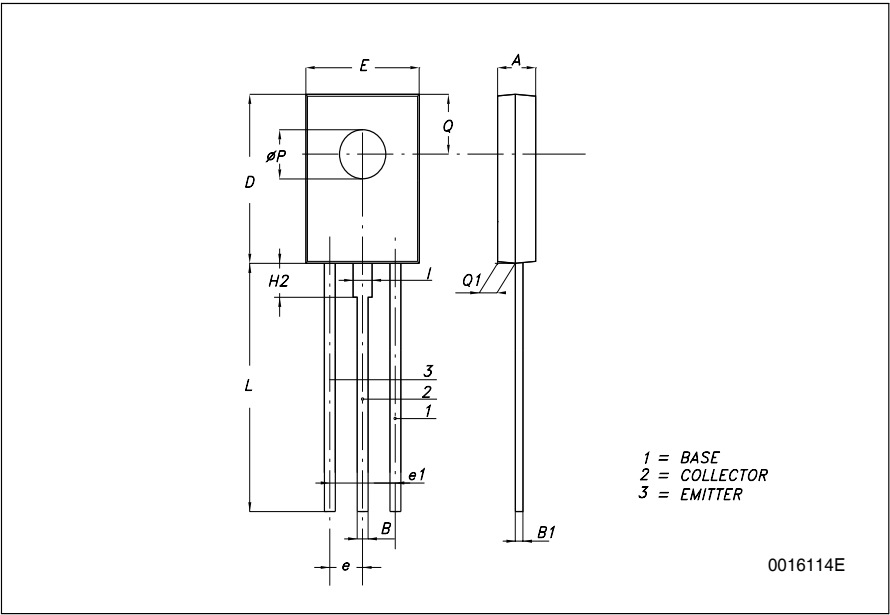
**Figure 12. Inductive load switching test circuit**

### 3      **Package mechanical data**

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

SOT-32 (TO-126) MECHANICAL DATA

DIM.	mm.		
	MIN.	TYP	MAX.
A	2.4		2.9
B	0.64		0.88
B1	0.39		0.63
D	10.5		11.05
E	7.4		7.8
e	2.04	2.29	2.54
e1	4.07	4.58	5.08
L	15.3		16
P	2.9		3.2
Q		3.8	
Q1	1		1.52
H2		2.15	
I		1.27	



## 4 Revision history

**Table 3. Revision history**

Date	Revision	Changes
23-May-2007	1	Initial release.

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