

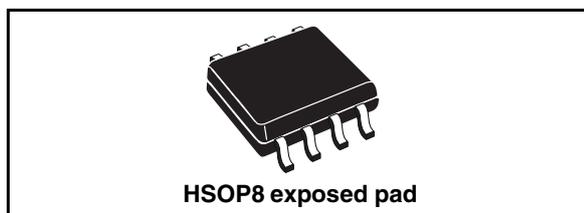
## Up to 2 A step down switching regulator for automotive applications

### Features

- Qualified following the AEC-Q100 requirements (temperature grade 3), see PPAP for more details.
- 2 A DC output current
- Operating input voltage from 4 V to 36 V
- 3.3 V / ( $\pm 2\%$ ) reference voltage
- Output voltage adjustable from 1.235 V to 35 V
- Low dropout operation: 100 % duty cycle
- 250 kHz Internally fixed frequency
- Voltage feedforward
- Zero load current operation
- Internal current limiting
- Inhibit for zero current consumption
- Synchronization
- Protection against feedback disconnection
- Thermal shutdown

### Application

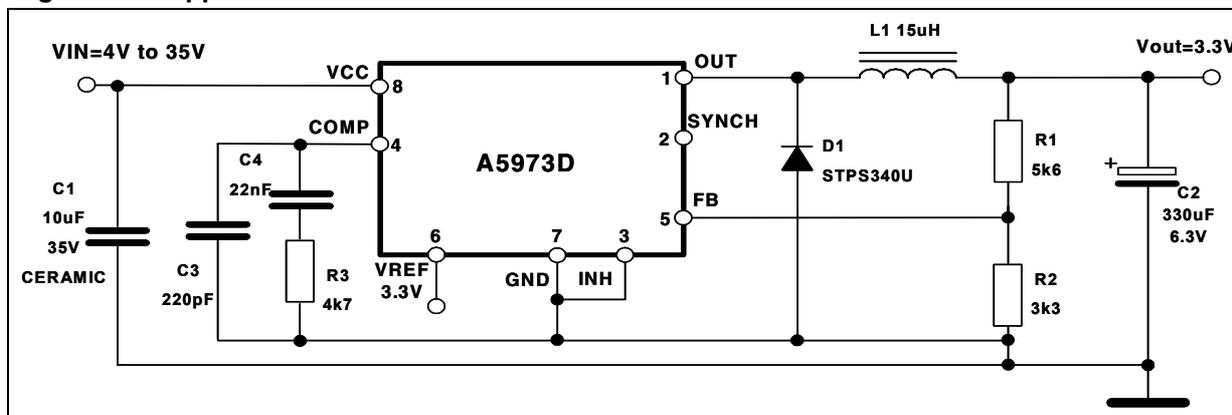
- Dedicated to automotive applications



### Description

The A5973D is a step down monolithic power switching regulator with a minimum switch current limit of 2.25 A so it is able to deliver more than 2 A DC current to the load depending on the application conditions. The output voltage can be set from 1.235 V to 35 V. The high current level is also achieved thanks to an HSOP8 package with exposed frame, that allows to reduce the  $R_{th(JA)}$  down to approximately  $40^{\circ}\text{C/W}$ . The device uses an internal P-channel DMOS transistor (with a typical  $R_{DS(on)}$  of 250 m $\Omega$ ) as switching element to minimize the size of the external components. An internal oscillator fixes the switching frequency at 250 kHz. Having a minimum input voltage of 4 V only, it is particularly suitable for 5 V bus. Pulse by pulse current limit with the internal frequency modulation offers an effective constant current short circuit protection. Pulse by pulse current limit with the internal frequency modulation offers an effective constant current short circuit protection.

**Figure 1. Application schematic**



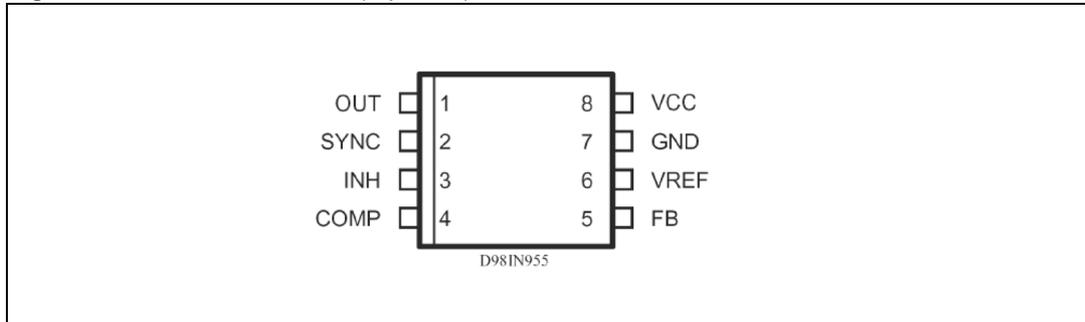
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# 1 Pin settings

## 1.1 Pin connection

Figure 1. Pin connection (top view)



## 1.2 Pin description

Table 1. Pin description

N	Pin	Description
1	OUT	Regulator output.
2	SYNCH	Master/slave synchronization.
3	INH	A logical signal (active high) disables the device. If INH not used the pin must be grounded. When it is open an internal pull-up disable the device.
4	COMP	E/A output for frequency compensation.
5	FB	Feedback input. Connecting directly to this pin results in an output voltage of 1.23 V. An external resistive divider is required for higher output voltages.
6	VREF	3.3 V VREF. No cap is requested for stability.
7	GND	Ground.
8	VCC	Unregulated DC input voltage.

## 2 Electrical data

### 2.1 Maximum ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_8$	Input voltage	40	V
$V_1$	OUT pin DC voltage	-1 to 40	V
	OUT pin peak voltage at $\Delta t = 0.1 \mu\text{s}$	-5 to 40	V
$I_1$	Maximum output current	int. limit.	
$V_4, V_5$	Analog pins	4	V
$V_3$	INH	-0.3 to $V_{CC}$	V
$V_2$	SYNCH	-0.3 to 4	V
$P_{TOT}$	Power dissipation at $T_A \leq 70 \text{ }^\circ\text{C}$	2.25	W
$T_J$	Operating junction temperature range	-40 to 150	$^\circ\text{C}$
$T_{STG}$	Storage temperature range	-55 to 150	$^\circ\text{C}$

### 2.2 Thermal data

**Table 3. Thermal data**

Symbol	Parameter	SO8	Unit
$R_{thJA}$	Maximum thermal resistance junction-ambient	40 <sup>(1)</sup>	$^\circ\text{C}/\text{W}$

1. Package mounted on board

### 3 Electrical characteristics

**Table 4. Electrical characteristics**  
( $T_J = -40\text{ °C}$  to  $125\text{ °C}$ ,  $V_{CC} = 12\text{ V}$ , unless otherwise specified)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
$V_{CC}$	Operating input voltage range	$V_0 = 1.235\text{ V}$ ; $I_0 = 2\text{ A}$	4		36	V
$R_{DS(on)}$	MOSFET on resistance			0.250	0.5	$\Omega$
$I_L$	Maximum limiting current <sup>(1)</sup>	$V_{CC} = 5\text{ V}$	2.25	3	3.5	A
		$V_{CC} = 5\text{ V}$ , $T_J = 25\text{ °C}$	2.5	3	3.5	
$f_{SW}$	Switching frequency		212	250	280	kHz
	Duty cycle		0		100	%
<b>Dynamic characteristics</b> (see test circuit)						
$V_5$	Voltage feedback	$4.4\text{ V} < V_{CC} < 36\text{ V}$ , $20\text{ mA} < I_0 < 2\text{ A}$	1.198	1.235	1.272	V
$\eta$	Efficiency	$V_0 = 5\text{ V}$ , $V_{CC} = 12\text{ V}$		90		%
<b>DC characteristics</b>						
$I_{qop}$	Total operating quiescent current			3	5	mA
$I_q$	Quiescent current	Duty cycle = 0; $V_{FB} = 1.5\text{ V}$			2.5	mA
$I_{qst-by}$	Total stand-by quiescent current	$V_{inh} > 2.2\text{ V}$		50	100	$\mu\text{A}$
		$V_{CC} = 36\text{ V}$ ; $V_{inh} > 2.2\text{ V}$		80	150	$\mu\text{A}$
<b>Inhibit</b>						
	INH threshold voltage	Device ON			0.8	V
		Device OFF	2.2			V
<b>Error amplifier</b>						
$V_{OH}$	High level output voltage	$V_{FB} = 1\text{ V}$	3.5			V
$V_{OL}$	Low level output voltage	$V_{FB} = 1.5\text{ V}$			0.4	V
$I_{o\ source}$	Source output current	$V_{COMP} = 1.9\text{ V}$ ; $V_{FB} = 1\text{ V}$	190	300		$\mu\text{A}$
$I_{o\ sink}$	Sink output current	$V_{COMP} = 1.9\text{ V}$ ; $V_{FB} = 1.5\text{ V}$	1	1.5		mA
$I_b$	Source bias current			2.5	4	$\mu\text{A}$
	DC open loop gain	$R_L = \infty$	50	65		dB

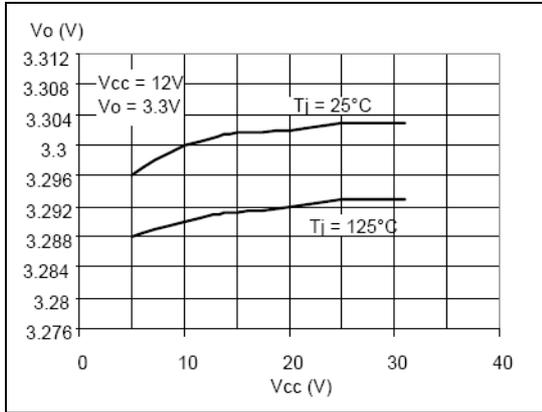
**Table 4. Electrical characteristics (continued)**  
 ( $T_J = -40\text{ }^\circ\text{C}$  to  $125\text{ }^\circ\text{C}$ ,  $V_{CC} = 12\text{ V}$ , unless otherwise specified)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
gm	Transconductance	$I_{COMP} = -0.1\text{ mA}$ to $0.1\text{ mA}$ ; $V_{COMP} = 1.9\text{ V}$		2.3		mS
<b>Synch function</b>						
	High input voltage	$V_{CC} = 4.4$ to $36\text{ V}$ ;	2.5		$V_{REF}$	V
	Low input voltage	$V_{CC} = 4.4$ to $36\text{ V}$ ;			0.74	V
	Slave synch current	$V_{synch} = 0.74\text{ V}$ <sup>(2)</sup> $V_{synch} = 2.33\text{ V}$	0.11 0.21		0.25 0.45	mA
	Master output amplitude	$I_{source} = 3\text{ mA}$	2.75	3		V
	Output pulse width	no load, $V_{synch} = 1.65\text{ V}$	0.20	0.35		$\mu\text{s}$
<b>Reference section</b>						
	Reference voltage	$I_{REF} = 0$ to $5\text{ mA}$ $V_{CC} = 4.4\text{ V}$ to $36\text{ V}$	3.2	3.3	3.399	V
	Line regulation	$I_{REF} = 0\text{ mA}$ $V_{CC} = 4.4\text{ V}$ to $36\text{ V}$		5	10	mV
	Load regulation	$I_{REF} = 0\text{ mA}$		8	15	mV
	Short circuit current		5	18	35	mA

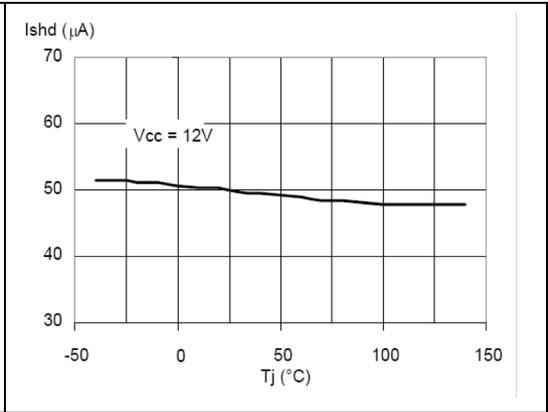
1. With  $T_J = 85\text{ }^\circ\text{C}$ ,  $I_{lim\_min} = 2.5\text{ A}$ , assured by design, characterization and statistical correlation.
2. Guarantee by design

# 4 Typical characteristics

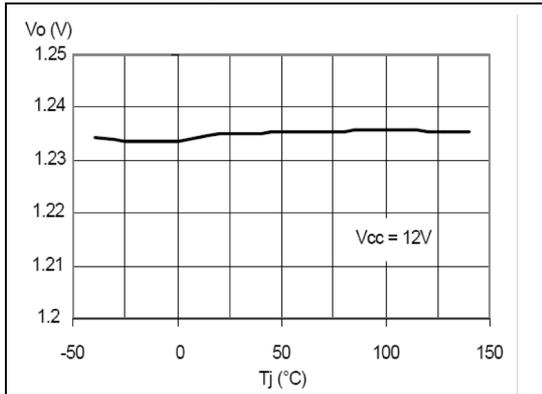
**Figure 2. Line regulator**



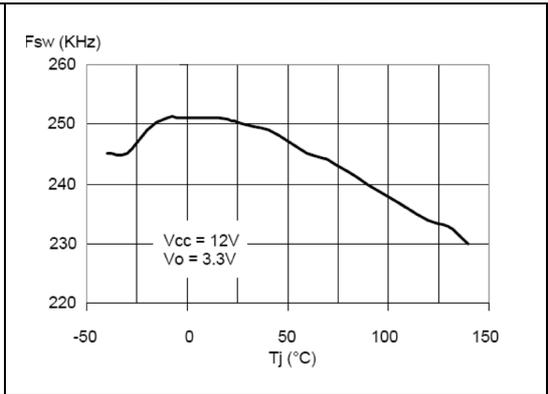
**Figure 3. Shutdown current vs junction temperature**



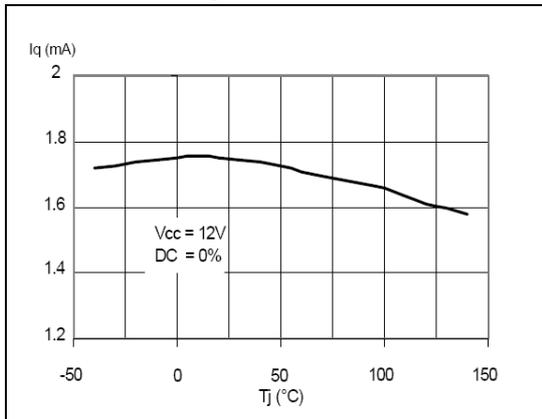
**Figure 4. Output voltage vs junction temperature**



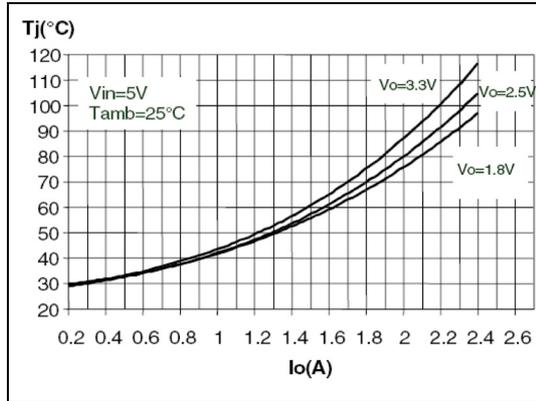
**Figure 5. Switching frequency vs junction temperature**



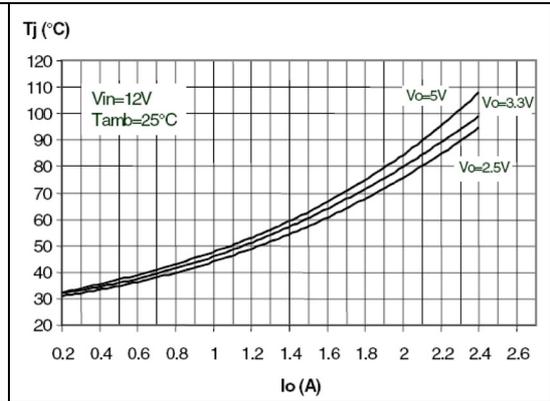
**Figure 6. Quiescent current vs junction temperature**



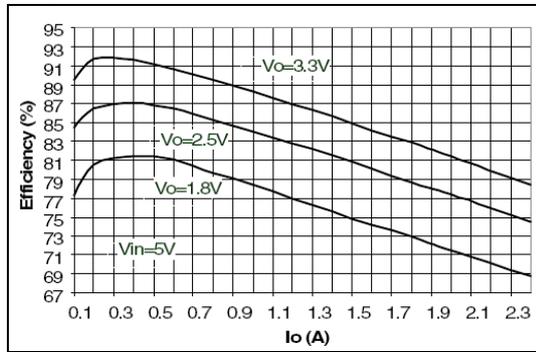
**Figure 7. Junction temperature vs output current**



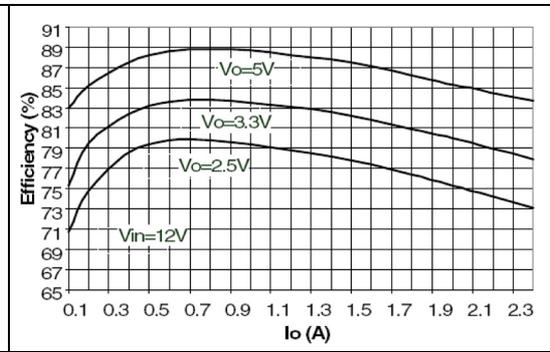
**Figure 8. Junction temperature vs output current**



**Figure 9. Efficiency vs output current**



**Figure 10. Efficiency vs output current**



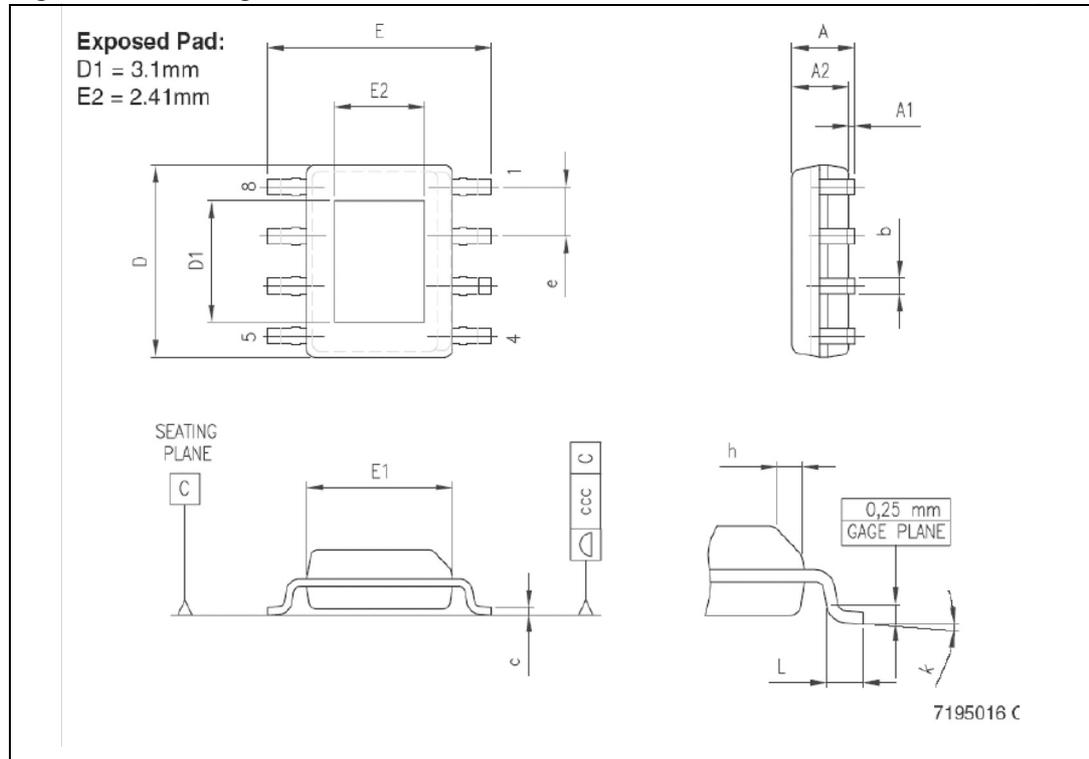
## 5 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

**Table 5. HSOP8 mechanical data**

Dim	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A			1.70			0.0669
A1	0.00		0.10		0.00	0.0039
A2	1.25			0.0492		
b	0.31		0.51	0.0122		0.0201
c	0.17		0.25	0.0067		0.0098
D	4.80	4.90	5.00	0.1890	0.1929	0.1969
D1	3	3.1	3.2	0.118	0.122	0.126
E	5.80	6.00	6.20	0.2283		0.2441
E1	3.80	3.90	4.00	0.1496		0.1575
E2	2.31	2.41	2.51	0.091	0.095	0.099
e		1.27				
h	0.25		0.50	0.0098		0.0197
L	0.40		1.27	0.0157		0.0500
k	0° (min), 8° (max)					
ccc			0.10			0.0039

**Figure 11. Package dimensions**



## 6 Revision history

**Table 6. Document revision history**

Date	Revision	Changes
06-Aug-2007	1	Initial release
23-Oct-2007	2	Updated: <i>Table 4 on page 5, Table 5 on page 10</i>
07-Jan-2008	3	Updated <i>Table 5 on page 10</i>
06-May-2008	4	Updated <i>Table 4 on page 5</i>
29-Aug-2008	5	Updated <i>Table 4 on page 5</i>

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