M61880FP

Laser Diode Driver/Controller

REJ03F0068-0100Z
Rev.1.0
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Description

The M61880FP is a laser diode driver/controller that performs drive and laser power control of a type of semiconductor laser diode in which the semiconductor laser diode anode and monitoring photodiode cathode are connected to the stem.

The M61880FP has a sink type laser drive current output pin, is capable of high-speed switching at up to 200 Mbps, and can drive a laser diode at a maximum drive current of 100 mA (drive current = switching current + bias current).

A high-speed sample-and-hold circuit is incorporated, enabling a self-APC* system to be implemented without the need for laser power control from outside.

* Automatic Power Control

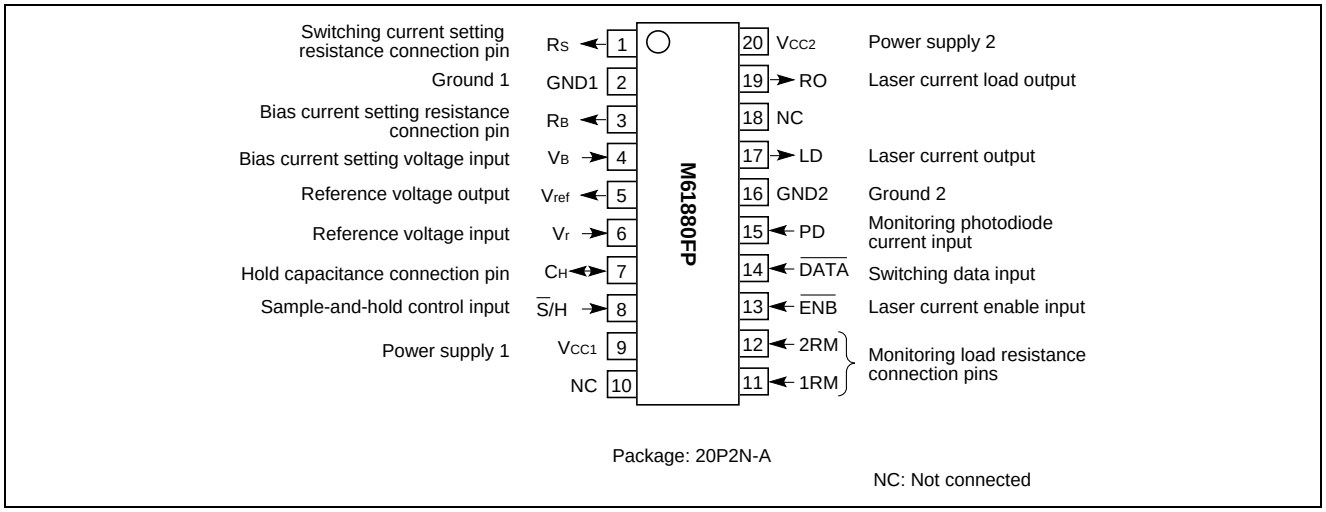
Features

- On-chip self-APC sample-and-hold circuit
  High-speed sampling circuit
  APC 1% variance response time = 1 µs (C = 0.047 µF)
  High-impedance hold circuit
  (1% error or less at C = 0.047 µF, t = 1 ms)
- High-speed switching (200 Mbps max.)
- High drive current (100 mA max.)
- Bias current settable (40 mA max.)
- 5 V single power supply

Application

Semiconductor laser diode application systems (LBPs, PPCs, optical communications, measuring instruments, etc.)

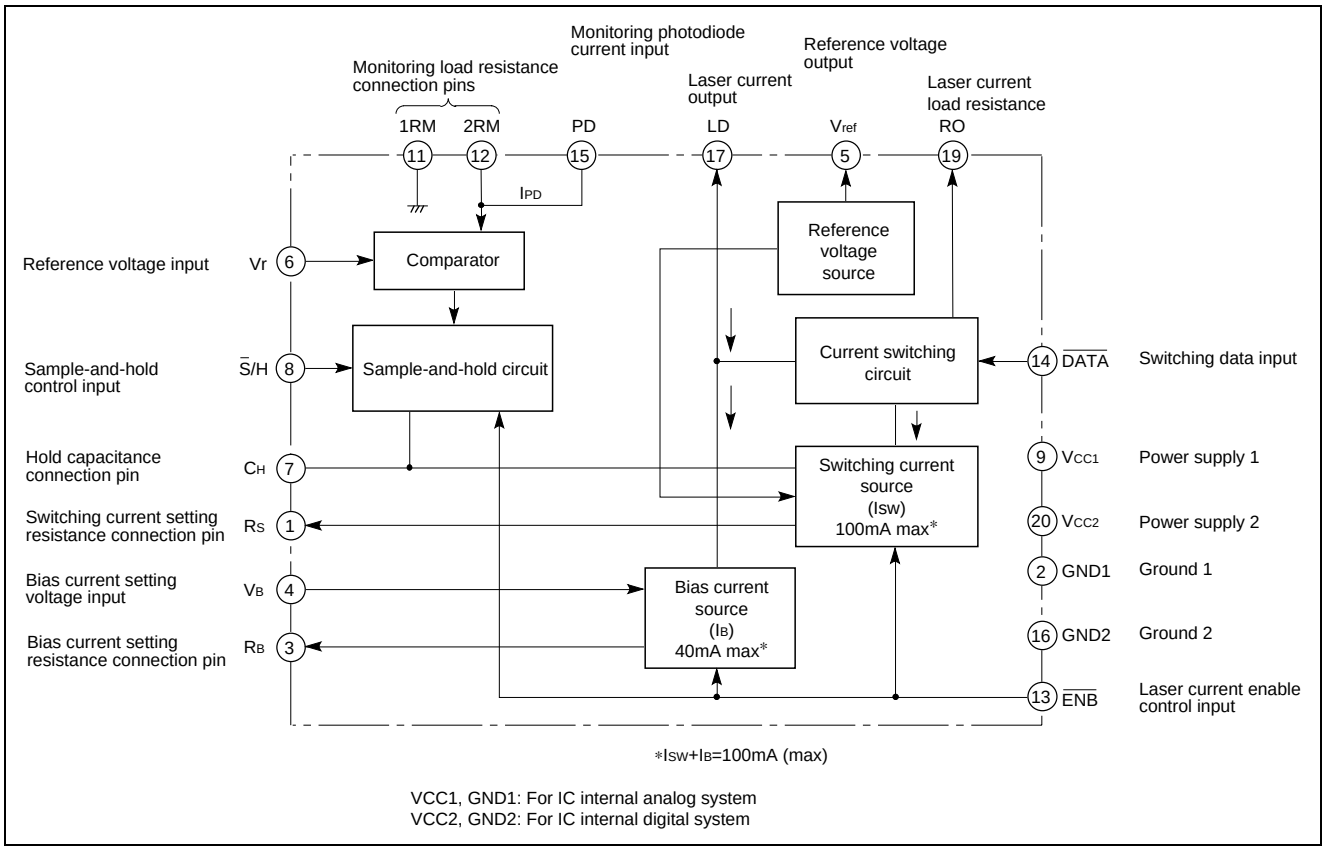
Pin Configuration (Top View)



Package: 20P2N-A

NC: Not connected

Block Diagram



Function Overview

The M61880FP is a semiconductor laser diode driver/controller that automatically performs drive and laser power control of a type of semiconductor laser diode in which the semiconductor laser diode (LD) anode and monitoring photodiode (PD) cathode are connected to the stem.

Laser power control operation is performed by connecting an external capacitance to the CH pin and applying a reference voltage to the Vr pin.

The PD current resulting from LD light emission flows to a resistance connected between 1RM and 2RM, and generates a voltage (VM). This VM voltage is compared with the voltage applied to the Vr pin, and if VM < Vr, the current from the CH pin is taken as a source current and an external capacitance is charged.

If VM > Vr, the current from the CH pin is taken as a sink current and the external capacitance charge is discharged.

This operation is performed when $\overline{S}$/H input = "L" and $\overline{DATA}$ input = "L" (sampling). When $\overline{S}$/H input = "H", the CH pin goes to the high-impedance state (hold) irrespective of the state of VM, Vr, and the $\overline{DATA}$ input.

The LD drive current is composed of switching current ISW controlled by $\overline{DATA}$ input and LD bias current IB unrelated to the $\overline{DATA}$ input state.

Pin Description

Pin No.	Symbol	Name	Function
1	Rs	Switching current setting resistance connection pin	Connects switching object current (ISW) setting resistance to GND.
2	GND1	Ground 1	Internal analog GND
3	RB	Bias current setting resistance connection pin	Connects bias current (IB) setting resistance to GND. Leave this pin open when IB is not used.
4	VB	Bias current setting voltage input	Bias current value (IB) is set by applying a voltage to this pin. Leave this pin open when IB is not used.
5	Vref	Reference voltage output	M61880 internal reference voltage (1.5 V typ.) output pin
6	Vr	Reference voltage input	Connected to non-reversed input pin of comparator in sample-and-hold circuit. Connect this pin to Vref pin when using M61880 internal reference voltage.
7	CH	Hold capacitance connection pin	Connects hold capacitance to GND. This pin is connected to sample-and-hold circuit output and ISW current source input in M61880.
8	$\overline{S}$/H	Sample-and-hold control input	Sampling when “H”, hold when “L”
9	Vcc1	Power supply 1	Internal analog power supply. Connected to positive power supply (+5 V).
10	NC	NC	Not connected to internal circuitry.
11, 12	1RM 2RM	Monitoring load resistance connection pins	Connects load resistance for converting monitor photodiode current to voltage between 1RM and 2RM. (1RM pin is connected to GND in IC.)
13	$\overline{ENB}$	Laser current enable input	When “H”, LD drive current source circuit is turned off. Also, CH pin is forcibly fixed at “L” level.
14	$\overline{DATA}$	Switching data input	ISW+IB current flows to laser diode when “+”, and IB current when “H”.
15	PD	Monitoring photodiode current input	Connects monitor photodiode anode.
16	GND2	Ground 2	Internal digital GND
17	LD	Laser current output	Connects semiconductor laser diode cathode.
18	NC	NC	Not connected to internal circuitry.
19	RO	Laser current load output	Connects laser current load resistance to Vcc.
20	Vcc2	Power supply 2	Internal digital power supply. Connected to positive power supply (+5 V).

Operation

1. Laser drive current setting method

The laser drive current consists of switching current ISW + bias current IB.

(1) Switching current ISW setting method

a. Decide the maximum current value ILD(MAX) to flow in the laser diode (LD). This is decided taking account of the LD type, dispersion, temperature changes, secular changes, etc.

b. Find ISW (initial set value) from the following equation.
ISW (initial set value) = ILD(MAX)/1.9

c. Find switching current setting resistance RS from the following equation.
R_S [kΩ] ≒ 30 × Vref (1.5V) [V] / I_{SW} (initial set value) [mA]

In this case the LD current can be controlled in a range of 10% to 90% of ISW (initial set value).

(2) Bias current IB setting method

Bias current IB [A] is set by deciding bias current setting resistance RB and bias current setting voltage VB.

$$I_B\ [A] \fallingdotseq V_B\ [A] / R_B\ [\Omega]$$

where $1.2\ V \le V_B \le Vcc - 2.7V$, I_B (max.) = 40mA

2. Switching operation

When $\overline{DATA}$ = "L", the LD drive current is ISW+IB, and when $\overline{DATA}$ = "H", the LD drive current is IB.

3. $\overline{ENB}$ input

In laser drive current control by $\overline{DATA}$ input, the drive current to the laser is controlled when the M61880 internal current source is on, while control by $\overline{ENB}$ turns LD drive current source operation on/off.

Power is turned on when $\overline{ENB}$ = "H", and the current secure is turned off when $\overline{ENB}$ = "L". When $\overline{ENB}$ = "H", the CH pin is forcibly fixed at the "L" level, and the capacitor connected to the CH pin is forcibly discharged.

When changing the $\overline{ENB}$ pin from "H" to "L", in order to prevent an abnormal current from flowing in the LD, drive the $\overline{DATA}$ pin to the "H" state, then wait 10 µsec or more after the $\overline{ENB}$ pin changes from "H" to "L" before changing the $\overline{DATA}$ pin from "H" to "L".

4. Internal reset operation

The M61880 incorporates a reset circuit for preventing an overcurrent in the laser when power is turned on. In the range VCC < 3.5 V (typ.), the internal current source is turned off and the CH pin is forcibly fixed at the "H" level.

5. RO pin

The RO pin connects the drive current load resistance, and a currently virtually equal to ISW flows from this pin.

The load resistance is connected between this pin and VCC, thereby reducing power consumption in the IC.

For reasons relating to circuit operation, the voltage at this pin must be 2.5 V or higher. Therefore, if the maximum value of ISW is designated ISW(max.), maximum value RO(max.) of load resistance RO is as follows:

$$R_S\ (max.)\ [\Omega] = \frac{Vcc\ (min.)\ [V] - 2.5\ [V]}{I_{SW}\ (max.)\ [A]}$$

For example, if VCC(min.) = 4.75 V and ISW(max.) = 100 mA, RO(max.) = 22 Ω. That is to say, when the RS value is set so that ISW is a maximum of 100 mA, RO must not exceed 22Ω.

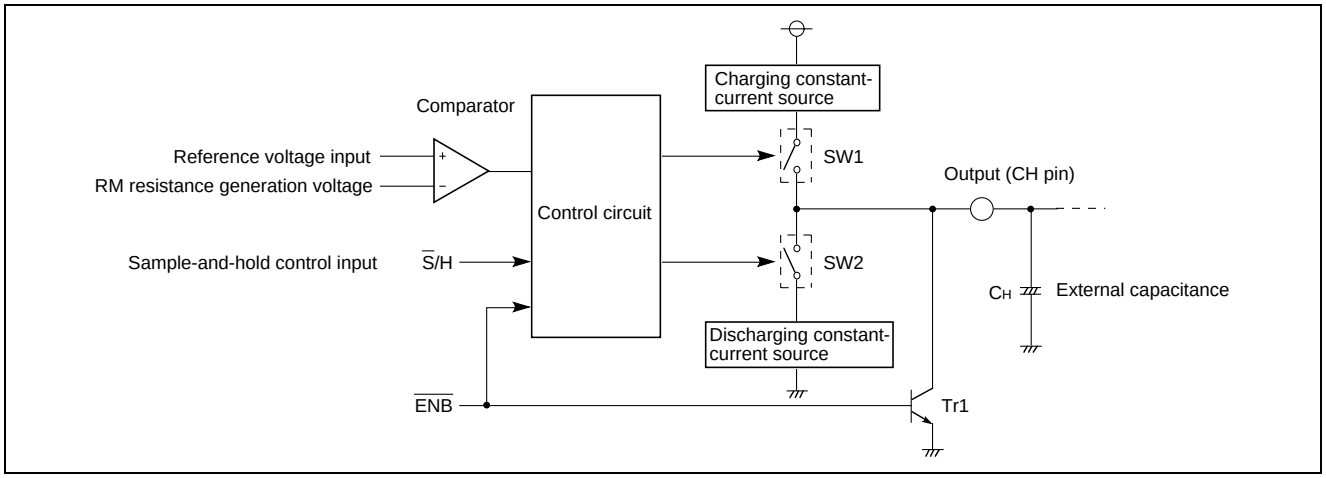
6. Sample-and-hold circuit

(1) Overview of circuit operation

The operation of the sample-and-hold circuit incorporated in the M61880 is outlined below.

The PD current resulting from LD light emission flows to resistance RM connected between 1RM and 2RM, and generates a voltage (VM). This VM voltage is compared with the voltage applied to the Vr pin, and if VM < Vr, the current from the CH pin is taken as a source current and an external capacitance is charged. If VM > Vr, the current from the CH pin is taken as a sink current and the external capacitance charge is discharged.

This operation is performed when $\overline{S}$/H input = "L" and $\overline{DATA}$ input = "L" (sampling). When $\overline{S}$/H input = "H", the CH pin goes to the high-impedance state (hold) irrespective of the state of VM, Vr, and the $\overline{DATA}$ input.



Conceptual Diagram of Sample-and-Hold Circuit

Operation Function Table

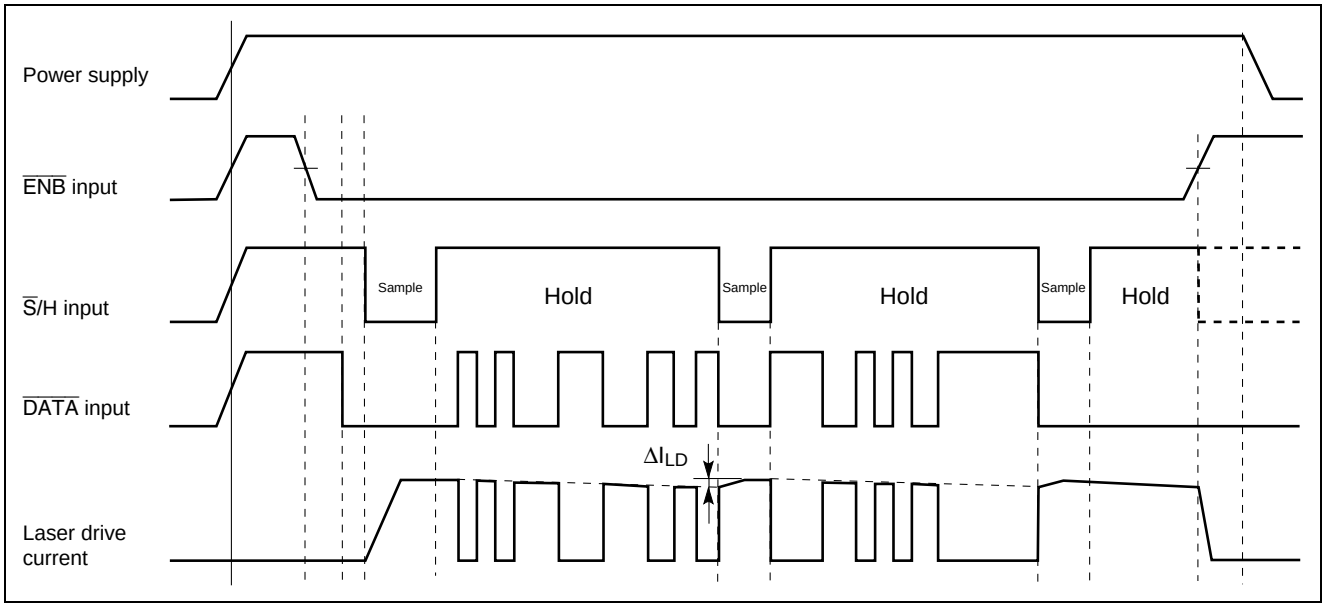
Input				Switch State			
ENB	S/H	DATA	VM, Vr	SW1	SW2	Tr1	Output (CH Pin)
H	X	X	X	OFF	OFF	ON	Fixed at "L"
L	H	X	X	OFF	OFF	OFF	High-impedance state (hold)
L	L	H	X	OFF	OFF	OFF	High-impedance state (hold)
		L	VM < Vr	ON	OFF	OFF	Current source (sample)
			VM > Vr	OFF	ON	OFF	Current sink (sample)

X: Don't Care

(2) APC timing chart

An example of a timing chart of APC operation by means of the sample-and-hold control signals is shown below.

In this example, a case is shown in which the direction of the CH pin leakage current in the hold state is assumed to be the direction of flow to the M61880 (forward direction).



Example of Sample-and-Hold Type APC Circuit Operation Timing Chart

7. VCC and GND pins

Power supply related pins are the VCC1 and VCC2 pins and the GND1 and GND2 pins. In terms of the internal circuitry , these are connected as follows. (Basically, a single power supply should be used.)

VCC1, GND1: Connected to analog system.
VCC2, GND2: Connected to digital system.

The main points to be noted with regard to actual wiring are as follows.

(1) Make the wiring as wide as possible and avoid lengthy, circuitous wiring.

(2) Locate an electrolytic capacitor for voltage stabilization close to VCC1 and GND1.

(3) Locate a bypass capacitor close to VCC2 and GND2.

Also ensure that M61880 power is supplied while laser diode power is being supplied.

Note on Wiring of Peripheral Elements

Peripheral elements necessary for M61880 operation should be located as close as possible to the M61880.

Power Consumption Calculation Method

M61880 power consumption P is given approximately by the following equation:

$$P = Icc.\times.Vcc.+.I(RO) \times.V(RO) +.I(LD) \times V(LD)$$

where V(RO): RO pin voltage V(LD): LD pin voltage

I(RO): RO pin load current I(LD): LD pin load current

For example, when VCC = 5.25 V, V(RO) = V(LD) = 2.5 V, and I(RO) = I(LD) = 100 mA, the power consumption values when the laser is on and off are as follows.

(1) When laser is on, ($\overline{DATA}$ = “L”, ICC = 55 mA)

$$PON = 55.\times.5.25.+.0 + 100 \times.2.5 = 538.8 \text{ (mW)}$$

(2) When laser is off, ($\overline{DATA}$ = “H”, ICC = 55 mA)

$$PON = 55.\times.5.25.+.100 \times.2.5 = 538.8 \text{ (mW)}$$

Absolute Maximum Ratings

Item		Symbol	Ratings	Unit	Conditions
Power supply voltage		VCC	-0.3 to +5.5	V	
Input voltage	CH, Vr	VI	-0.3 to Vcc	V	
	$\overline{DATA}$, $\overline{ENB}$, $\overline{S}$/H		-0.3 to Vcc		
Output voltage	RO	Vo	-0.3 to Vcc	V	
Switching current		Isw	120	mA	
Bias current		IB	50	mA	
Power consumption		Pd	980	mW	When mounted on board. When Ta = 25°C (Note)
Storage temperature		Tstg	-60 to +150	°C	

Note: When Ta ≥ 25°C, 9.8 mW/°C derating should be applied.

Recommended Operating Conditions

(Unless otherwise noted, Ta = -20ºC to +70ºC)Absolute Maximum Ratings

		Limits			
Item	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	Vcc	4.75	5.0	5.25	V
Switching current	Isw			100	mA
Bias current	IB			40	mA
Operating ambient temperature	Topr	–20		70	°C

Note: ISW+IB ≤ 100 mA

Electrical Characteristics

(Unless specified otherwise noted, VCC = 5 V ±5%, Ta = -20ºC to +70ºC)

Item		Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
"H" input voltage	$\overline{DATA}$	VIH	2.0			V	
	$\overline{ENB}$, S/H		2.0			V	
"L" input voltage	$\overline{DATA}$	VIL			0.8	V	
	$\overline{ENB}$, S/H				0.8	V	
Reference voltage input	Vr	Vr	0.35	1.5	2.0	V	
Reference voltage output	Vref	Vref	1.4	1.5	1.6	V	Io = ±10µA
	Temperature coefficient			0.1		mV/°C	Ta = –20 to 25°C
				–0.1			Ta = 25 to 70°C
Operating voltage range	LD	VLD	2.5		Vcc	V	ILD = 75mA
Effective voltage upper limit	CH	VI	2.7	3.0		V	
"H" output voltage	CH	VOH	Vcc–1.6			V	$\overline{ENB}$ = "L", IOH = (–0.6mA)
"L" output voltage	CH	VOL			0.6	V	$\overline{ENB}$ = "L", IOL = (0.6mA)
Input voltage	$\overline{DATA}$, $\overline{ENB}$	II			20	µA	VI = 2.7V
			–0.2			mA	VI = 0.4V
Switching current (Note)	LD	Isw		75		mA	CH = 3.5V, Rs = 1.2kΩ, VLD = 3V
Bias current (Note)	LD	IB		20		mA	VB = 1.4V, RB = 70kΩ, VLD = 3V
Load charge current	CH	Icg	–0.2	–0.1	–0.66	mA	$\overline{ENB}$ = "L", Vo = (0.6 to Vcc–1.6V)
Load discharge current	CH	Idg	0.66	1.0	2.0	mA	$\overline{ENB}$ = "L", Vo = (0.6 to Vcc–1.6V)
Off-state output current	CH	Ioz	–0.5		0.5	µA	Vo = 2.0 to 3.0V, hold state
Off output current	LD	LOFF			50	µA	$\overline{ENB}$ = "L", $\overline{DATA}$ = "H", Isw = 50mA
					50	µA	$\overline{ENB}$ = "H", $\overline{DATA}$ = "L", Isw = 50mA
Power supply current		Icc		43	63	mA	Vcc = 5.25V, $\overline{ENB}$ = 0V, CH = 2.5V, VB = 1.5V, Rs = 820Ω, RB = 75 Ω Ro = LD = 5.0V, $\overline{DATA}$ = 0V
				43	63		$\overline{DATA}$ = 4.5V

* Reference values are values when Ta = 25ºC and VCC = 5 V.

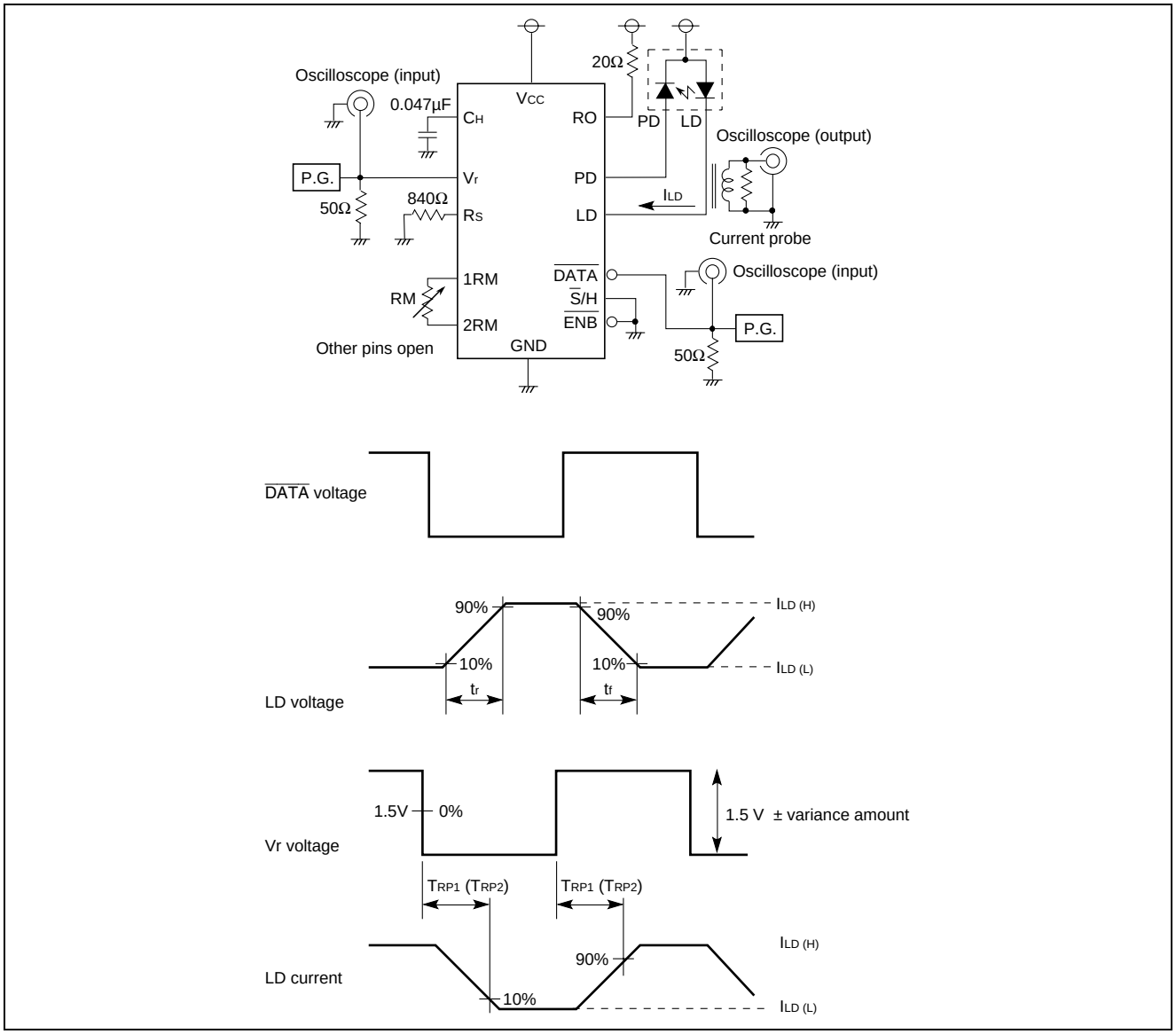
Note: These items indicate input voltage/output current conversion characteristics. The M61880 should be used with ISW and IB within the Specification Value range given in "Recommended Operating Conditions."

Switching Characteristics

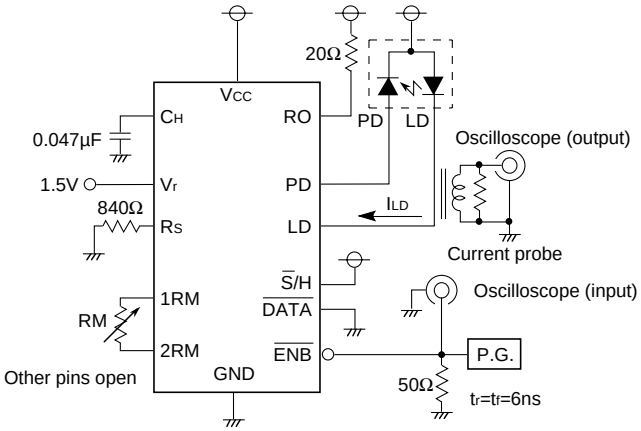
(Unless specified otherwise noted, Ta = 25ºC and VCC = 5 V)

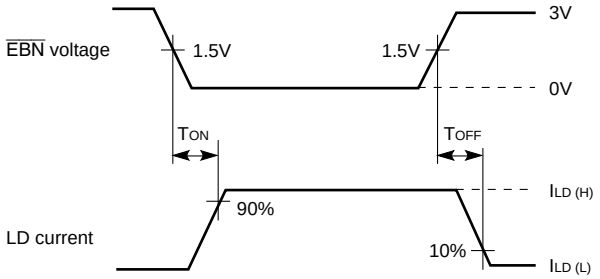
Item	Symbol	Test Pins		Limits			Unit	Test Conditions
		Input	Output	Min.	Typ.	Max.		
Operating frequency	fop			—	100	2.0	Mbps	
LD current rise time (*)	tr	$\overline{DATA}$ voltage	LD current	—	1.0	2.0	nsec	ILD (H) = 50mA, ILD (L) = 0mA Rs = 840Ω, CH = 0.047µF, APC adjustment; RM = adjustment (CH = 2.5V), Vr = 1.5V (Note 1)
LD current fall time (*)	tf	$\overline{DATA}$ voltage	LD current		1.0		nsec	
APC circuit response time 1 (1% variance response time)	tRP1	Vr voltage	LD current		1		µsec	ILD (H) = 50mA, Rs = 840Ω, CH = 0.047µF, $\overline{DATA}$ = 0V APC adjustment; RM = adjustment (CH = 2.5V), Vr = 1.5V ± 0.5% (Note 1)
APC circuit response time 2 (50% variance response time)	tRP2	Vr voltage	LD current		3		µsec	
Circuit on time	tON	$\overline{ENB}$ voltage	LD current			350	µsec	ILD (H) = 50mA (Note 2)
Circuit off time	tOFF	$\overline{ENB}$ voltage	LD current			5	µec	ILD (H) = 50mA (Note 2)

Note 1: Test Circuit



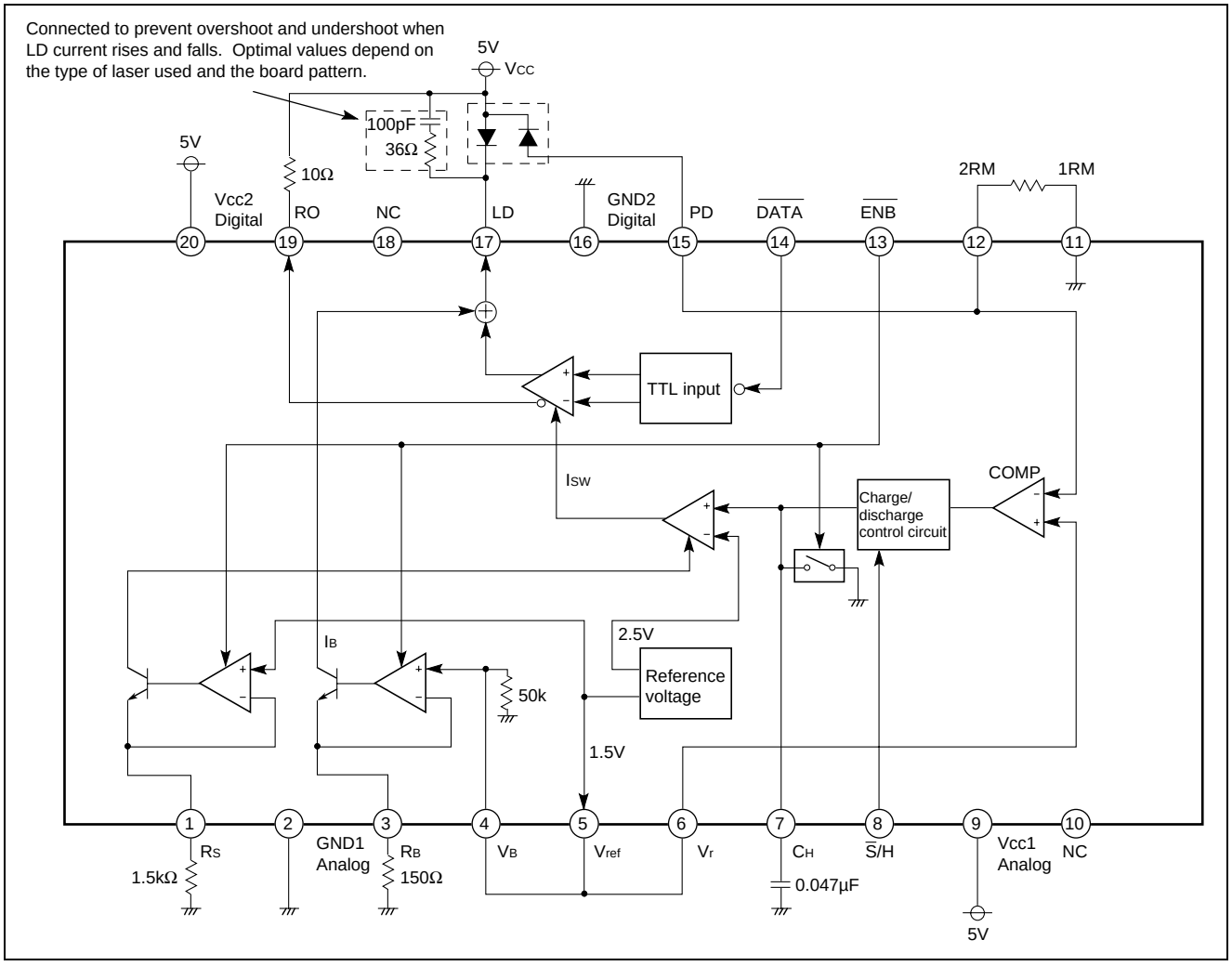
Note 2: Test Circuit





Application Example

1. Example of sample-and-hold type self-APC circuit



2. Example of controlling sample-and-hold circuit by means of $\overline{\text{DATA}}$ signal

When the M61880 is used in optical communications, etc., (when the $\overline{\text{S}}$/H signal cannot be supplied), the $\overline{\text{DATA}}$ signal can be used as a sample-and-hold control signal.

In this case, the $\overline{\text{S}}$/H pin should be fixed at "L". If value CH of the hold capacitor connected to the CH pin is 0.047µF, switching at around 20 Mbps is possible.

3. Examples of varying LD switching drive current by means of external control

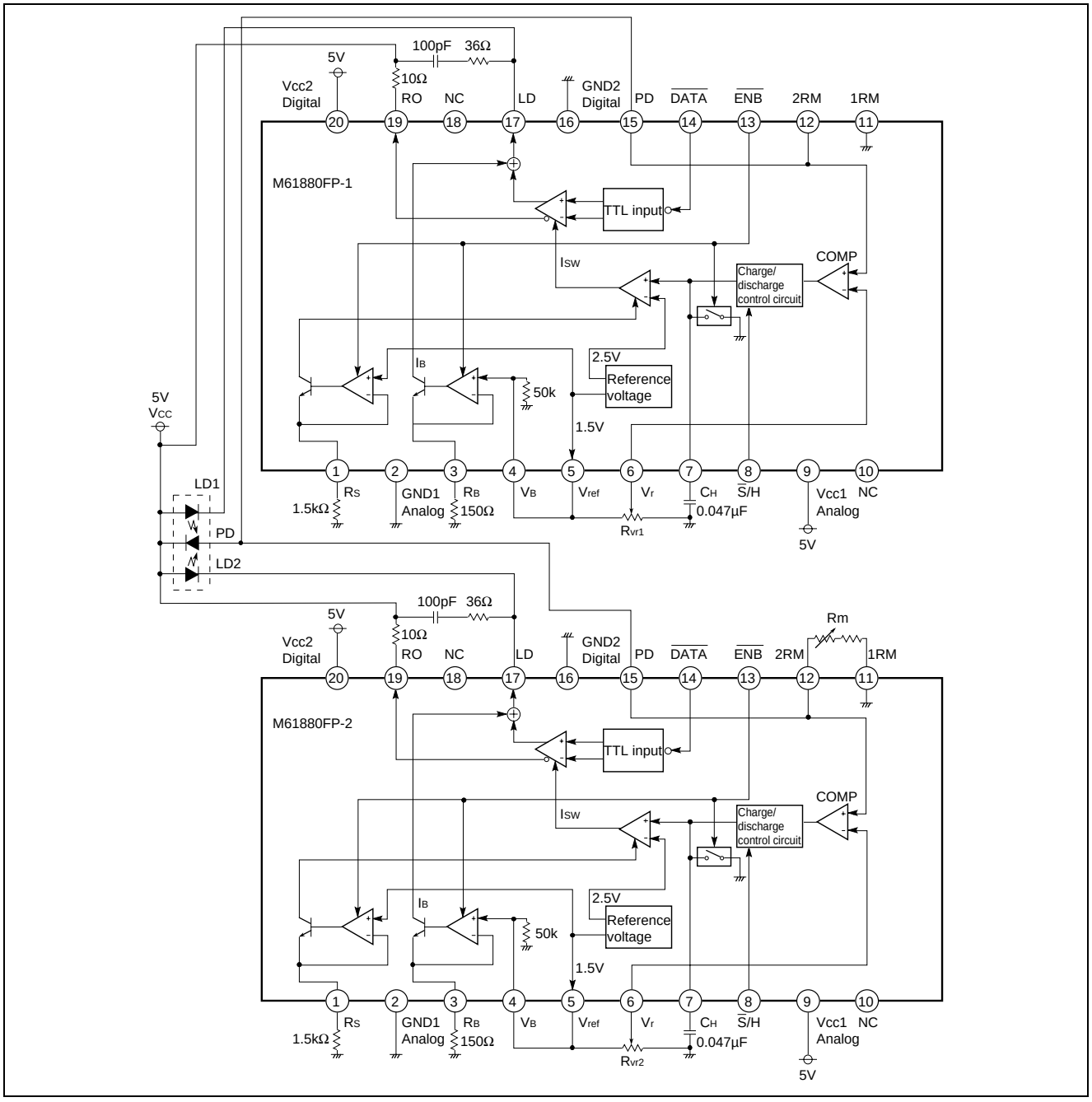
(1) Varying the monitoring load resistance value (resistance connected between pins 11 and 12)

The LD drive current can be varied by varying the resistance between pins 11 and 12 in the circuit in 1. above.

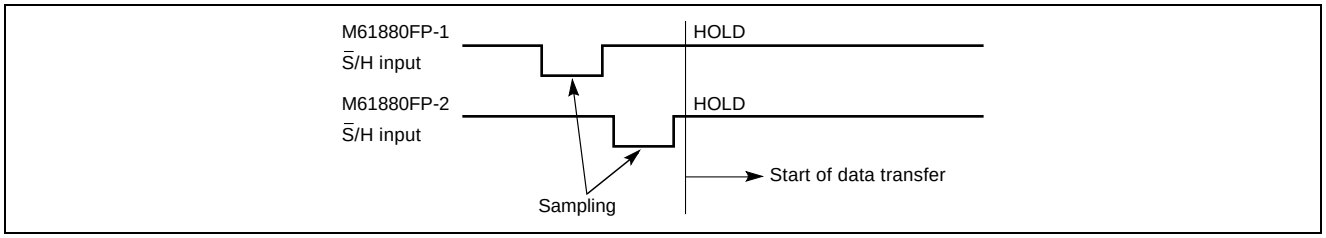
(2) Varying the voltage applied to the Vr pin

The LD drive current can be varied by applying an external voltage (within the reference voltage input range) to pin 6 in the circuit in 1. above. A maximum multiplication factor of 2/0.35 = 5.7 times can be obtained as the LD drive current ratio in this case.

4. Example of sample-and-hold type self-APC circuit
(Controlling two laser diodes)



Sample-and-Hold Timing



Sample-and-Hold Type APC Operation

A timing chart for a case where a sample-and-hold type APC circuit is configured using an M61880FP (Figure 1) is shown in Figure 2 on the following page.

The operation of a sample-and-hold type APC circuit will be described here using the timing chart in Figure 2. It is assumed that the laser drive current is set to 50 mA (bias current = 0 mA), and the values shown in Figure 1 are used as constants required for calculation purposes.

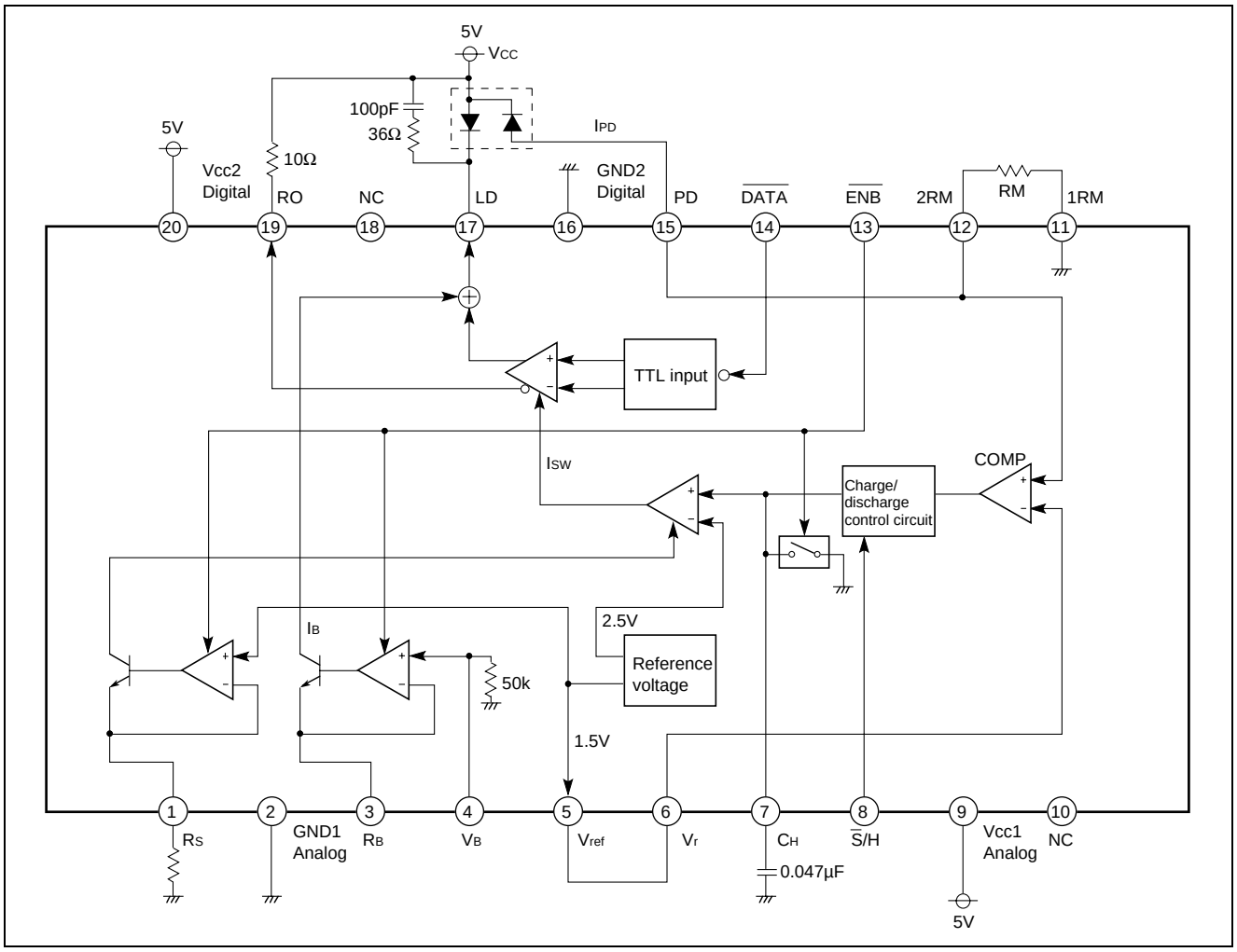


Figure 1 Example of Sample-and-Hold Type APC Circuit Application

1. Initial sampling period (T1)

When sampling starts, the CH pin voltage is 0 V, and therefore the laser diode (LD) is not emitting light. Consequently, the voltage of the COMP input pin (pin 12) is also 0 V. Next, COMP starts charging the hold capacitor connected to CH (current also starts flowing in the LD in proportion to the rise of the CH pin voltage, and the pin 12 voltage also rises), and charging is performed until the pin 12 voltage reaches comparison voltage Vr.

In this case, the CH pin voltage rises from 0 V to VCH due to the M61880FP's CH pin load charge current (Icg). Time t required for this is given by the following equation.

$$t = \frac{C_H \times VCH}{Icg} \quad \text{..... Equation (1)}$$

In Equation (1), if CH = 0.047µF, VCH = 2.5 V, and Icg = 0.66 mA (*), then t = 178µs.

* Minimum Icg specification value in "Electrical Characteristics" in this Specification.

2. Hold periods (T2, T4)
In these periods, the CH pin goes to the high-impedance state. However, the charge current does not become absolutely 0, and a slight leakage current is present. The hold capacitor is charged or discharged by the CH pin off-state leakage current (Ioz).

Assuming that a leakage current (Ioz) is generated in the direction in which the hold capacitor is discharged, the change in the CH pin current (ΔV) is given by the following equation.

$$\Delta V = \frac{Ioz\ (0.5\mu A) \times T2\ (4)}{C_H \times (0.047\mu F)} \quad \text{..... Equation (2)}$$

(T2(4) is the hold time.)

When the CH pin voltage decreases by ΔV, the laser drive current also decreases.

3. Sampling periods (T3, T5)
In these periods, the LD light quantity that changed during a hold period (T2, T4) is corrected.

Taking only the influence of the CH pin leakage current into consideration (actually, LD temperature variations also have an effect), making substitutions of Ioz = 0.5μA, T = 1 ms, and CH = 0.047μF in Equation (2) gives a result of ΔV = 10 mV.

The time required to compensate for this ΔV value (10 mV) is given by the following equation.

$$t = \frac{C_H \times \Delta V}{Icg} \quad \text{..... Equation (3)}$$

From Equation (3), t = 0.7μs.

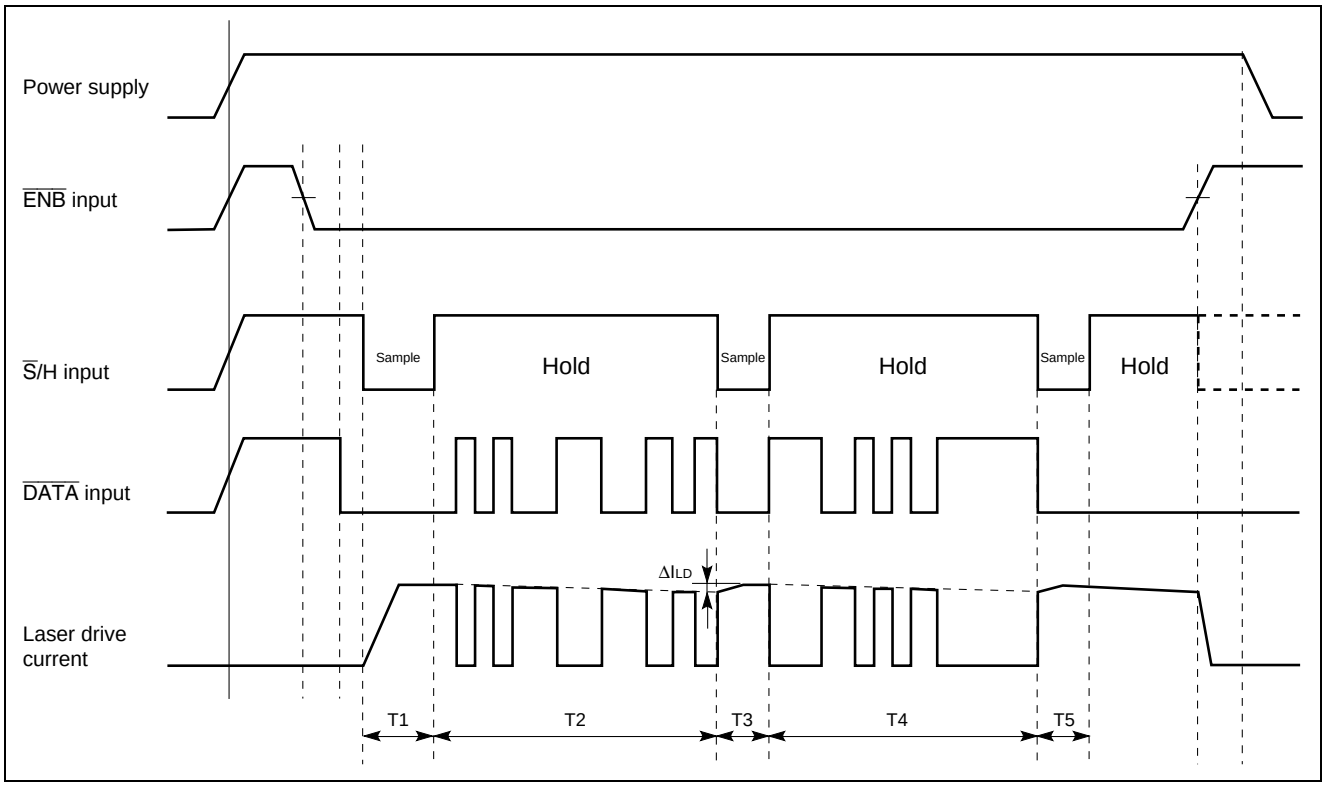


Figure 2 Sample-and-Hold Type APC Circuit Operation Timing Chart

Description of Laser Switching Current Setting Circuit

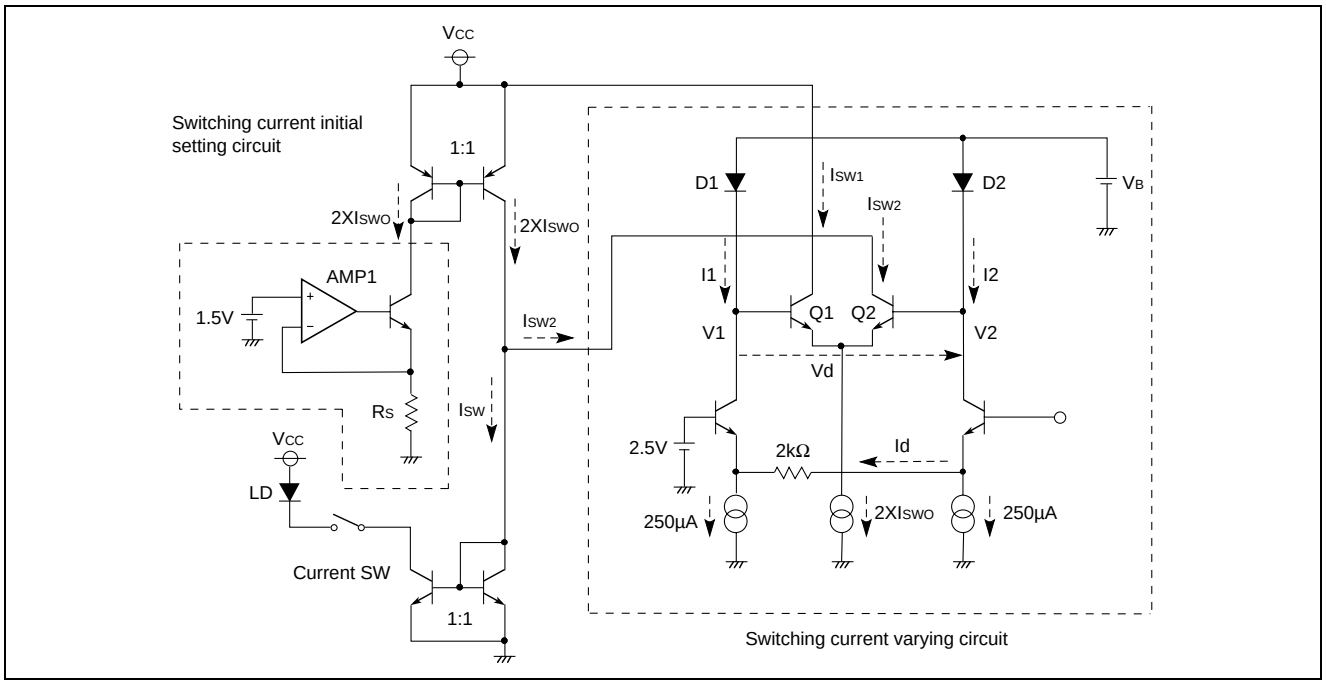


Figure 1 Switching Current Setting Equivalent Circuit

1. Switching current initial setting circuit

The switching current initial set value is set by switching current setting resistance Rs in a V-I conversion circuit using an op-amp.

$$I_{SWO}\,[mA] = 30 \times \frac{V_{ref}\,(1.5V)\,[V]}{R_S\,[k\Omega]} \quad \text{..... (1)}$$

2. Switching current varying circuit

If the potential difference between the CH pin voltage and internal reference voltage is designated ΔV (= VCH – 2.5 V), Id flowing in a 2 kΩ resistance due to this ΔV voltage is as follows.

$$I_d = \frac{\Delta V}{2k\Omega} \quad \text{..... (2)}$$

Therefore, the I1 and I2 currents are given by the following equations.

$$\begin{cases} I1 = 250\ \mu A - Id \\ I2 = 250\ \mu A - Id \end{cases} \quad \text{..... (3)}$$

Next, the relationship between I1, I2, ISW1, and ISW2 due to a Gilbert circuit comprising D1, D2, Q1, and Q2, is given by the following equation.

$$\frac{I1}{I2} = \frac{Isw1}{Isw2} \quad \text{..... (4)}$$

Also, the relationship between ISW1, ISW2, and ISW0 is given by the following equation.

$$Isw1 + Isw2 = 2 \bullet Iswo \quad \text{..... (5)}$$

Finding ISW2 from Equations (4) and (5),

$$I_{SW2} = 2 \bullet I_{SWO} \times \frac{I1}{I1 + I2} \quad \text{..... (6)}$$

Meanwhile, ISW can be expressed as follows.

$$Isw = 2 \bullet Iswo - Isw2 \quad \text{..... (7)}$$

The relationship between ISW and ΔV is found as shown below.

Substituting Equation (6) in Equation (7),

$$Isw = 2 \bullet Iswo \left(\frac{I2}{I1 + I2} \right) \quad \text{..... (8)}$$

and further substituting Equation (3),

$$Isw = Iswo \left(1 + \frac{Id}{250\mu A}\right) \quad \text{..... (9)}$$

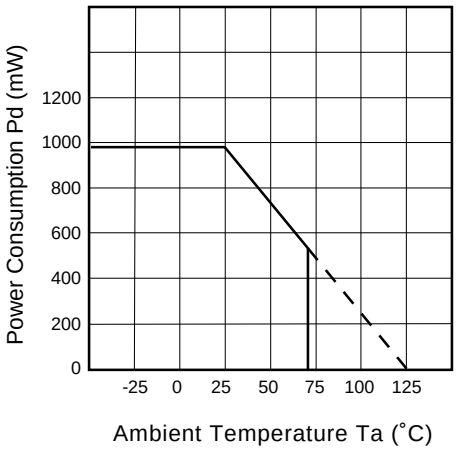
Next, substituting Equation (2) gives the relationship between ISW and ΔV as follows.

$$Isw = Iswo \left(1 + \frac{\Delta V/2k\Omega}{250\mu A}\right) \quad \text{..... (10)}$$

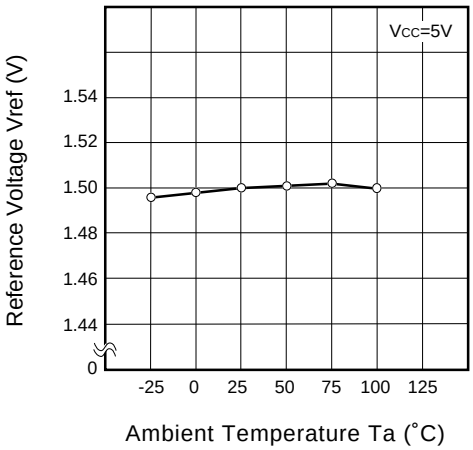
A characteristic curve of the CH pin voltage and switching current is shown toward the end of “Electrical Characteristic Graphs” following.

Electrical Characteristic Graphs

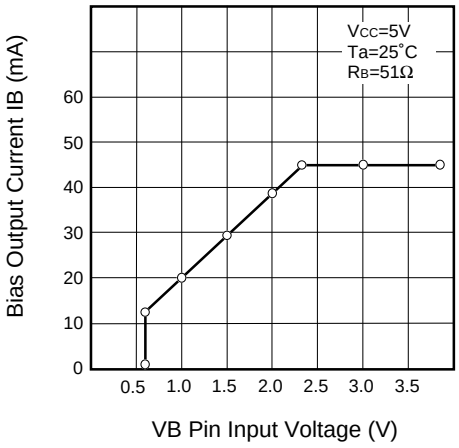
Thermal Reduction Curve



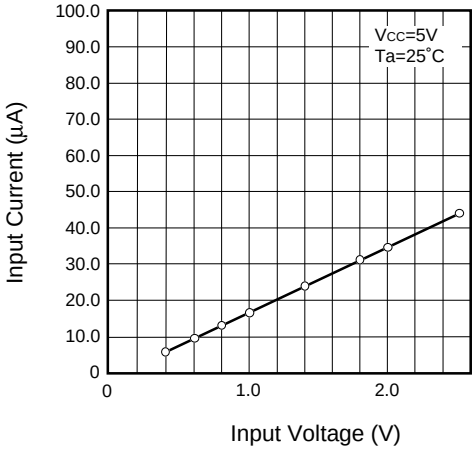
Reference Voltage - Temperature Characteristic



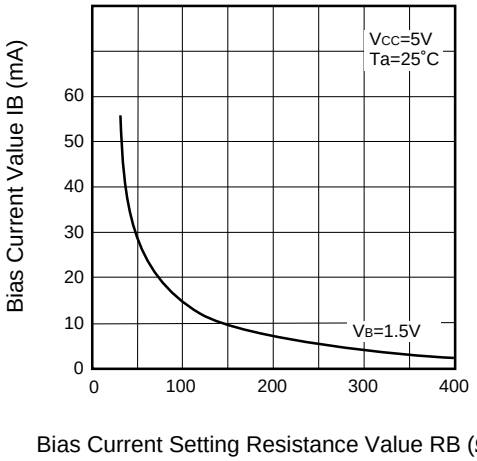
Bias Setting Pin Input Voltage - Output Characteristic



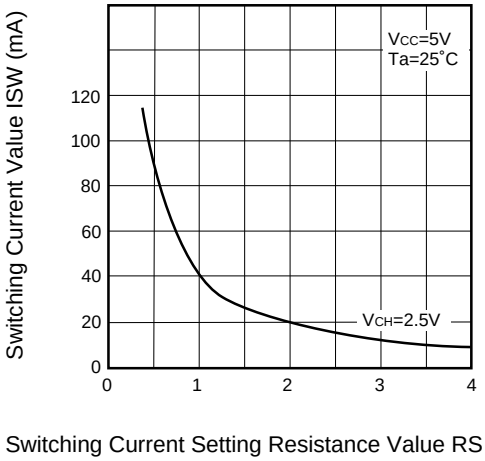
VB Pin Input Voltage - Current Voltage Characteristic



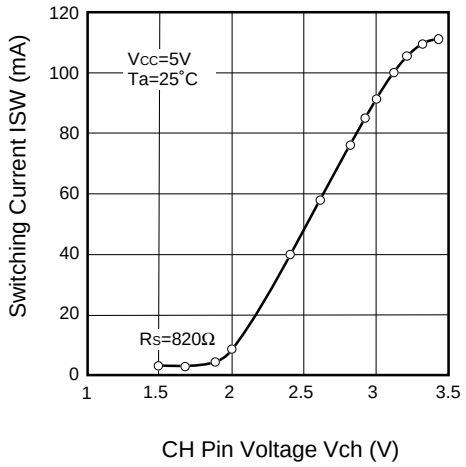
Bias Current Setting Resistance - Current Characteristic



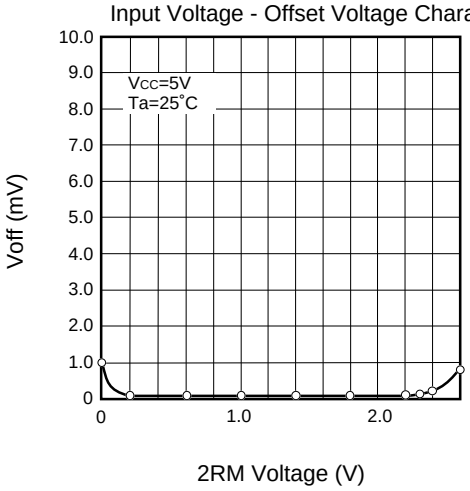
Switching Current Setting Resistance - Current Characteristic



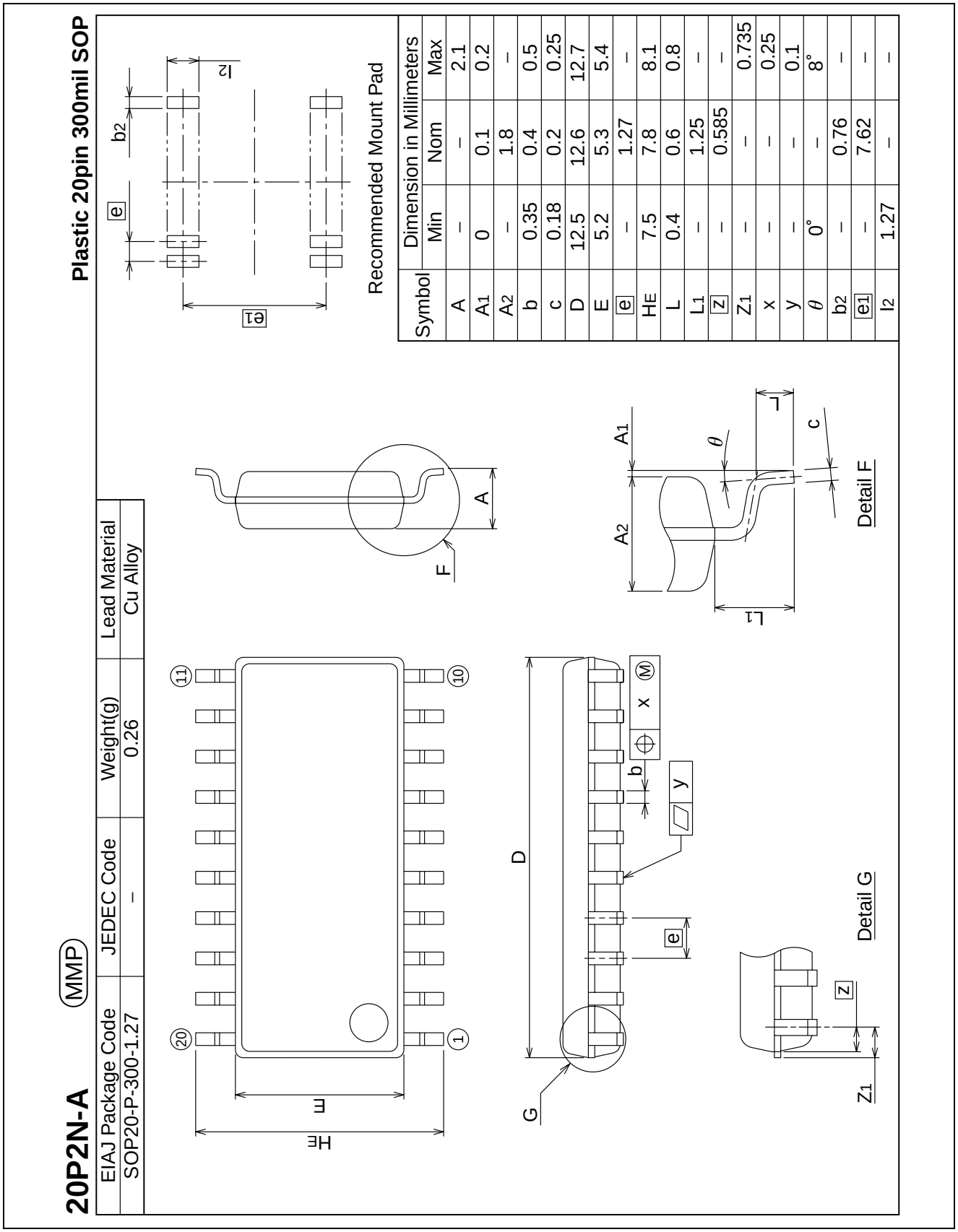
CH Pin Voltage - Switching Current Characteristic



APC Comparator Input Voltage - Offset Voltage Characteristic



Package Dimensions



Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	2.1
A_1	0	0.1	0.2
A_2	–	1.8	–
b	0.35	0.4	0.5
c	0.18	0.2	0.25
D	12.5	12.6	12.7
E	5.2	5.3	5.4
e	–	1.27	–
H_E	7.5	7.8	8.1
L	0.4	0.6	0.8
L_1	–	1.25	–
Z	–	0.585	–
Z_1	–	–	0.735
x	–	–	0.25
y	–	–	0.1
θ	0°	–	8°
b_2	–	0.76	–
e_1	–	7.62	–
l_2	1.27	–	–

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