FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-16602-1E

32-bit Microcontroller

CMOS

FR60 MB91460 Series

MB91461

■ DESCRIPTION

MB91461 is a line of the general-purpose 32-bit RISC microcontrollers designed for embedded control applications such as consumer devices and vehicle system, which require high-speed real-time processing. MB91461 uses the FR60 CPU compatible with the FR family* CPUs.

MB91461 contains the LIN-UART and CAN controller.

* : FR, the abbreviation of FUJITSU RISC controller, is a line of products of FUJITSU Limited.

■ FEATURES

- **FR60 CPU**
  - 32-bit RISC, load/store architecture, five-stage pipeline
  - Maximum operating frequency : 80 MHz (oscillation frequency 20 MHz, oscillation frequency 4 multiplier (PLL clock multiplication method))
  - 16-bit fixed-length instructions (basic instructions)
  - Instruction execution speed : 1 instruction per cycle
  - Instructions including memory-to-memory transfer, bit manipulation instructions, and barrel shift instructions: Instructions suitable for embedded applications
  - Function entry/exit instructions and register data multi load store instructions: Instructions supporting C language
  - Register interlock function : Facilitating assembly-language coding
  - Built-in multiplier with instruction-level support

    Signed 32-bit multiplication : 5 cycles

    Signed 16-bit multiplication : 3 cycles
  - Interrupt (PC/PS saving) : 6 cycles (16 priority levels)

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Be sure to refer to the “Check Sheet” for the latest cautions on development.

“Check Sheet” is seen at the following support page
URL : http://www.fujitsu.com/global/services/microelectronics/product/micom/support/index.html

“Check Sheet” lists the minimal requirement items to be checked to prevent problems beforehand in system development.

FUJITSU

- Harvard architecture enabling simultaneous execution of both program access and data access
- Instructions compatible with the FR family

• Internal peripheral resources
- MB91461 does not contain the ROM and flash memory.
- Internal RAM capacity : Instruction cache 4 Kbytes + 64 Kbytes (Instruction/data common RAM)
- General-purpose port : Maximum 72 ports
- DMAC (DMA Controller)
  Maximum of 5 channels for simultaneous operation is possible. (1 channel for external-to-external)
  3 transfer sources (external pin/internal peripheral/software)
  Activation source can be selected using software.
  Addressing mode with 32-bit full address indication (increment/decrement/fixed)
  Transfer mode (demand transfer/burst transfer/step transfer/block transfer)
  Fly-by transfer support (between external I/O and memory)
  Transfer data size selection 8/16/32-bit
  Multi-byte transfer enabled (by software)
  DMAC descriptor in I/O areas (200_H to 240_H, 1000_H to 1024_H)
- A/D converter (sequential comparison)
  10-bit resolution: 13 channels
  Conversion time: 1 µs (peripheral macro operation clock at 16.67 MHz)
- External interrupt input: 16 channels
  Pins shared with RX pins of CAN0 and CAN1
- Bit search module (for REALOS)
  Function of searching for the first “0” data/ “1” data/change bit position in 1 word from the MSB (upper bit)
- LIN-UART (full duplex double buffer): 7 channels
  Clock synchronous/asynchronous selectable
  Sync-break detection
  Internal dedicated baud rate generator
- I^2C* bus interface (400 kbps supported): 3 channels
  Master/slave sending and receiving
  Arbitration function, clock synchronization function
- CAN controller (C-CAN) : 2 channels
  Maximum transfer speed : 1 Mbps
  32 sent/received message buffers
- 16-bit PPG timer : 8 channels
- 16-bit reload timer : 5 channels
- 16-bit free-run timer : 4 channels (1 channel each for ICU and OCU)
- Input capture : 4 channels (work with free-run timer)
- Output compare : 4 channels (work with free-run timer)
- Watchdog timer
  Watchdog reset output pin available
- Real-time clock
- Low-power consumption mode: Sleep/stop/shutdown mode function

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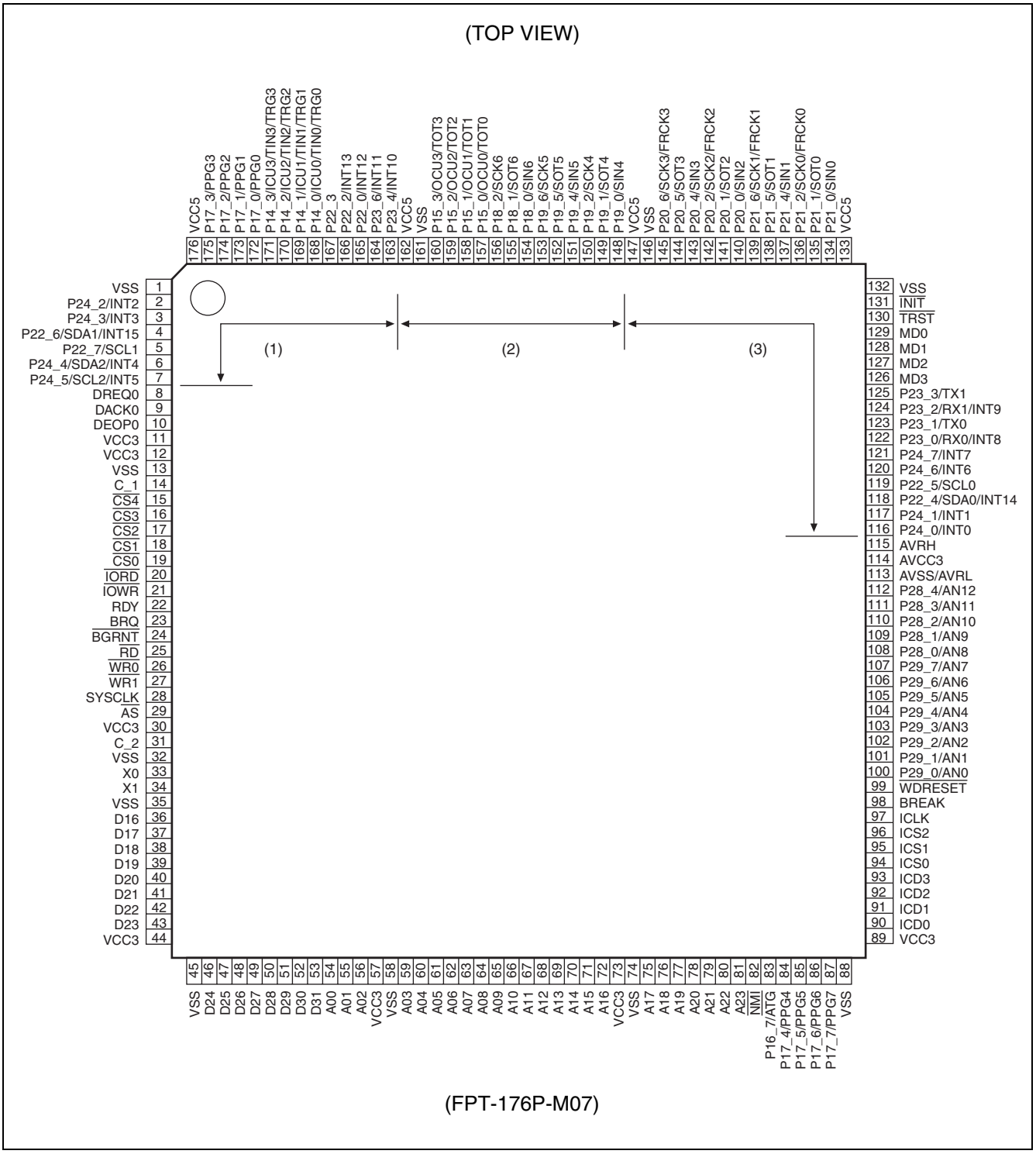
- Package : LQFP-176 (FPT-176P-M07)
- CMOS 0.18 μm technology
- 3 V/5 V power supplies [Internal logic is kept at 1.8 V by step-down circuit, some I/Os have the withstand voltage of 5.0 V]
- Operating temperature range : between − 40°C and + 85°C

* : Purchase of Fujitsu I²C components conveys a license under the Philips I²C Patent Rights to use, these components in an I²C system provided that the system conforms to the I²C Standard Specification as defined by Philips.

■ PIN ASSIGNMENT



Note : (1) to (3) are 3.3 V/5 V pin supported pin, and can set 3.3 V and 5 V to the voltage in each block. I²C pin in (1) can be inputted at 5 V power supply. However, 3.3 V of the input threshold value is used as the standard value regardless of the power supply voltage.
If 5 V is set in (1) or (2), also set 5 V to (3).

■ PIN DESCRIPTION

Pin no.	Pin name	I/O	I/O circuit type*	Function
2	P24_2	I/O	D	General-purpose input/output port
	INT2			External interrupt input pin
3	P24_3	I/O	D	General-purpose input/output port
	INT3			External interrupt input pin
4	P22_6	I/O Open Drain	C	General-purpose input/output port
	SDA1			I²C bus data input/output pin
	INT15			External interrupt input pin
5	P22_7	I/O Open Drain	C	General-purpose input/output port
	SCL1			I²C bus clock input/output pin
6	P24_4	I/O Open Drain	C	General-purpose input/output port
	SDA2			I²C bus data input/output pin
	INT4			External interrupt input pin
7	P24_5	I/O Open Drain	C	General-purpose input/output port
	SCL2			I²C bus clock input/output pin
	INT5			External interrupt input pin
8	DREQ0	I	H	DMA external transfer request input
9	DACK0	O	H	DMA external transfer acknowledge output
10	DEOP0	O	H	DMA external transfer EOP (End of Process) output
15	$\overline{CS4}$	O	H	Chip select 4 output
16	$\overline{CS3}$	O	H	Chip select 3 output
17	$\overline{CS2}$	O	H	Chip select 2 output
18	$\overline{CS1}$	O	H	Chip select 1 output
19	$\overline{CS0}$	O	H	Chip select 0 output
20	$\overline{IORD}$	O	H	Read strobe output at DMA fly-by transfer
21	$\overline{IOWR}$	O	H	Write strobe output at DMA fly-by transfer
22	RDY	I	H	External ready input
23	BRQ	I	H	External bus open request input
24	$\overline{BGRNT}$	O	H	External bus open acknowledge output
25	$\overline{RD}$	O	H	External read strobe output
26	$\overline{WR0}$	O	H	External write strobe output
27	$\overline{WR1}$	O	H	External write strobe output
28	SYSCLK	O	H	System clock output
29	$\overline{AS}$	O	H	Address strobe output
33	X0	—	G	Clock (oscillation) input
34	X1	—	G	Clock (oscillation) output

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Pin no.	Pin name	I/O	I/O circuit type*	Function
36 to 43 46 to 53	D16 to D31	I/O	H	External data bus signal
54 to 56 59 to 72 75 to 81	A00 to A23	O	H	External address bus signal
82	$\overline{\text{NMI}}$	I	H	NMI (Non Maskable Interrupt) input
83	P16_7	I/O	H	General-purpose input/output port
	$\overline{\text{ATG}}$			A/D converter external trigger input
84 to 87	P17_4 to P17_7	I/O	H	General-purpose input/output ports
	PPG4 to PPG7			PPG timer output pins
90 to 93	ICD0 to ICD3	I/O	H	Data input/output pins for development tool
94 to 96	ICS0 to ICS2	O	H	Status output pins for development tool
97	ICLK	O	I	Clock output pin for development tool
98	BREAK	I	H	Break input pin for development tool
99	$\overline{\text{WDRESET}}$	O	J	Watchdog reset output pin
100 to 107	P29_0 to P29_7	I/O	F	General-purpose input/output ports
	AN0 to AN7			Analog input pins for A/D converter
108 to 112	P28_0 to P28_4	I/O	F	General-purpose input/output ports
	AN8 to AN12			Analog input pins for A/D converter
116, 117	P24_0, P24_1	I/O	D	General-purpose input/output ports
	INT0, INT1			External interrupt input pins. Can be used as a return source from shutdown.
118	P22_4	I/O Open Drain	C	General-purpose input/output port
	SDA0			I^2C bus data input/output pin
	INT14			External interrupt input pin
119	P22_5	I/O Open Drain	C	General-purpose input/output port
	SCL0			I^2C bus clock input/output pin
120	P24_6	I/O	D	General-purpose input/output port
	INT6			External interrupt input pin. Can be used as a return source from shutdown.
121	P24_7	I/O	D	General-purpose input/output port
	INT7			External interrupt input pin. Can be used as a return source from shutdown.

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Pin no.	Pin name	I/O	I/O circuit type*	Function
122	P23_0	I/O	D	General-purpose input/output port
	RX0			RX input pin of CAN0
	INT8			External interrupt input pin. Can be used as a return source from shutdown.
123	P23_1	I/O	D	General-purpose input/output port
	TX0			TX output pin of CAN0
124	P23_2	I/O	D	General-purpose input/output port
	RX1			RX input pin of CAN1
	INT9			External interrupt input pin. Can be used as a return source from shutdown.
125	P23_3	I/O	D	General-purpose input/output port
	TX1			TX output pin of CAN1
126	MD3	I	A	Mode setting pins
127	MD2	I	A	
128	MD1	I	A	
129	MD0	I	B	
130	$\overline{\text{TRST}}$	I	E	Reset input pin for development tool
131	$\overline{\text{INIT}}$	I	B	External reset input
134	P21_0	I/O	D	General-purpose input/output port
	SIN0			Data input pin of UART0
135	P21_1	I/O	D	General-purpose input/output port
	SOT0			Data output pin of UART0
136	P21_2	I/O	D	General-purpose input/output port
	SCK0			Clock input/output pin of UART0
	FRCK0			External clock input pin of free-run timer0
137	P21_4	I/O	D	General-purpose input/output port
	SIN1			Data input pin of UART1
138	P21_5	I/O	D	General-purpose input/output port
	SOT1			Data output pin of UART1
139	P21_6	I/O	D	General-purpose input/output port
	SCK1			Clock input/output pin of UART1
	FRCK1			External clock input pin of free-run timer1
140	P20_0	I/O	D	General-purpose input/output port
	SIN2			Data input pin of UART2

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Pin no.	Pin name	I/O	I/O circuit type*	Function
141	P20_1	I/O	D	General-purpose input/output port
	SOT2			Data output pin of UART2
142	P20_2	I/O	D	General-purpose input/output port
	SCK2			Clock input/output pin of UART2
	FRCK2			External clock input pin of free-run timer2
143	P20_4	I/O	D	General-purpose input/output port
	SIN3			Data input pin of UART3
144	P20_5	I/O	D	General-purpose input/output port
	SOT3			Data output pin of UART3
145	P20_6	I/O	D	General-purpose input/output port
	SCK3			Clock input/output pin of UART3
	FRCK3			External clock input pin of free-run timer3
148	P19_0	I/O	D	General-purpose input/output port
	SIN4			Data input pin of UART4
149	P19_1	I/O	D	General-purpose input/output port
	SOT4			Data output pin of UART4
150	P19_2	I/O	D	General-purpose input/output port
	SCK4			Clock input/output pin of UART4
151	P19_4	I/O	D	General-purpose input/output port
	SIN5			Data input pin of UART5
152	P19_5	I/O	D	General-purpose input/output port
	SOT5			Data output pin of UART5
153	P19_6	I/O	D	General-purpose input/output port
	SCK5			Clock input/output pin of UART5
154	P18_0	I/O	D	General-purpose input/output port
	SIN6			Data input pin of UART6
155	P18_1	I/O	D	General-purpose input/output port
	SOT6			Data output pin of UART6
156	P18_2	I/O	D	General-purpose input/output port
	SCK6			Clock input/output pin of UART6
157 to 160	P15_0 to P15_3	I/O	D	General-purpose input/output ports
	OCU0 to OCU3			Output compare output pins
	TOT0 to TOT3			Reload timer output pins
163	P23_4	I/O	D	General-purpose input/output port
	INT10			External interrupt input pin

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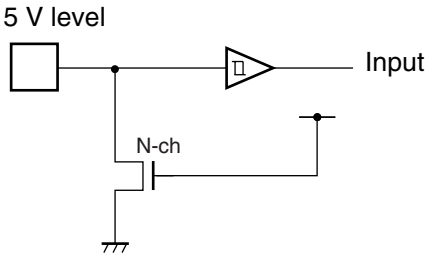
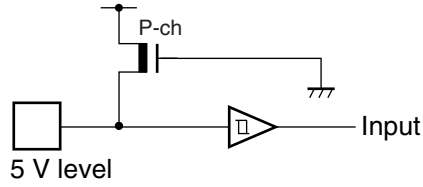
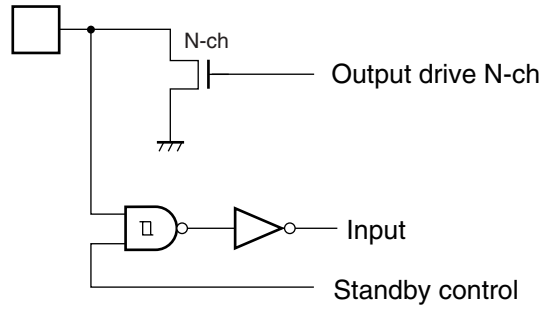
Pin no.	Pin name	I/O	I/O circuit type*	Function
164	P23_6	I/O	D	General-purpose input/output port
	INT11			External interrupt input pin
165	P22_0	I/O	D	General-purpose input/output port
	INT12			External interrupt input pin
166	P22_2	I/O	D	General-purpose input/output port
	INT13			External interrupt input pin
167	P22_3	I/O	D	General-purpose input/output port
168 to 171	P14_0 to P14_3	I/O	D	General-purpose input/output ports
	ICU0 to ICU3			Input capture input pins
	TIN0 to TIN3			External trigger input pins of reload timer
	TRG0 to TRG3			External trigger input pins of PPG
172 to 175	P17_0 to P17_3	I/O	D	General-purpose input/output ports
	PPG0 to PPG3			PPG timer output pins

*: For details of I/O circuit types, refer to “■ I/O CIRCUIT TYPE”.

[Power supply/GND pins]

Pin number	Pin name	I/O	Function
1, 13, 32, 35, 45, 58, 74, 88, 132, 146, 161	VSS	(VSS)	GND pins
11, 12, 30, 44, 57, 73, 89	VCC3	(VCC3)	3.3 V power supply pins
133, 147	VCC5	(VCC5)	5 V power supply pins. These pins are I/O power supplies corresponding to 116 to 145 pins. The corresponding I/O pin operates at 3.3 V when supplying 3.3 V, and at 5 V when supplying 5V. Be sure to supply 5 V if more than one 5V operating pin is specified, or 5V is supplied at pin 162 or pin 176.
162	VCC5	(VCC5)	5 V power supply pin. This pin is an I/O power supply corresponding to 148 to 160 pins. The corresponding I/O pin operates at 3.3 V when supplying 3.3 V, and at 5V when supplying 5 V. Be sure to supply 5 V if more than one 5 V operating pin is specified.
176	VCC5	(VCC5)	5 V power supply pin. This pin is an I/O power supply corresponding to 2 to 7 pins. The corresponding I/O pin operates at 3.3 V when supplying 3.3 V, and at 5 V when supplying 5 V. Be sure to supply 5 V if more than one 5 V operating pin is specified.
113	AVSS/AVRL	(AVSS)	Analog GND pin for A/D converter
114	AVCC3	(AVCC3)	3.3 V power supply pin for A/D converter
115	AVRH	(AVRH)	Reference power supply pin for A/D converter
14	C_1	—	Capacitor connection pin for internal regulator. Connect a 4.8 μF capacitor.
31	C_2	—	Capacitor connection pin for internal regulator. Connect a 4.8 μF capacitor.

■ I/O CIRCUIT TYPE

Type	Circuit type	Remarks
A		5 V CMOS hysteresis input
B		5 V CMOS hysteresis input
C		Input/output pin for I²C I_{OL} = 3 mA With stand voltage of 5 V With standby control

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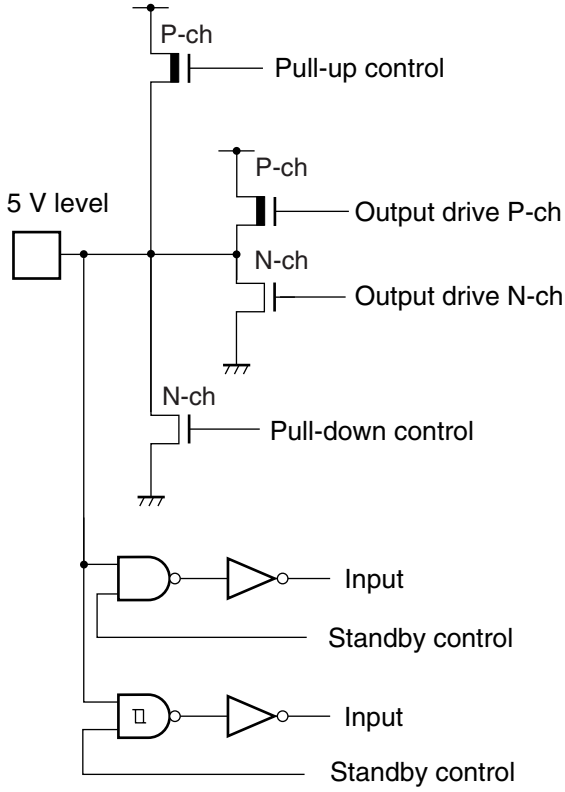
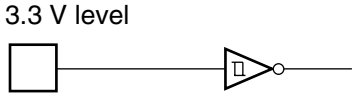
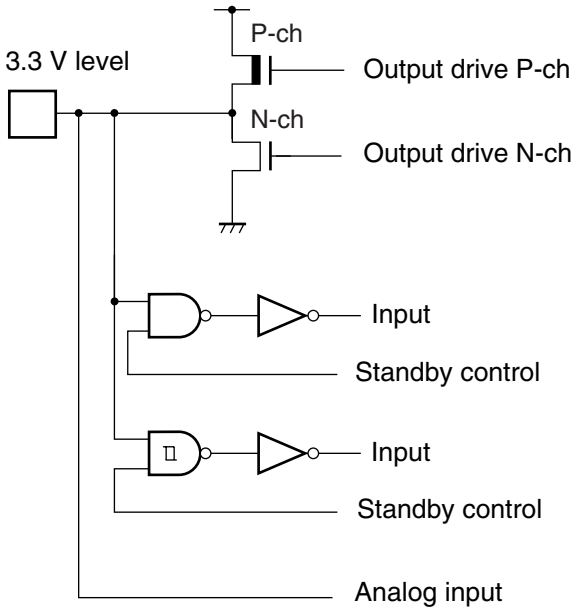
Type	Circuit type	Remarks
D		5 V CMOS output I_{OL} = 4 mA 5 V CMOS input 5 V CMOS hysteresis input With 50 kΩ pull-up/pull-down control With standby control
E		3.3 V CMOS hysteresis input With stand voltage of 5 V With standby control
F		3.3 V CMOS output I_{OL} = 4 mA 3.3 V CMOS input 3.3 V CMOS hysteresis input Analog input With standby control

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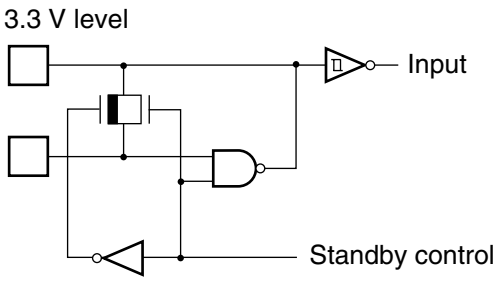
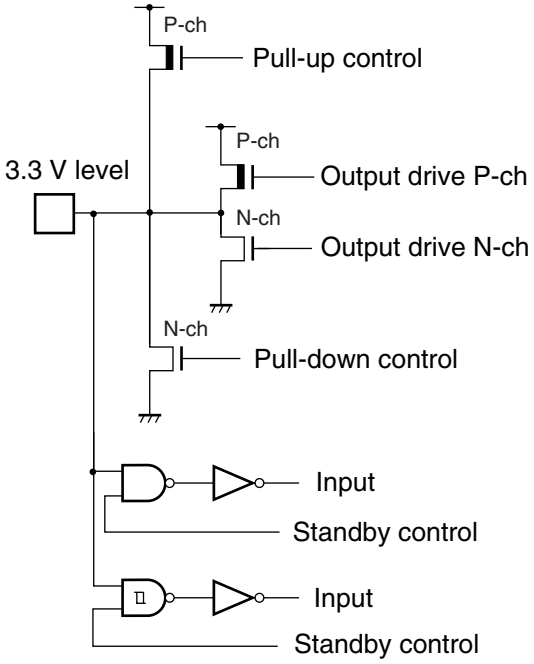
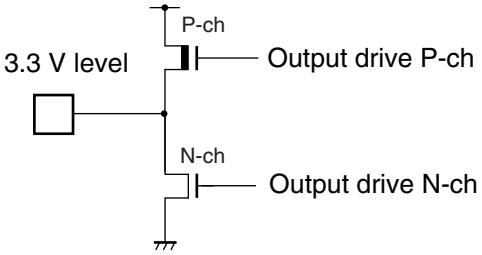
Type	Circuit type	Remarks
G		3.3 V oscillation cell
H		3.3 V CMOS output I_{OL} = 4 mA 3.3 V CMOS input 3.3 V CMOS hysteresis input With 33 kΩ pull-up/pull-down control With standby control
I, J		3.3 V CMOS output I : I_{OL} = 8 mA J : I_{OL} = 4 mA

■ HANDLING DEVICES

• Preventing Latch-up

Latch-up may occur in a CMOS IC if a voltage higher than V_{CC} or less than V_{SS} is applied to an input or output pin or if a voltage exceeding the rating is applied between VCC pin and VSS pin. If latch-up occurs, the power supply current increases rapidly, sometimes resulting in thermal breakdown of the device. Therefore, when using a CMOS IC, do not exceed the maximum rating.

• Handling of unused input pins

If unused input pins are left open, abnormal operation may result. Any unused input pins should be connected to pull-up or pull-down resistor.

• Power supply pins

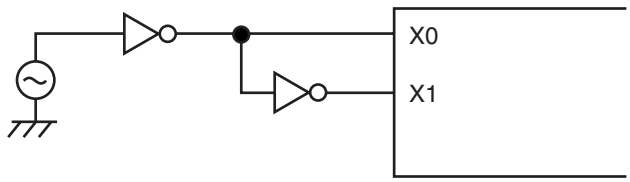
When provided with multiple VCC pins or VSS pins, the device is designed such that the pins having equal potential are interconnected internally to prevent malfunctions such as latch-up. All of these pins must however be connected to the power supply and ground externally to reduce unwanted radiation, to prevent the strobe signal from malfunctioning due to a rise of ground level, and to follow the total output current standards. In addition, VCC pin and VSS pin of this device should be connected from the power supply source with the lowest possible impedance.
It is also recommended to connect a ceramic capacitor of approximately 0.1 μF as a bypass capacitor between VCC pin and VSS pin near this device.
This series has a built-in step-down regulator. Connect a bypass capacitor of 4.7 μF to C_1 and C_2 pins for the regulator.

• Crystal oscillator circuit

Noise in proximity to the X0 and X1 pins can cause abnormal operation in this device. Printed circuit boards should be designed so that the X0 and X1 pins, and crystal oscillator, as well as bypass capacitors connected to ground, are placed as close together as possible.
The use of printed circuit board architecture in which the X0 and X1 pins are surrounded by ground contributes to stable operation and is strongly recommended.
Please ask the crystal maker to evaluate the oscillational characteristics of the crystal and this device.

• Notes on using external clock

In principle, when using external clock, supply a clock to the X0 pin and X1 pin simultaneously. Also, an opposite phase clock to the X0 pin must be supplied to the X1 pin. However, in this case the stop mode (oscillation stop mode) must not be used (This is because the X1 pin stops at ”H” output in STOP mode).



(Note) Stop mode (oscillation stop mode) cannot be used.

Example of using external clock (normal)

- Mode pins (MD0 to MD3)

  When using mode pins, connect them directly to VCC pin or VSS pin. To prevent the device from entering test mode accidentally due to noise, minimize the lengths of the patterns between each mode pin and VCC pin or VSS pin on the printed circuit board as possible and connect them with low impedance.

- Power-on sequences for 3.3 V and 5 V
  - Immediately after power-on, keep “L” level input to the $\overline{\text{INIT}}$ pin for the oscillation stabilization wait time (8 ms) to ensure the oscillation stabilization wait time for the oscillator circuit.
  - There is no power-on sequences.
  - When executing a reset cancellation (changing $\overline{\text{INIT}}$ pin from “L” level to “H” level), be sure to execute it while 3 V and 5 V power supplies are stable.

- Caution on operations during PLL clock mode

  On this microcontroller, if in case the crystal oscillator breaks off or an external reference clock input stops while the PLL clock mode is selected, a self-oscillator circuit contained in the PLL may continue its operation at its self-running frequency. However, Fujitsu will not guarantee results of operations if such failure occurs.

- External bus setting

  This model guarantees the maximum frequency of 40 MHz for the external bus clock SYSCLK.

  Setting the base clock frequency to 80 MHz without changing the initial value of DIVR1 (external bus base clock division setting register) sets the external bus frequency also to 80 MHz. Before changing the base clock frequency, set SYSCLK not exceeding 40 MHz.

- Pull-up control

  Connecting a pull-up resistor to the pin serving as an external bus pin cannot guarantee the AC standard.

- Notes on PS register

  Since some instructions process the PS register in advance, the following exceptional operations may cause a break in the interrupt process routine or an update of display contents of the flag in the PS register when the debugger is being used. In either case, as the device is designed to carry out reprocessing correctly upon returning from such an EIT event, it performs operations before and after the EIT as specified.

  1) The following operations may be performed when the instruction immediately followed by a DIV0U/DIV0S instruction accepts a user interrupt/NMI, executes a step, or breaks in response to a data event or emulator menu.

     -D0 and D1 flags are updated in advance.

     -An EIT process routine (user interrupt/NMI or emulator) is executed.

     -Upon returning from the EIT, the DIV0U/DIV0S instruction is executed and the D0 and D1 flags are updated to the same values as those in 1).

  2) The following operations are performed when each instruction of OR CCR, ST ILM, MOV Ri and PS is executed to enable interrupts while a user interrupt/NMI source has been occurring.

     -The PS register is updated in advance.

     -An EIT process routine (user interrupt/NMI or emulator) is executed.

     -Upon returning from the EIT, the above instructions are executed and the PS register is updated to the same value as that in 1).

■ NOTES ON DEBUGGER

• Step execution of RETI instruction

In the environment where interrupts occur frequently when stepping, only the corresponding interrupt process routines are executed repeatedly. As the result of that, the main routine and low-interrupt-level programs are not executed (For example, if an interrupt to the time base timer is enabled, a break always occurs at the beginning of the time base routine when stepping RETI) .

Disable the corresponding interrupts when the debug on the corresponding interrupt process routines becomes unnecessary.

• Break function

If the target address of a hardware break (including an event break) is set to the address currently contained in the system stack pointer or in the area containing the stack pointer, the user program causes a break after execution of one instruction even though there is no actual data access instruction in the user program.

To prevent this, do not set (word) access to the area containing the address of the system stack pointer as the target of a hardware break (including an event break).

• Operand break

If a stack pointer exists in the area which is set as the DSU operand break, malfunctions may occur. Do not set the access to the areas containing the address of system stack pointer as a target of data event break.

■ DSU4 (ICE) DEDICATED CONNECTION PINS

MB91461 DSU4 (ICE) dedicated connection pins

Pin no.	Pin name	Function
93 to 90	ICD3 to ICD0	Data input/output pins for development tool
96 to 94	ICS2 to ICS0	Status output pins for development tool
97	ICLK	Clock pin for development tool
98	BREAK	Break pin for development tool
130	$\overline{\text{TRST}}$	Reset pin for development tool (3 V/5 V supported input pin)

- User target side connector and the MB91461 connection

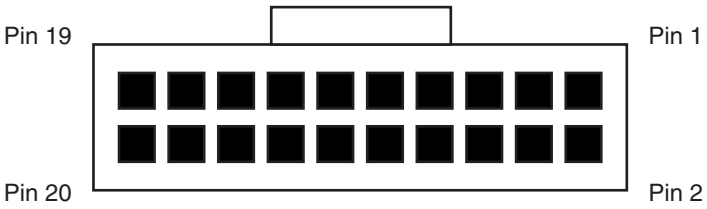
  The recommended connector for the user target side is shown below.

  Manufacturer : YAMAICHI ELECTRONICS CO., LTD.

  Model number : FAP-20-08#*

  Note : The asterisk (*) in the model number represents each of the following pin shapes:

  - 1 : Right angle/wrapping
  - 2 : Right angle/solder dip
  - 4 : Straight/solder dip



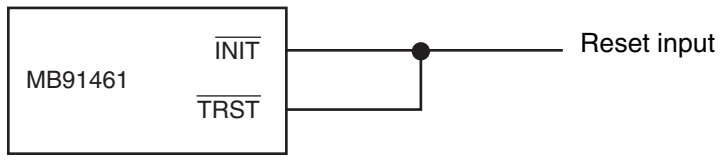
Connector pin no.	Signal line name	I/O	Pin handling	
1	EVCC2	I	Open	
2	EVCC3	I	Open	
3	DSUIO	I/O	Open	
4	UVCC	O	User V_{CC} output	
6	XRSTIN	O	Connected to user circuit $\overline{INIT}$ signal	
8	PLVL	I	Open	
5	XTRST	I	MB91461	Connected to $\overline{TRST}$ (130 pin)
7	XINIT	I		Connected to $\overline{INIT}$ (131 pin)
9	GND	—		Connected to VSS
10	BREAK	I		Connected to BREAK (98 pin)
11	ICD3	I/O		Connected to ICD3 (93 pin)
12	ICD2			Connected to ICD2 (92 pin)
13	ICD1			Connected to ICD1 (91 pin)
14	ICD0			Connected to ICD0 (90 pin)
15	GND	—		Connected to VSS
16	ICS2	O		Connected to ICS2 (96 pin)
17	ICS1			Connected to ICS1 (95 pin)
18	ICS0			Connected to ICS0 (94 pin)
19	GND	—		Connected to VSS
20	ICLK	O		Connected to ICLK (97 pin)

Handling of dedicated pin for DSU4 (ICE) in mass production

Handling of dedicated pin for DSU4 (ICE) in mass production

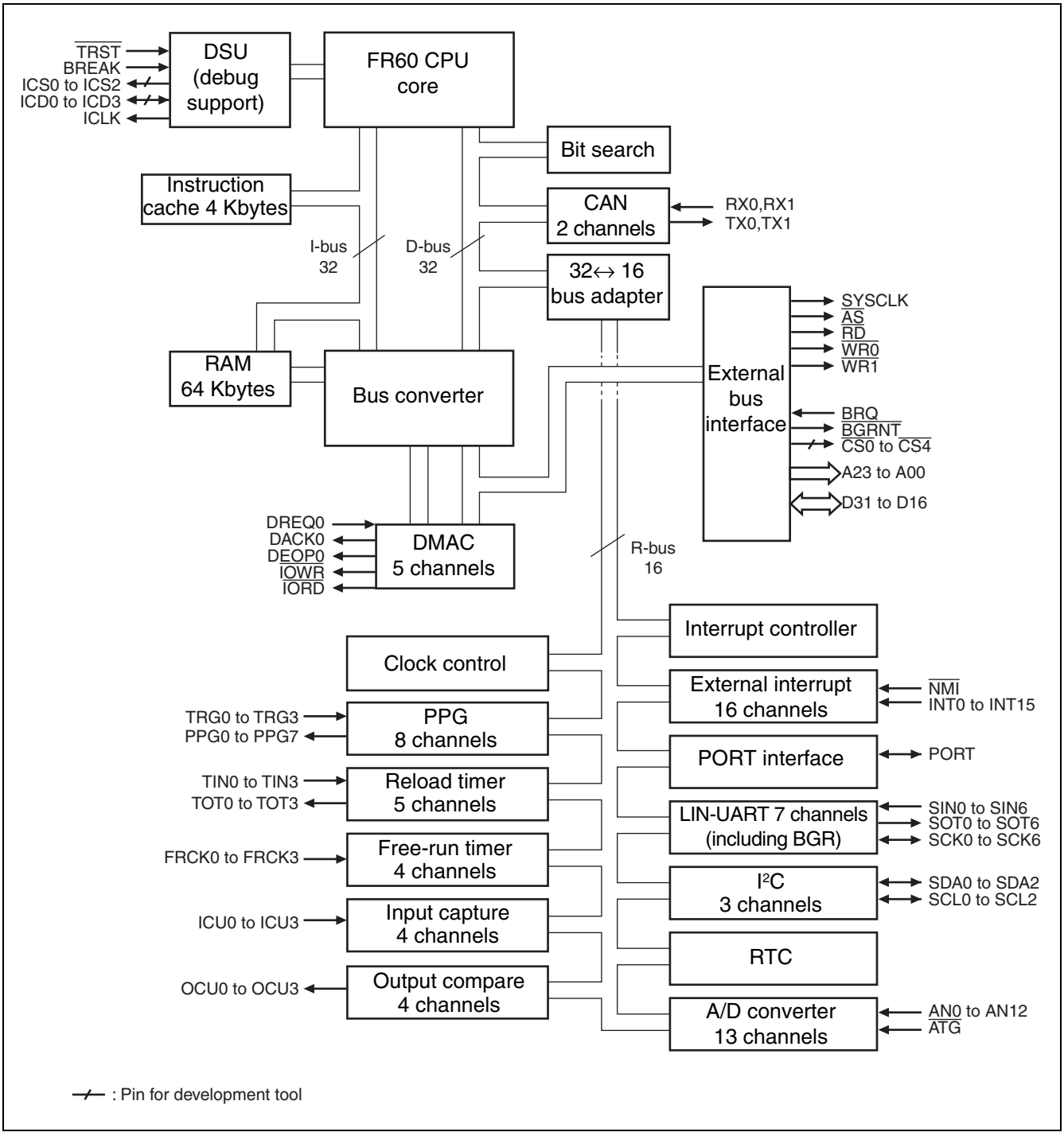
MB91461 pin no.	Pin name	Pin handling
93 to 90	ICD3 to ICD0	Open
96 to 94	ICS2 to ICS0	Open
97	ICLK	Open
98	BREAK	Open
130	$\overline{\text{TRST}}$	Connected to $\overline{\text{INIT}}$ (131 pin: external reset input pin)

Connection handling of the reset pin ($\overline{\text{TRST}}$) for development tool (DSU) in mass production



Since the reset pin ($\overline{\text{TRST}}$) for development tool is the input pin supporting 3V/5V, it can be connected to $\overline{\text{INIT}}$ pin directly.

■ BLOCK DIAGRAM



■ CPU AND CONTROL UNIT

The FR family CPU is a high performance core that is designed based on the RISC architecture with advanced instructions for embedded applications.

1. Features

- Adoption of RISC architecture
  Basic instruction: 1 instruction per cycle
- General-purpose registers: 32-bit × 16 registers
- 4 Gbytes linear memory space
- Multiplier installed
  32-bit × 32-bit multiplication: 5 cycles
  16-bit × 16-bit multiplication: 3 cycles
- Enhanced interrupt processing function
  Quick response speed (6 cycles)
  Multiple-interrupt support
  Level mask function (16 levels)
- Enhanced instructions for I/O operation
  Memory-to-memory transfer instruction
  Bit processing instruction
- Basic instruction word length: 16 bits
- Low-power consumption
  Sleep mode/stop mode/shutdown mode

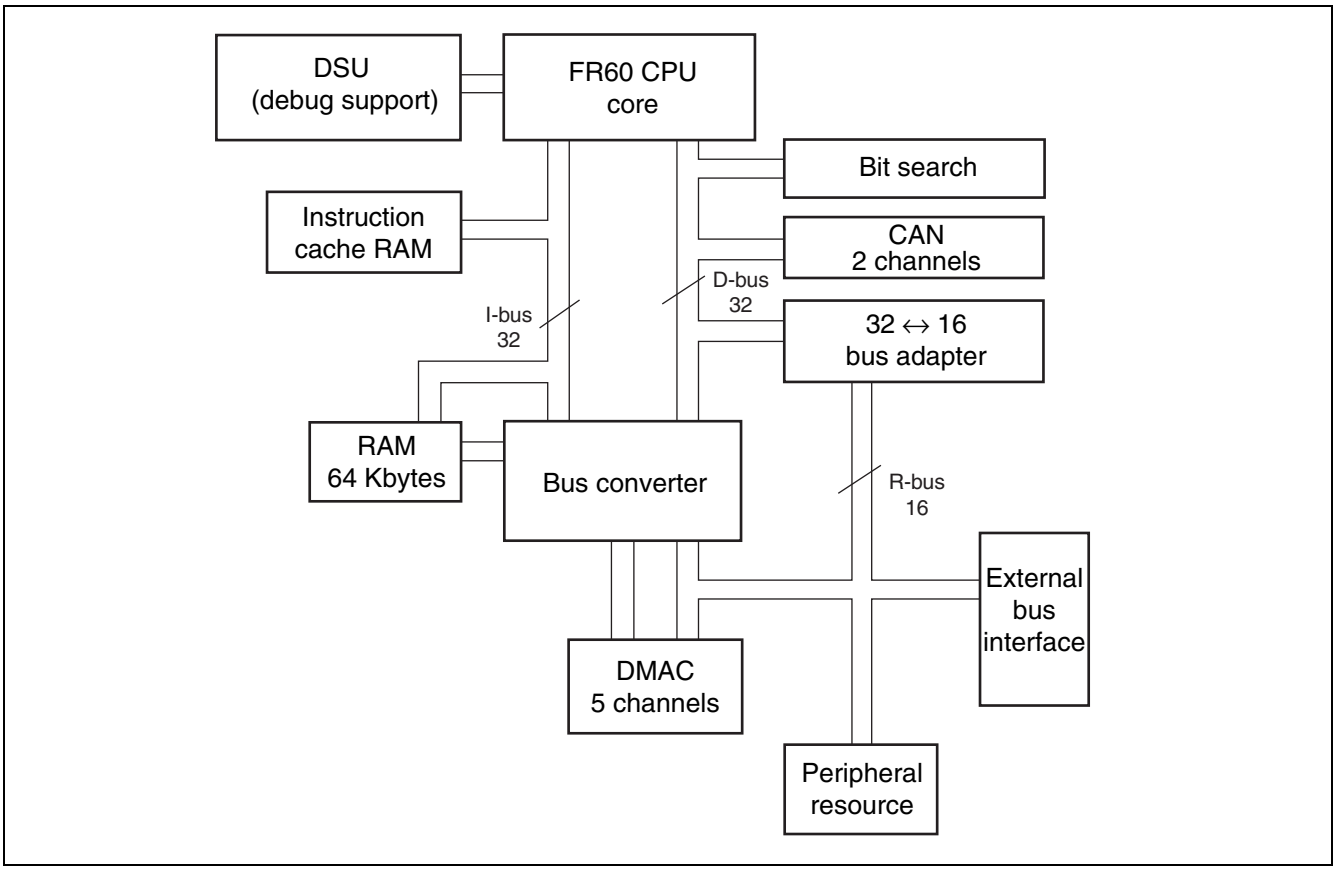
2. Internal architecture

The FR family CPU uses the Harvard architecture in which the instruction bus and data bus are independent of each other.

A 32-bit ↔ 16-bit bus adapter is connected to the 32-bit bus (D-bus) to provide an interface between the CPU and peripheral resources.

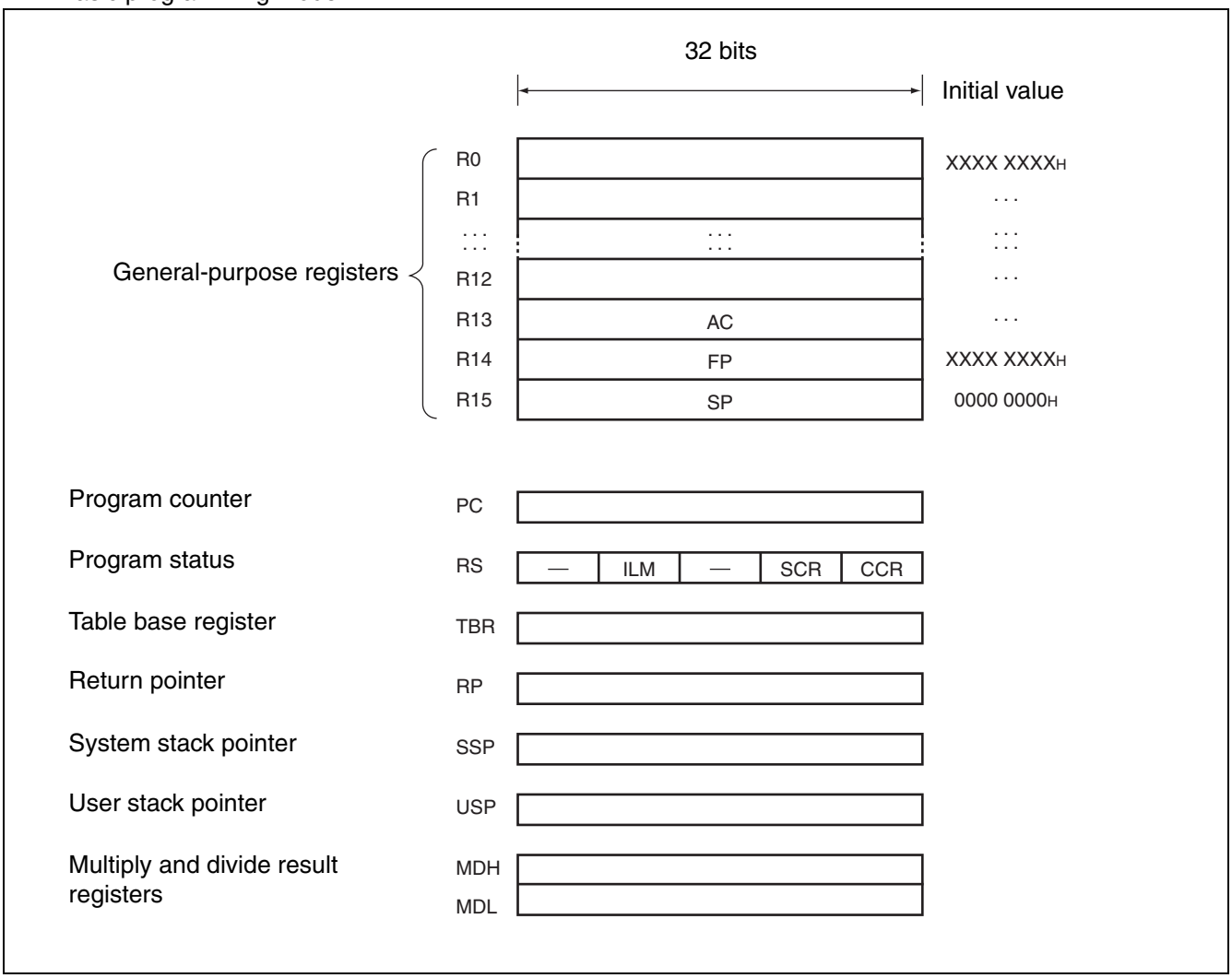
A Harvard ↔ Princeton bus converter is connected to both the I-bus and D-bus to provide an interface between the CPU and the bus controller.

The following figure shows the internal architecture structure.



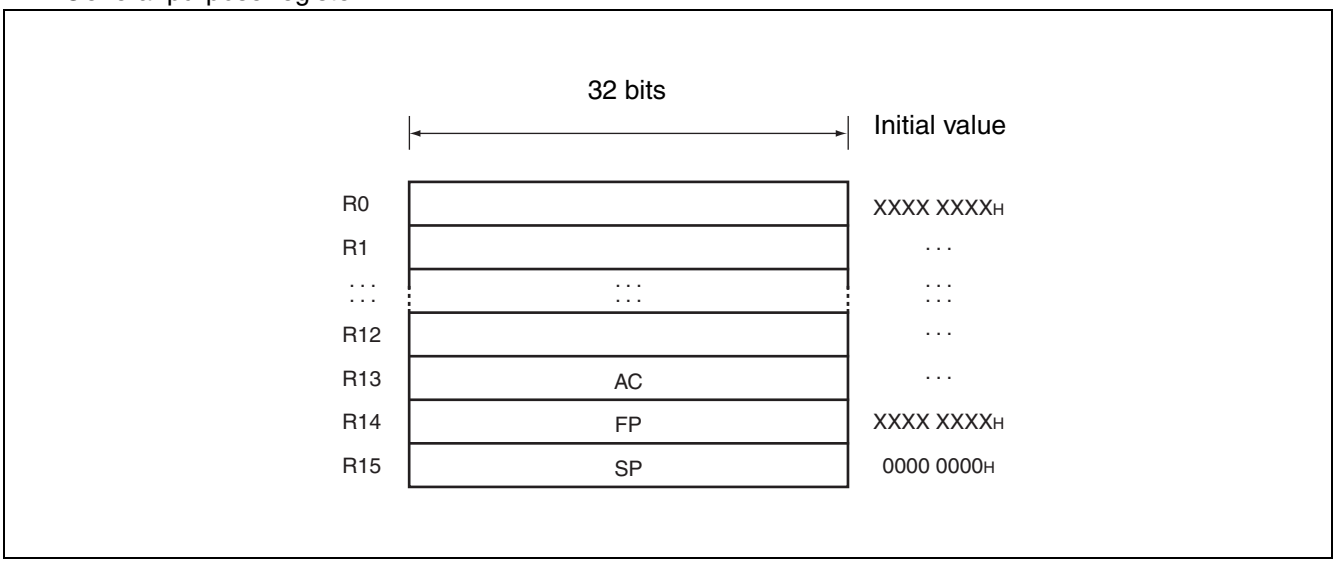
3. Programming model

- Basic programming model



4. Registers

• General-purpose register



Registers R0 to R15 are general-purpose registers. These registers can be used as accumulators for computation operations and as pointers for memory access.

Of the 16 registers, enhanced commands are provided for the following registers to enable their use for particular applications.

R13 : Virtual accumulator

R14 : Frame pointer

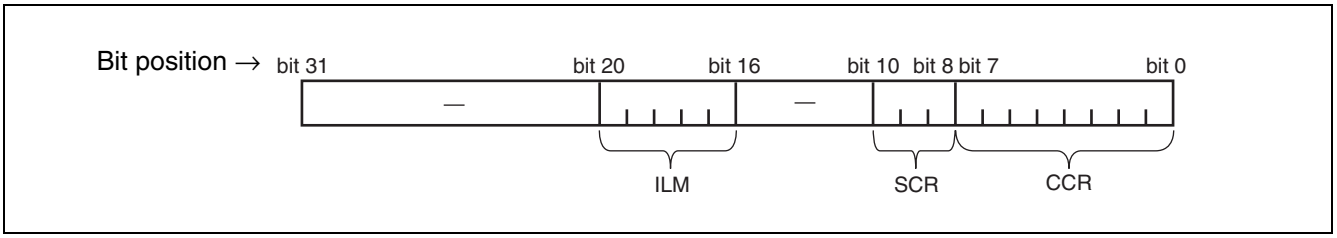
R15 : Stack pointer

Initial values at reset are undefined for R0 to R14. The value for R15 is 00000000H (SSP value).

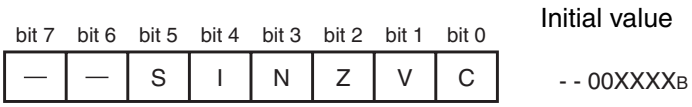
• PS (Program Status)

This register holds the program status, and is divided into three parts, ILM, SCR, and CCR.

All undefined bits (-) in the diagram are reserved bits. The read values are always “0”. Write access to these bits is invalid.



• CCR (Condition Code Register)



S : Stack flag

I : Interrupt enable flag

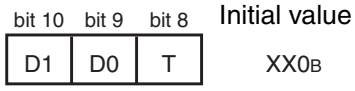
N : Negative enable flag

Z : Zero flag

V : Overflow flag

C : Carry flag

• SCR (System Condition Register)



Flag for step multiplication (D1, D0)

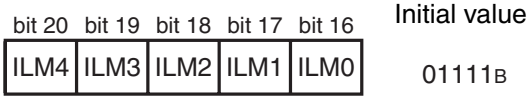
This flag stores interim data during execution of step multiplication.

Step trace trap flag (T)

This flag indicates whether the step trace trap is enabled or disabled.

The step trace trap function is used by emulators. When an emulator is in use, it cannot be used in execution of user programs.

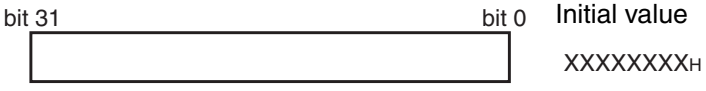
• ILM



This register stores interrupt level mask values, and the values stored in ILM4 to ILM0 are used for level masking.

The register is initialized to value “01111_B” at reset.

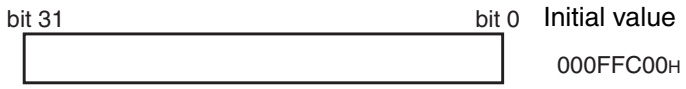
• PC (Program Counter)



The program counter indicates the address of the instruction that is being executed.

The initial value at reset is undefined.

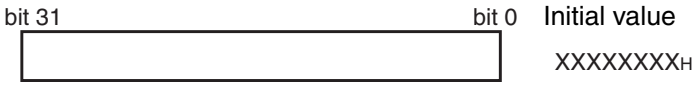
• TBR (Table Base Register)



The table base register stores the starting address of the vector table used in EIT processing.

The initial value at reset is 000FFC00H.

• RP (Return Pointer)



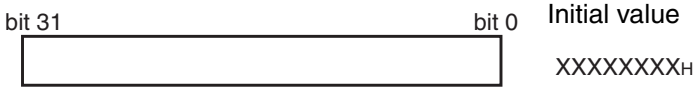
The return pointer stores the address for return from subroutines.

During execution of a CALL instruction, the PC value is transferred to this RP register.

During execution of a RET instruction, the contents of the RP register are transferred to PC.

The initial value at reset is undefined.

• USP (User Stack Pointer)

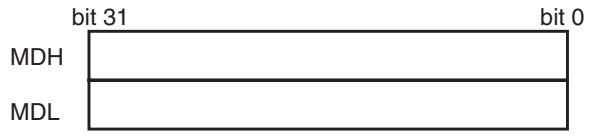


The user stack pointer, when the S flag is “1”, this register functions as the R15 register.

- The USP register can also be explicitly specified.

  The initial value at reset is undefined.
- This register cannot be used with RETI instructions.

• Multiply & divide registers



These registers are for multiplication and division, and are each 32 bits in length.

The initial value at reset is undefined.

■ MODE SETTING

In the FR family, the mode pins (MD2, MD1, MD0) and the mode register (MODR) are used to set the operating mode.

1. Mode pins

The three pins MD2, MD1, MD0 are used to specify the mode vector fetch related settings.

Settings other than shown in the table are not allowed.

Mode pins*			Mode name	Reset vector access area	Remarks
MD2	MD1	MD0			
0	0	0	Internal ROM mode vector	Internal	Not allowed
0	0	1	External ROM mode vector	External	Bus width is set by mode register.

* : Always use MD3 with “0”.

Note : The FR family does not support the external mode vector fetch using multiplex bus.

2. Mode register (MODR)

The data written to the mode register using mode vector fetch is called mode data.

After the mode register (MODR) is set, the device operates according to the operation mode set in this register.

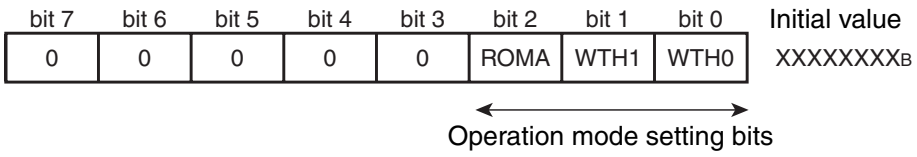
The mode register is set by all reset sources. User programs cannot write data to the mode register.

Rewriting is allowed in the emulator mode. In this case, use an 8-bit length data transfer instruction.

A 16/32-bit length transfer instruction cannot be used for writing.

Description of the mode register is given below.

[Mode register description]



[bit7 to bit3] Reserved bits

Be sure to set these bits to “00000_B”.

Operation is not guaranteed when any value other than “00000_B” is set.

[bit2] ROMA (Internal enable bit)

The ROMA bit is used to set whether to enable the internal F-bus RAM and F-bus ROM areas.

ROMA	Function	Remarks
0	External ROM mode	Internal F-bus RAM becomes valid. The internal ROM area (40000_H to $FFFFF_H$) is used as an external area.
1	Internal ROM mode	Internal F-bus RAM and F-bus ROM become valid.

Note : Use ”0” in MB91461.

[bit1, bit0] WTH1, WTH0 (Bus width setting bits)

These bits are used to set the bus width to be used in the external bus mode.

When the operation mode is the external bus mode, these values are set in bits BW1 and BW0 in AMD0 (CS0 area).

WTH1	WTH0	Function	Remarks
0	0	8-bit bus width	External bus mode
0	1	16-bit bus width	External bus mode
1	0	—	Setting disabled
1	1	Single chip mode	Setting disabled

■ MEMORY SPACE

1. Memory space

The FR family has 4 Gbytes of logical address space (2^{32} addresses) available to the CPU by linear access.

- Direct addressing area

The following address space area is used for I/O.

This area is called direct addressing area, and the address of an operand can be specified directly in an instruction.

The size of directly addressable area depends on the length of the data being accessed as shown below.

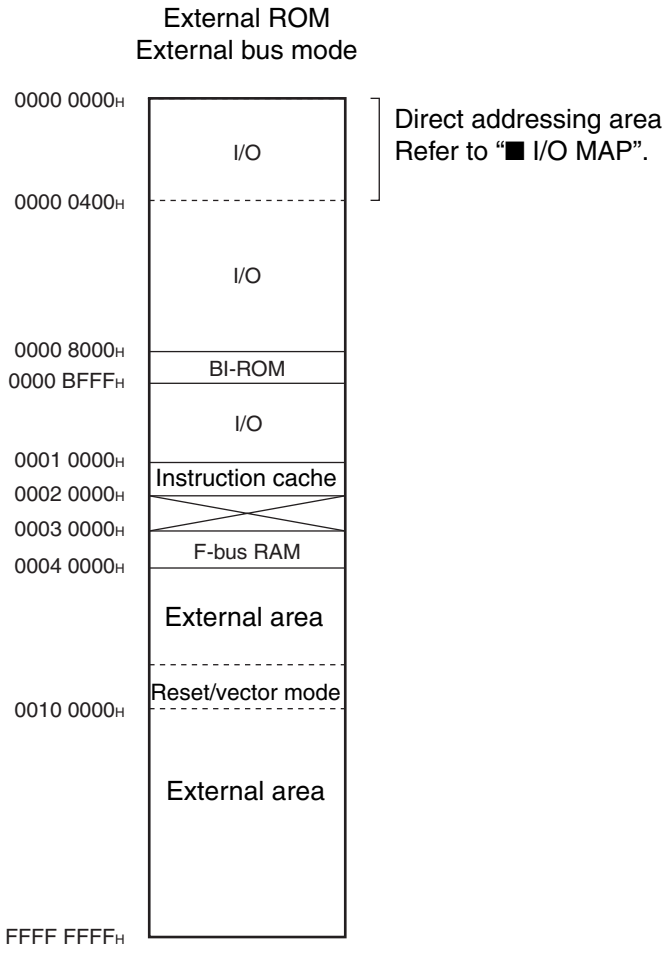
Byte data access : 000_H to $0FF_H$

Half word access : 000_H to $1FF_H$

Word data access : 000_H to $3FF_H$

2. Memory map

MB91461

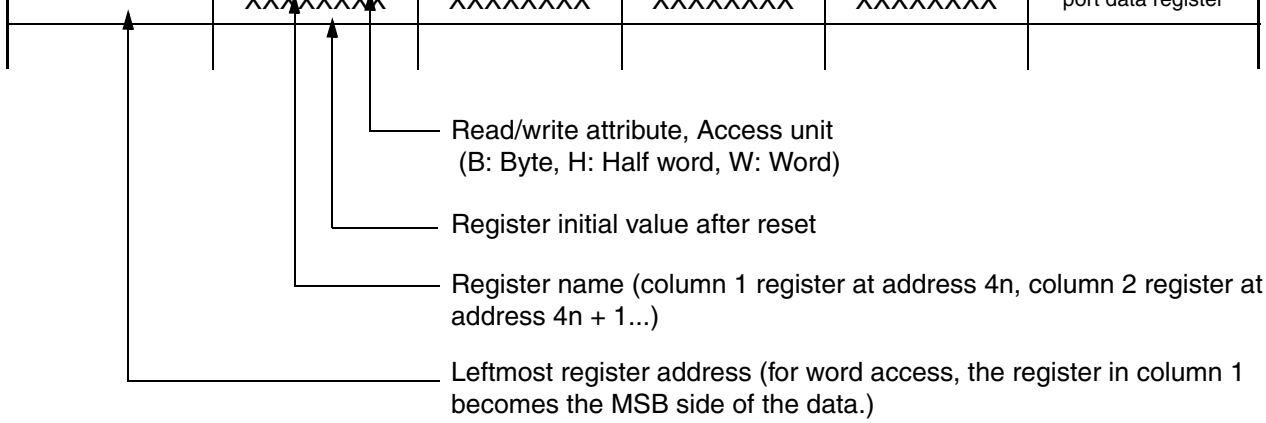


: Access prohibited

Each mode is set depending on the mode vector fetch after $\overline{INIT}$ is negated. (For details on mode settings, refer to "■ MODE SETTING".)

■ I/O MAP

Address	Register				Block
	+ **0**	+ **1**	+ **2**	+ **3**	
000000H	PDR0 [R/W]B XXXXXXXX	PDR1 [R/W]B XXXXXXXX	PDR2 [R/W]B XXXXXXXX	PDR3 [R/W]B XXXXXXXX	T-unit port data register



Note : Initial values of register bits are represented as follows:

" 1 " : Initial value " 1 "
" 0 " : Initial value " 0 "
" X " : Initial value " undefined "
" - " : No physical register at this location
Access is barred with an undefined data access attribute.

Address	Register				Block
	0	1	2	3	
000000H	Reserved				R-bus port data register
000004H	Reserved				
000008H	Reserved				
00000CH	Reserved		PDR14 [R/W] B,H ----XXXX	PDR15 [R/W] B,H ----XXXX	
000010H	PDR16 [R/W] B,H X-------	PDR17 [R/W] B,H XXXXXXXX	PDR18 [R/W] B,H -----XXX	PDR19 [R/W] B,H -XXX-XXX	
000014H	PDR20 [R/W] B,H -XXX-XXX	PDR21 [R/W] B,H -XXX-XXX	PDR22 [R/W] B,H XXXXXX-X	PDR23 [R/W] B,H -X-XXXXX	
000018H	PDR24 [R/W] B,H XXXXXXXX	Reserved			
00001CH	PDR28 [R/W] B,H ---XXXXX	PDR29 [R/W] B,H XXXXXXXX	Reserved		
000020H	Reserved				
000024H to 00002CH	Reserved				Reserved
000030H	EIRR0 [R/W] B 00000000	ENIR0 [R/W] B 00000000	ELVR0 [R/W] B,H 00000000 00000000		External interrupt (INT0 to INT7) NMI
000034H	EIRR1 [R/W] B 00000000	ENIR1 [R/W] B 00000000	ELVR1 [R/W] B,H 00000000 00000000		External interrupt (INT 8 to INT15)
000038H	DICR [R/W] B -------0	HRCL [R/W] B 0--11111	Reserved		Delay interrupt
00003CH	Reserved				Reserved
000040H	SCR00 [R/W,W] B,H,W 00000000	SMR00 [R/W,W] B,H,W 00000000	SSR00 [R/W,R] B,H,W 00001000	RDR00/TDR00 [R/W] B,H,W 00000000	UART (LIN) 0
000044H	ESCR00 [R/W] B,H 00000X00	ECCR00 [R/W,R,W] B,H -00000XX	Reserved		
000048H	SCR01 [R/W,W] B,H,W 00000000	SMR01 [R/W,W] B,H,W 00000000	SSR01 [R/W,R] B,H,W 00001000	RDR01/TDR01 [R/W] B,H,W 00000000	LIN-UART 1
00004CH	ESCR01 [R/W] B,H 00000X00	ECCR01 [R/W,R,W] B,H -00000XX	Reserved		

(Continued)

Address	Register				Block
	0	1	2	3	
000050H	SCR02 [R/W,W] B,H,W 00000000	SMR02 [R/W,W] B,H,W 00000000	SSR02 [R/W,R] B,H,W 00001000	RDR02/TDR02 [R/W] B,H,W 00000000	LIN-UART 2
000054H	ESCR02 [R/W]B,H 00000X00	ECCR02 [R/W,R,W] B,H -00000XX	Reserved		
000058H	SCR03 [R/W,W] B,H,W 00000000	SMR03 [R/W,W] B,H,W 00000000	SSR03 [R/W,R] B,H,W 00001000	RDR03/TDR03 [R/W] B,H,W 00000000	LIN-UART 3
00005CH	ESCR03 [R/W] B,H 00000X00	ECCR03 [R/W,R,W] B,H -00000XX	Reserved		
000060H	SCR04 [R/W,W] B,H,W 00000000	SMR04 [R/W,W] B,H,W 00000000	SSR04 [R/W,R] B,H,W 00001000	RDR04/TDR04 [R/W] B,H,W 00000000	LIN-UART 4
000064H	ESCR04 [R/W] B,H,W 00000X00	ECCR04 [R/W,R,W] B,H,W -00000XX	FSR04 [R] B,H,W ---00000	FCR04 [R/W] B,H,W 0001-000	
000068H	SCR05 [R/W,W] B,H,W 00000000	SMR05 [R/W,W] B,H,W 00000000	SSR05 [R/W,R] B,H,W 00001000	RDR05/TDR05 [R/W] B,H,W 00000000	LIN-UART 5
00006CH	ESCR05 [R/W] B,H,W 00000X00	ECCR05 [R/W,R,W] B,H,W -00000XX	FSR05 [R] B,H,W ---00000	FCR05 [R/W] B,H,W 0001-000	
000070H	SCR06 [R/W,W] B,H,W 00000000	SMR06 [R/W,W] B,H,W 00000000	SSR06 [R/W,R] B,H,W 00001000	RDR06/TDR06 [R/W] B,H,W 00000000	LIN-UART 6
000074H	ESCR06 [R/W] B,H,W 00000X00	ECCR06 [R/W,R,W] B,H,W -00000XX	FSR06 [R] B,H,W ---00000	FCR06 [R/W] B,H,W 0001-000	
000078H to 00007CH	Reserved				Reserved
000080H	BGR100 [R/W] B,H,W 00000000	BGR000 [R/W] B,H,W 00000000	BGR101 [R/W] B,H,W 00000000	BGR001 [R/W] B,H,W 00000000	Baud rate generator UART (LIN) 0 to 6
000084H	BGR102 [R/W] B,H,W 00000000	BGR002 [R/W] B,H,W 00000000	BGR103 [R/W] B,H,W 00000000	BGR003 [R/W] B,H,W 00000000	
000088H	BGR104 [R/W] B,H,W 00000000	BGR004 [R/W] B,H,W 00000000	BGR105 [R/W] B,H,W 00000000	BGR005 [R/W] B,H,W 00000000	

(Continued)

Address	Register				Block
	0	1	2	3	
00008C$_H$	BGR106 [R/W] B,H,W 00000000	BGR006 [R/W] B,H,W 00000000	Reserved		Baud rate generator UART (LIN) 0 to 6
000090$_H$ to 0000CC$_H$	Reserved				Reserved
0000D0$_H$	IBCR0 [R/W] B,H 00000000	IBSR0 [R] B,H 00000000	ITBAH0 [R/W] B,H ------00	ITBAL0 [R/W] B,H 00000000	I^2C 0
0000D4$_H$	ITMKH0 [R/W] B,H 00----11	ITMKL0 [R/W] B,H 11111111	ISMK0 [R/W] B,H 01111111	ISBA0 [R/W] B,H -0000000	
0000D8$_H$	Reserved	IDAR0 [R/W] B,H 00000000	ICCR0 [R/W] B -0011111	Reserved	
0000DC$_H$	IBCR1 [R/W] B,H 00000000	IBSR1 [R] B,H 00000000	ITBAH1 [R/W] B,H ------00	ITBAL1 [R/W] B,H 00000000	I^2C 1
0000E0$_H$	ITMKH1 [R/W] B,H 00----11	ITMKL1 [R/W] B,H 11111111	ISMK1 [R/W] B,H 01111111	ISBA1 [R/W] B,H -0000000	
0000E4$_H$	Reserved	IDAR1 [R/W] B,H 00000000	ICCR1 [R/W] B -0011111	Reserved	
0000E8$_H$ to 0000FC$_H$	Reserved				Reserved
000100$_H$	GCN10 [R/W] B,H 00110010 00010000		Reserved	GCN20 [R/W] B ----0000	PPG control 0 to 3
000104$_H$	GCN11 [R/W] B,H 00110010 00010000		Reserved	GCN21 [R/W] B ----0000	PPG control 4 to 7
000108$_H$	Reserved				Reserved
000110$_H$	PTMR00 [R] H 11111111 11111111		PCSR00 [W] H XXXXXXXX XXXXXXXX		PPG 0
000114$_H$	PDUT00 [W] H XXXXXXXX XXXXXXXX		PCNH00 [R/W] B,H 00000000	PCNL00 [R/W] B,H 000000-0	
000118$_H$	PTMR01 [R] H 11111111 11111111		PCSR01 [W] H XXXXXXXX XXXXXXXX		PPG 1
00011C$_H$	PDUT01 [W] H XXXXXXXX XXXXXXXX		PCNH01 [R/W] B,H 00000000	PCNL01 [R/W] B,H 000000-0	
000120$_H$	PTMR02 [R] H 11111111 11111111		PCSR02 [W] H XXXXXXXX XXXXXXXX		PPG 2
000124$_H$	PDUT02 [W] H XXXXXXXX XXXXXXXX		PCNH02 [R/W] B,H 00000000	PCNL02 [R/W] B,H 000000-0	

(Continued)

Address	Register				Block
	0	1	2	3	
000128H	PTMR03 [R] H 11111111 11111111		PCSR03 [W] H XXXXXXXX XXXXXXXX		PPG 3
00012CH	PDUT03 [W] H XXXXXXXX XXXXXXXX		PCNH03 [R/W] B,H 00000000	PCNL03 [R/W] B,H 000000-0	
000130H	PTMR04 [R] H 11111111 11111111		PCSR04 [W] H XXXXXXXX XXXXXXXX		PPG 4
000134H	PDUT04 [W] H XXXXXXXX XXXXXXXX		PCNH04 [R/W] B,H 00000000	PCNL04 [R/W] B,H 000000-0	
000138H	PTMR05 [R] H 11111111 11111111		PCSR05 [W] H XXXXXXXX XXXXXXXX		PPG 5
00013CH	PDUT05 [W] H XXXXXXXX XXXXXXXX		PCNH05 [R/W] B,H 00000000	PCNL05 [R/W] B,H 000000-0	
000140H	PTMR06 [R] H 11111111 11111111		PCSR06 [W] H XXXXXXXX XXXXXXXX		PGG 6
000144H	PDUT06 [W] H XXXXXXXX XXXXXXXX		PCNH06 [R/W] B,H 00000000	PCNL06 [R/W] B,H 000000-0	
000148H	PTMR07 [R] H 11111111 11111111		PCSR07 [W] H XXXXXXXX XXXXXXXX		PPG 7
00014CH	PDUT07 [W] H XXXXXXXX XXXXXXXX		PCNH07 [R/W] B,H 00000000	PCNL07 [R/W] B,H 000000-0	
000170H to 00017CH	Reserved				Reserved
000180H	Reserved	ICS01 [R/W] B 00000000	Reserved	ICS23 [R/W] B 00000000	Input capture 0 to 3
000184H	IPCP0 [R] H XXXXXXXX XXXXXXXX		IPCP1 [R] H XXXXXXXX XXXXXXXX		
000188H	IPCP2 [R] H XXXXXXXX XXXXXXXX		IPCP3 [R] H XXXXXXXX XXXXXXXX		
00018CH	OCS01 [R/W] 11101100 00001100		OCS23 [R/W] 11101100 00001100		Output compare 0 to 3
000190H	OCCP0 [R/W] H XXXXXXXX XXXXXXXX		OCCP1 [R/W] H XXXXXXXX XXXXXXXX		
000194H	OCCP2 [R/W] H XXXXXXXX XXXXXXXX		OCCP3 [R/W] H XXXXXXXX XXXXXXXX		

(Continued)

Address	Register				Block
	0	1	2	3	
000198H to 00019CH	Reserved				Reserved
0001A0H	ADERH [R/W] B,H,W 00000000 00000000		ADERL [R/W] B,H,W 00000000 00000000		A/D converter
0001A4H	ADCS1 [R/W] B,H 00000000	ADCS0 [R/W] B,H 00000000	ADCR1 [R] B,H 000000XX	ADCR0 [R] B,H XXXXXXXX	
0001A8H	ADCT1 [R/W] B,H 00010000	ADCT0 [R/W] B,H 00101100	ADSCH [R/W] B,H ---00000	ADECH [R/W] B,H ---00000	
0001ACH	Reserved				Reserved
0001B0H	TMRLR0 [W] H XXXXXXXX XXXXXXXX		TMR0 [R] H XXXXXXXX XXXXXXXX		Reload timer 0 (PPG 0, 1)
0001B4H	Reserved		TMCSRC0 [R/W] B,H ---00000	TMCSRC0 [R/W] B,H 0-000000	
0001B8H	TMRLR1 [W] H XXXXXXXX XXXXXXXX		TMR1 [R] H XXXXXXXX XXXXXXXX		Reload timer 1 (PPG 2, 3)
0001BCH	Reserved		TMCSRC1 [R/W] B,H ---00000	TMCSRC1 [R/W] B,H 0-000000	
0001C0H	TMRLR2 [W] H XXXXXXXX XXXXXXXX		TMR2 [R] H XXXXXXXX XXXXXXXX		Reload timer 2 (PPG 4, 5)
0001C4H	Reserved		TMCSRC2 [R/W] B,H ---00000	TMCSRC2 [R/W] B,H 0-000000	
0001C8H	TMRLR3 [W] H XXXXXXXX XXXXXXXX		TMR3 [R] H XXXXXXXX XXXXXXXX		Reload timer 3 (PPG 6, 7)
0001CCH	Reserved		TMCSRC3 [R/W] B,H ---00000	TMCSRC3 [R/W] B,H 0-000000	
0001D0H to 0001E4H	Reserved				Reserved
0001E8H	TMRLR7 [W] H XXXXXXXX XXXXXXXX		TMR7 [R] H XXXXXXXX XXXXXXXX		Reload timer 7 (A/D converter)
0001ECH	Reserved		TMCSRC7 [R/W] B,H ---00000	TMCSRC7 [R/W] B,H 0-000000	
0001F0H	TCDT0 [R/W] H XXXXXXXX XXXXXXXX		Reserved	TCCS0 [R/W] -0000000	Free-run timer 0 (ICU 0, 1)

(Continued)

Address	Register				Block
	0	1	2	3	
0001F4H	TCDT1 [R/W] H XXXXXXXX XXXXXXXX		Reserved	TCCS1 [R/W] -0000000	Free-run timer 1 (ICU 2, 3)
0001F8H	TCDT2 [R/W] H XXXXXXXX XXXXXXXX		Reserved	TCCS2 [R/W] -0000000	Free-run timer 2 (OCU 0, 1)
0001FCH	TCDT3 [R/W] H XXXXXXXX XXXXXXXX		Reserved	TCCS3 [R/W] -0000000	Free-run timer 3 (OCU 2, 3)
000200H	DMACA0 [R/W] B,H,W*1 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC
000204H	DMACB0 [R/W] B,H,W 00000000 00000000 XXXXXXXX XXXXXXXX				
000208H	DMACA1 [R/W] B,H,W*1 00000000 0000XXXX XXXXXXXX XXXXXXXX				
00020CH	DMACB1 [R/W] B,H,W 00000000 00000000 XXXXXXXX XXXXXXXX				
000210H	DMACA2 [R/W] B,H,W*1 00000000 0000XXXX XXXXXXXX XXXXXXXX				
000214H	DMACB2 [R/W] B,H,W 00000000 00000000 XXXXXXXX XXXXXXXX				
000218H	DMACA3 [R/W] B,H,W*1 00000000 0000XXXX XXXXXXXX XXXXXXXX				
00021CH	DMACB3 [R/W] B,H,W 00000000 00000000 XXXXXXXX XXXXXXXX				
000220H	DMACA4 [R/W] B,H,W*1 00000000 0000XXXX XXXXXXXX XXXXXXXX				
000224H	DMACB4 [R/W] B,H,W 00000000 00000000 XXXXXXXX XXXXXXXX				
000228H to 00023CH	Reserved				
000240H	DMACR [R/W] B,H,W 00--0000	Reserved			
000244H to 000254H	Reserved				Reserved
000258H to 000364H	Reserved				

(Continued)

Address	Register				Block
	0	1	2	3	
000368H	IBCR2 [R/W] B,H 00000000	IBSR2 [R] B,H 00000000	ITBAH2 [R/W] B,H ------00	ITBAL2 [R/W] B,H 00000000	I²C 2
00036CH	ITMKH2 [R/W] B,H 00----11	ITMKL2 [R/W] B,H 11111111	ISMK2 [R/W] B,H 01111111	ISBA2 [R/W] B,H -0000000	
000370H	Reserved	IDAR2 [R/W] B,H 00000000	ICCR2 [R/W] B -0011111	Reserved	
000374H to 0003BCH	Reserved				Reserved
0003C0H	Reserved				
0003C4H	Reserved			ISIZE [R/W] B ------11	Instruction cache
0003D0H	Reserved				Reserved
0003E4H	Reserved			ICHRC [R/W] B 0-000000	Instruction cache
0003E8H to 0003ECH	Reserved				Reserved
0003F0H	BSD0 [W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Bit search module
0003F4H	BSD1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003F8H	BSDC [W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003FCH	BSRR [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000400H to 00043CH	Reserved				Reserved
000440H	ICR00 [R/W] B,H,W ---11111	ICR01 [R/W] B,H,W ---11111	ICR02 [R/W] B,H,W ---11111	ICR03 [R/W] B,H,W ---11111	Interrupt controller
000444H	ICR04 [R/W] B,H,W ---11111	ICR05 [R/W] B,H,W ---11111	ICR06 [R/W] B,H,W ---11111	ICR07 [R/W] B,H,W ---11111	
000448H	ICR08 [R/W] B,H,W ---11111	ICR09 [R/W] B,H,W ---11111	Reserved	ICR11 [R/W] B,H,W ---11111	
00044CH	ICR12 [R/W] B,H,W ---11111	ICR13 [R/W] B,H,W ---11111	Reserved		

(Continued)

Address	Register				Block
	0	1	2	3	
000450H	ICR16 [R/W] B,H,W ---11111	Reserved		ICR19 [R/W] B,H,W ---11111	Interrupt controller
000454H	ICR20 [R/W] B,H,W ---11111	ICR21 [R/W] B,H,W ---11111	ICR22 [R/W] B,H,W ---11111	ICR23 [R/W] B,H,W ---11111	
000458H	Reserved	ICR25 [R/W] B,H,W ---11111	ICR26 [R/W] B,H,W ---11111	ICR27 [R/W] B,H,W ---11111	
00045CH	Reserved	ICR29 [R/W] B,H,W ---11111	Reserved		
000460H	Reserved				
000464H	Reserved		ICR38 [R/W] B,H,W ---11111	ICR39 [R/W] B,H,W ---11111	
000468H	Reserved		ICR42 [R/W] B,H,W ---11111	ICR43 [R/W] B,H,W ---11111	
00046CH	Reserved				
000470H	ICR48 [R/W] B,H,W ---11111	ICR49 [R/W] B,H,W ---11111	ICR50 [R/W] B,H,W ---11111	ICR51 [R/W] B,H,W ---11111	
000474H	Reserved				
000478H	Reserved		ICR58 [R/W] B,H,W ---11111	ICR59 [R/W] B,H,W ---11111	
00047CH	Reserved		ICR62 [R/W] B,H,W ---11111	ICR63 [R/W] B,H,W ---11111	
000480H	RSRR [R/W] B,H,W 10000000	STCR [R/W] B,H,W 00110011	TBCR [R/W] B,H,W X0000X00	CTBR [W] B,H,W XXXXXXXX	Clock control
000484H	CLKR [R/W] B,H,W 00000000	WPR [W] B,H,W XXXXXXXX	DIVR0 [R/W] B,H,W 00000011	DIVR1 [R/W] B,H,W 00000000	
000488H	Reserved				Reserved

(Continued)

Address	Register				Block
	0	1	2	3	
00048CH	PLLDIVM [R/W] B,H ---00000	PLLDIVN [R/W] B,H ---00000	Reserved		PLL interface
000490H	Reserved				Reserved
000494H to 00049CH	Reserved				
0004A0H	Reserved	WTCER [R/W] B,H ------00	WTCR [R/W] B,H 00000000 000-00-0		Real-time clock
0004A4H	Reserved	WTBR [R/W] B, B,H ---XXXXX XXXXXXXX XXXXXXXX			
0004A8H	WTHR [R/W] B,H ---XXXXX	WTMR [R/W] B,H --XXXXXX	WTSR [R/W] B --XXXXXX	Reserved	
0004ACH to 0004BCH	Reserved				Reserved
0004C0H	CANPRE [R/W] B,H 00000000	Reserved			CAN (clock control)
0004C4H	Reserved			HWDCS [R/W,W] B 00011000	Hardware watchdog
0004C8H	OSCR [R/W] B,H 00---000	Reserved			Interval timer
0004CCH	Reserved				Reserved
0004D0H	Reserved				
0004D4H	SHDE [R/W] B 0-------	Reserved	EXTE [R/W] B,H 00000000	EXTF [R/W] B,H 00000000	Shutdown controller
0004D8H	EXTLV [R/W] B,H 00000000 00000000		Reserved		
0004DCH to 00063CH	Reserved				Reserved
000640H	ASR0 [R/W] B,H,W 00000000 00000000		ACR0*2 [R/W] B,H,W 1111XX00 00000000		External bus
000644H	ASR1 [R/W] B,H,W XXXXXXXX XXXXXXXX		ACR1 [R/W] B,H,W XXXXXXXX XXXXXXXX		
000648H	ASR2 [R/W] B,H,W XXXXXXXX XXXXXXXX		ACR2 [R/W] B,H,W XXXXXXXX XXXXXXXX		
00064CH	ASR3 [R/W] B,H,W XXXXXXXX XXXXXXXX		ACR3 [R/W] B,H,W XXXXXXXX XXXXXXXX		

(Continued)

Address	Register				Block
	0	1	2	3	
000650H	ASR4 [R/W] B,H,W XXXXXXXX XXXXXXXX		ACR4 [R/W] B,H,W XXXXXXXX XXXXXXXX		External bus
000654H	Reserved				
000658H	Reserved				
00065CH	Reserved				
000660H	AWR0 [R/W] B,H,W 01111111 11111011		AWR1 [R/W] B,H,W XXXXXXXX XXXXXXXX		
000664H	AWR2 [R/W] B,H,W XXXXXXXX XXXXXXXX		AWR3 [R/W] B,H,W XXXXXXXX XXXXXXXX		
000668H	AWR4 [R/W] B,H,W XXXXXXXX XXXXXXXX		Reserved		
00066CH	Reserved				
000670H	Reserved				
000674H	Reserved				
000678H	IOWR0 [R/W] B,H,W XXXXXXXX	IOWR1 [R/W] B,H,W XXXXXXXX	IOWR2 [R/W] B,H,W XXXXXXXX	Reserved	
00067CH	Reserved				
000680H	CSER [R/W] B,H,W 00000001	CHER [R/W] B,H,W 11111111	Reserved	TCR [R/W]*3 B,H,W 0000XXXX	
000684H	Reserved				
000688H to 0007F8H	Reserved				
0007FCH	Reserved	MODR [W] B XXXXXXXX	Reserved		Mode register
000800H to 000CFCH	Reserved				Reserved
000D00H	Reserved				R-bus port data direct read register
000D04H	Reserved				
000D08H	Reserved				
000D0CH	Reserved		PDRD14 [R] B,H ----XXXX	PDRD15 [R] B,H ----XXXX	
000D10H	PDRD16 [R] B,H X-------	PDRD17 [R] B,H XXXXXXXX	PDRD18 [R] B,H -----XXX	PDRD19 [R] B,H -XXX-XXX	

(Continued)

Address	Register				Block
	0	1	2	3	
000D14H	PDRD20 [R] B,H -XXX-XXX	PDRD21 [R] B,H -XXX-XXX	PDRD22 [R] B,H XXXXXX-X	PDRD23 [R] B,H -X-XXXXX	R-bus port data direct read register
000D18H	PDRD24 [R] B,H XXXXXXXX	Reserved			
000D1CH	PDRD28 [R] B,H ---XXXXX	PDRD29 [R] B,H XXXXXXXX	Reserved		
000D20H	Reserved				
000D24H to 000D3CH	Reserved				Reserved
000D40H	Reserved				R-bus port direction register
000D44H	Reserved				
000D48H	Reserved				
000D4CH	Reserved		DDR14 [R/W] B,H ----0000	DDR15 [R/W] B,H ----0000	
000D50H	DDR16 [R/W] B,H 0-------	DDR17 [R/W] B,H 00000000	DDR18 [R/W] B,H -----000	DDR19 [R/W] B,H -000-000	
000D54H	DDR20 [R/W] B,H -000-000	DDR21 [R/W] B,H -000-000	DDR22 [R/W] B,H 000000-0	DDR23 [R/W] B,H -0-00000	
000D58H	DDR24 [R/W] B,H ---00000	Reserved			
000D5CH	DDR28 [R/W] B,H ---00000	DDR29 [R/W] B,H 00000000	Reserved		
000D60H	Reserved				
000D64H to 000D7CH	Reserved				Reserved
000D80H	Reserved				R-bus port function register
000D84H	Reserved				
000D88H	Reserved				
000D8CH	Reserved		PFR14 [R/W] B,H ----0000	PFR15 [R/W] B,H ----0000	
000D90H	PFR16 [R/W] B,H 0-------	PFR17 [R/W] B,H 00000000	PFR18 [R/W] B,H -----000	PFR19 [R/W] B,H -000-000	

(Continued)

Address	Register				Block
	0	1	2	3	
000D94H	PFR20 [R/W] B,H -000-000	PFR21 [R/W] B,H -000-000	PFR22 [R/W] B,H 000000-0	PFR23 [R/W] B,H -0-00000	R-bus port function register
000D98H	PFR24 [R/W] B,H 00000000	Reserved	Reserved	Reserved	
000D9CH	PFR28 [R/W] B,H ---00000	PFR29 [R/W] B,H 00000000	Reserved	Reserved	
000DA0H	Reserved				
000DA4H to 000DBCH	Reserved				Reserved
000DC0H	Reserved				R-bus expansion port function register
000DC4H	Reserved				
000DC8H	Reserved				
000DCCH	Reserved		EPFR14 [R/W] B,H ----0000	EPFR15 [R/W] B,H ----0000	
000DD0H	EPFR16 [R/W] B,H 0-------	EPFR17 [R/W] B,H 00000000	EPFR18 [R/W] B,H -----000	EPFR19 [R/W] B,H -000-000	
000DD4H	EPFR20 [R/W] B,H -000-000	EPFR21 [R/W] B,H -000-000	EPFR22 [R/W] B,H 000000-0	EPFR23 [R/W] B,H -0-00000	
000DD8H	EPFR24 [R/W] B,H 00000000	Reserved			
000DDCH	EPFR28 [R/W] B,H ---00000	EPFR29 [R/W] B,H 00000000	Reserved		
000DE0H	Reserved				
000DE4H to 000DFCH	Reserved				Reserved
000E00H to 000E3CH	Reserved				

(Continued)

Address	Register				Block
	0	1	2	3	
000E40H	Reserved				R-bus pin input level selection register
000E44H	Reserved				
000E48H	Reserved				
000E4CH	Reserved		PILR14 [R/W] B,H ----0000	PILR15 [R/W] B,H ----0000	
000E50H	PILR16 [R/W] B,H 0-------	PILR17 [R/W] B,H 00000000	PILR18 [R/W] B,H -----000	PILR19 [R/W] B,H -000-000	
000E54H	PILR20 [R/W] B,H -000-000	PILR21 [R/W] B,H -000-000	PILR22 [R/W] B,H 000000-0	PILR23 [R/W] B,H -0-00000	
000E58H	PILR24 [R/W] B,H 00000000	Reserved			
000E5CH	PILR28 [R/W] B,H ---00000	PILR29 [R/W] B,H 00000000	Reserved		
000E60H to 000EBCH	Reserved				
000EC0H	Reserved				R-bus port pull-up/pull-down enable register
000EC4H	Reserved				
000EC8H	Reserved				
000ECCH	Reserved		PPER14 [R/W] B,H ----0000	PPER15 [R/W] B,H ----0000	
000ED0H	PPER16 [R/W] B,H 0-------	PPER17 [R/W] B,H 00000000	PPER18 [R/W] B,H -----000	PPER19 [R/W] B,H -000-000	
000ED4H	PPER20 [R/W] B,H -000-000	PPER21 [R/W] B,H -000-000	PPER22 [R/W] B,H 000000-0	PPER23 [R/W] B,H -0-00000	
000ED8H	PPER24 [R/W] B,H 00000000	Reserved			
000EDCH	PPER28 [R/W] B,H ---00000	PPER29 [R/W] B,H 00000000	Reserved		
000EE0H	Reserved				

(Continued)

Address	Register				Block
	0	1	2	3	
000EE4H to 000EFCH	Reserved				Reserved
000F00H	Reserved				R-bus port pull-up/pull-down control register
000F04H	Reserved				
000F08H	Reserved				
000F0CH	Reserved		PPCR14 [R/W] B,H ----1111	PPCR15 [R/W] B,H ----1111	
000F10H	PPCR16 [R/W] B,H 1-------	PPCR17 [R/W] B,H -111-111	PPCR18 [R/W] B,H 111111-1	PPCR19 [R/W] B,H -1-11111	
000F14H	PPCR20 [R/W] B,H -111-111	PPCR21 [R/W] B,H -111-111	PPCR22 [R/W] B,H 111111-1	PPCR23 [R/W] B,H -1-11111	
000F18H	PPCR24 [R/W] B,H ---11111	Reserved			
000F1CH	PPCR28 [R/W] B,H ---11111	PPCR29 [R/W] B,H 11111111	Reserved		
000F20H	Reserved				
000F24H to 000F3CH	Reserved				Reserved
001000H	DMASA0 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DMAC
001004H	DMADA0 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001008H	DMASA1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00100CH	DMADA1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001010H	DMASA2 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001014H	DMADA2 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

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Address	Register				Block
	0	1	2	3	
001018H	DMASA3 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DMAC
00101CH	DMADA3 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001020H	DMASA4 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001024H	DMADA4 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001028H to 007FFCH	Reserved				Reserved
008000H to 00BFFCH	Reserved				
00C000H	CTRLR0 [R/W] B,H 00000000 00000001		STATR0 [R/W] B,H 00000000 00000000		CAN 0 control register
00C004H	ERRCNT0 [R] B,H,W 00000000 00000000		BTR0 [R/W] B,H,W 00100011 00000001		
00C008H	INTR0 [R]B,H,W 00000000 00000000		TESTR0 [R/W]B,H,W 00000000 X0000000		
00C00CH	BRPE0 [R/W]B,H,W 00000000 00000000		Reserved		
00C010H	IF1CREQ0 [R/W] B,H 00000000 00000001		IF1CMSK0 [R/W] B,H 00000000 00000000		CAN 0 IF 1 register
00C014H	IF1MSK20 [R/W] B,H,W 11111111 11111111		IF1MSK10 [R/W] B,H,W 11111111 11111111		
00C018H	IF1ARB20 [R/W] B,H,W 00000000 00000000		IF1ARB10 [R/W] B,H,W 00000000 00000000		
00C01CH	IF1MCTR0 [R/W] B,H,W 00000000 00000000		Reserved		
00C020H	IF1DTA10 [R/W] B,H,W 00000000 00000000		IF1DTA20 [R/W] B,H,W 00000000 00000000		
00C024H	IF1DTB10 [R/W] B,H,W 00000000 00000000		IF1DTB20 [R/W]B,H,W 00000000 00000000		
00C028H to 00C02CH	Reserved				
00C030H	IF1DTA20 [R/W] B,H,W 00000000 00000000		IF1DTA10 [R/W] B,H,W 00000000 00000000		
00C034H	IF1DTB20 [R/W] B,H,W 00000000 00000000		IF1DTB10 [R/W] B,H,W 00000000 00000000		

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Address	Register				Block
	0	1	2	3	
00C038H to 00C03CH	Reserved				CAN 0 IF 1 register
00C040H	IF2CREQ0 [R/W] B,H 00000000 00000001		IF2CMSK0 [R/W] B,H 00000000 00000000		CAN 0 IF 2 register
00C044H	IF2MSK20 [R/W] B,H,W 11111111 11111111		IF2MSK10 [R/W] B,H,W 11111111 11111111		
00C048H	IF2ARB20 [R/W] B,H,W 00000000 00000000		IF2ARB10 [R/W] B,H,W 00000000 00000000		
00C04CH	IF2MCTR0 [R/W] B,H,W 00000000 00000000		Reserved		
00C050H	IF2DTA10 [R/W] B,H,W 00000000 00000000		IF2DTA20 [R/W] B,H,W 00000000 00000000		
00C054H	IF2DTB10 [R/W] B,H,W 00000000 00000000		IF2DTB20 [R/W] B,H,W 00000000 00000000		
00C058H to 00C05CH	Reserved				
00C060H	IF2DTA20 [R/W] B,H,W 00000000 00000000		IF2DTA10 [R/W] B,H,W 00000000 00000000		
00C064H	IF2DTB20 [R/W] B,H,W 00000000 00000000		IF2DTB10 [R/W] B,H,W 00000000 00000000		
00C068H to 00C07CH	Reserved				
00C080H	TREQR20 [R] B,H,W 00000000 00000000		TREQR10 [R] B,H,W 00000000 00000000		CAN 0 status flag
00C084H	Reserved				
00C088H	Reserved				
00C08CH	Reserved				
00C090H	NEWDT20 [R] B,H,W 00000000 00000000		NEWDT10 [R] B,H,W 00000000 00000000		
00C094H	Reserved				
00C098H	Reserved				
00C09CH	Reserved				

(Continued)

Address	Register				Block
	0	1	2	3	
00C0A0H	INTPND20 [R] B,H,W 00000000 00000000		INTPND10 [R] B,H,W 00000000 00000000		CAN 0 status flag
00C0A4H	Reserved				
00C0A8H	Reserved				
00C0ACH	Reserved				
00C0B0H	MSGVAL20 [R] B,H,W 00000000 00000000		MSGVAL10 [R] B,H,W 00000000 00000000		
00C0B4H	Reserved				
00C0B8H	Reserved				
00C0BCH	Reserved				
00C0C0H to 00C0FCH	Reserved				
00C100H	CTRLR1 [R/W] B,H 00000000 00000001		STATR1 [R/W] B,H 00000000 00000000		CAN 1 control register
00C104H	ERRCNT1 [R] B,H,W 00000000 00000000		BTR1 [R/W] B,H,W 00100011 00000001		
00C108H	INTR1 [R] B,H,W 00000000 00000000		TESTR1 [R/W] B,H,W 00000000 X0000000		
00C10CH	BRPE1 [R/W] B,H,W 00000000 00000000		Reserved		
00C110H	IF1CREQ1 [R/W] B,H 00000000 00000001		IF1CMSK1 [R/W] B,H 00000000 00000000		CAN 1 IF 1 register
00C114H	IF1MSK21 [R/W] B,H,W 11111111 11111111		IF1MSK11 [R/W] B,H,W 11111111 11111111		
00C118H	IF1ARB21 [R/W] B,H,W 00000000 00000000		IF1ARB11 [R/W] B,H,W 00000000 00000000		
00C11CH	IF1MCTR1 [R/W] B,H,W 00000000 00000000		Reserved		
00C120H	IF1DTA11 [R/W] B,H,W 00000000 00000000		IF1DTA21 [R/W] B,H,W 00000000 00000000		
00C124H	IF1DTB11 [R/W] B,H,W 00000000 00000000		IF1DTB21 [R/W] B,H,W 00000000 00000000		

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Address	Register				Block
	0	1	2	3	
00C128H to 00C12CH	Reserved				CAN 1 IF 1 register
00C130H	IF1DTA21 [R/W] B,H,W 00000000 00000000		IF1DTA11 [R/W] B,H,W 00000000 00000000		
00C134H	IF1DTB21 [R/W] B,H,W 00000000 00000000		IF1DTB11 [R/W] B,H,W 00000000 00000000		
00C138H to 00C13CH	Reserved				
00C140H	IF2CREQ1 [R/W]B,H 00000000 00000001		IF2CMSK1 [R/W]B,H 00000000 00000000		CAN 1 IF 2 register
00C144H	IF2MSK21 [R/W]B,H,W 11111111 11111111		IF2MSK11 [R/W]B,H,W 11111111 11111111		
00C148H	IF2ARB21 [R/W]B,H,W 00000000 00000000		IF2ARB11 [R/W]B,H,W 00000000 00000000		
00C14CH	IF2MCTR1 [R/W]B,H,W 00000000 00000000		Reserved		
00C150H	IF2DTA11 [R/W]B,H,W 00000000 00000000		IF2DTA21 [R/W]B,H,W 00000000 00000000		
00C154H	IF2DTB11 [R/W]B,H,W 00000000 00000000		IF2DTB21 [R/W]B,H,W 00000000 00000000		
00C158H to 00C15CH	Reserved				
00C160H	IF2DTA21 [R/W]B,H,W 00000000 00000000		IF2DTA11 [R/W]B,H,W 00000000 00000000		
00C164H	IF2DTB21 [R/W]B,H,W 00000000 00000000		IF2DTB11 [R/W]B,H,W 00000000 00000000		
00C168H to 00C17CH	Reserved				
00C180H	TREQR21 [R]B,H,W 00000000 00000000		TREQR11 [R]B,H,W 00000000 00000000		CAN 1 status flag
00C184H	Reserved				
00C188H	Reserved				
00C18CH	Reserved				

(Continued)

Address	Register				Block
	0	1	2	3	
00C190H	NEWDT21 [R]B,H,W 00000000 00000000		NEWDT11 [R]B,H,W 00000000 00000000		CAN 1 status flag
00C194H	Reserved				
00C198H	Reserved				
00C19CH	Reserved				
00C1A0H	INTPND21 [R]B,H,W 00000000 00000000		INTPND11 [R]B,H,W 00000000 00000000		
00C1A4H	Reserved				
00C1A8H	Reserved				
00C1ACH	Reserved				
00C1B0H	MSGVAL21 [R]B,H,W 00000000 00000000		MSGVAL11 [R]B,H,W 00000000 00000000		
00C1B4H	Reserved				
00C1B8H	Reserved				
00C1BCH	Reserved				
00C1C0H to 00C1FCH	Reserved				
00F000H to 00FFFCH	Reserved				Reserved
010000H to 013FFCH	Cache TAG way 1 (010000H to 0107FCH)				Instruction cache
014000H to 017FFCH	Cache TAG way 2 (014000H to 0147FCH)				
018000H to 01BFFCH	Cache RAM way 1 (018000H to 0187FCH)				
01C000H to 01FFFCH	Cache RAM way 2 (01C000H to 01C7FCH)				

(Continued)

(Continued)

Address	Register				Block
	0	1	2	3	
020000H to 02FFFCH	Reserved				Reserved
030000H to 03FFFCH	I/D-RAM: 64 Kbytes (instruction access is 0 wait cycle, data access is 1 wait cycle)				I/D-RAM 64 Kbytes
040000H to 07FFFCH	External memory area (256 Kbytes)				External bus
080000H to 0BFFFCH	External memory area (256 Kbytes)				
0C0000H to 0FFFF4H	External memory area (256 Kbytes)				
0FFFF8H	FMV [R]				Reset vector/ mode vector
0FFFFCH	FRV [R]				
100000H to 13FFFCH	External memory area (256 Kbytes)				External bus
140000H to 17FFFCH	External memory area (256 Kbytes)				
180000H to 1BFFFCH	External memory area (256 Kbytes)				
1C0000H to 1FFFFCH	External memory area (256 Kbytes)				
200000H to 2FFFFCH	External memory area (1 Mbyte)				
300000H to 3FFFFCH	External memory area (1 Mbyte)				

*1 : The lower 16 bits (DTC15 to DTC0) of DMACA0 to DMACA4 cannot be accessed in bytes.

*2 : ACR0[11:10] depends on the mode vector fetch information on bus width.

*3 : TCR[3:0] INIT value = 0000, the value is kept after RST.

■ INTERRUPT SOURCE TABLE

Interrupt source	Interrupt number		Interrupt level		Offset	TBR default address	Resource number*1
	Decimal	Hexadecimal	Setting register	Register address			
Reset	0	00	—	—	3FC$_H$	000FFFFC$_H$	2
Mode vector	1	01	—	—	3F8$_H$	000FFFF8$_H$	3
System reserved	2	02	—	—	3F4$_H$	000FFFF4$_H$	—
System reserved	3	03	—	—	3F0$_H$	000FFFF0$_H$	—
System reserved	4	04	—	—	3EC$_H$	000FFFEC$_H$	—
System reserved	5	05	—	—	3E8$_H$	000FFFE8$_H$	—
System reserved	6	06	—	—	3E4$_H$	000FFFE4$_H$	—
Coprocessor absent trap	7	07	—	—	3E0$_H$	000FFFE0$_H$	—
Coprocessor error trap	8	08	—	—	3DC$_H$	000FFFDC$_H$	—
INTE instruction	9	09	—	—	3D8$_H$	000FFFD8$_H$	—
Instruction break exception	10	0A	—	—	3D4$_H$	000FFFD4$_H$	—
Operand break trap	11	0B	—	—	3D0$_H$	000FFFD0$_H$	—
Step trace trap	12	0C	—	—	3CC$_H$	000FFFCC$_H$	—
NMI request (tool)	13	0D	—	—	3C8$_H$	000FFFC8$_H$	—
Undefined instruction exception	14	0E	—	—	3C4$_H$	000FFFC4$_H$	—
NMI request	15	0F	15 (F) fixed	15 (F) fixed	3C0$_H$	000FFFC0$_H$	—
External interrupt 0	16	10	ICR00	440$_H$	3BC$_H$	000FFFBC$_H$	—
External interrupt 1	17	11			3B8$_H$	000FFFB8$_H$	—
External interrupt 2	18	12	ICR01	441$_H$	3B4$_H$	000FFFB4$_H$	—
External interrupt 3	19	13			3B0$_H$	000FFFB0$_H$	—
External interrupt 4	20	14	ICR02	442$_H$	3AC$_H$	000FFFAC$_H$	—
External interrupt 5	21	15			3A8$_H$	000FFFA8$_H$	—
External interrupt 6	22	16	ICR03	443$_H$	3A4$_H$	000FFFA4$_H$	—
External interrupt 7	23	17			3A0$_H$	000FFFA0$_H$	—
External interrupt 8	24	18	ICR04	444$_H$	39C$_H$	000FFF9C$_H$	—
External interrupt 9	25	19			398$_H$	000FFF98$_H$	—
External interrupt 10	26	1A	ICR05	445$_H$	394$_H$	000FFF94$_H$	—
External interrupt 11	27	1B			390$_H$	000FFF90$_H$	—
External interrupt 12	28	1C	ICR06	446$_H$	38C$_H$	000FFF8C$_H$	—
External interrupt 13	29	1D			388$_H$	000FFF88$_H$	—
External interrupt 14	30	1E	ICR07	447$_H$	384$_H$	000FFF84$_H$	—
External interrupt 15	31	1F			380$_H$	000FFF80$_H$	—

(Continued)

Interrupt source	Interrupt number		Interrupt level		Offset	TBR default address	Resource number*1
	Decimal	Hexadecimal	Setting register	Register address			
Reload timer 0	32	20	ICR08	448H	37CH	000FFF7CH	4
Reload timer 1	33	21			378H	000FFF78H	5
Reload timer 2	34	22	ICR09	449H	374H	000FFF74H	—
Reload timer 3	35	23			370H	000FFF70H	—
System reserved	36	24	ICR10	44AH	36CH	000FFF6CH	—
System reserved	37	25			368H	000FFF68H	—
System reserved	38	26	ICR11	44BH	364H	000FFF64H	—
Reload timer 7	39	27			360H	000FFF60H	—
Free-run timer 0	40	28	ICR12	44CH	35CH	000FFF5CH	—
Free-run timer 1	41	29			358H	000FFF58H	—
Free-run timer 2	42	2A	ICR13	44DH	354H	000FFF54H	—
Free-run timer 3	43	2B			350H	000FFF50H	—
System reserved	44	2C	ICR14	44EH	34CH	000FFF4CH	—
System reserved	45	2D			348H	000FFF48H	—
System reserved	46	2E	ICR15	44FH	344H	000FFF44H	—
System reserved	47	2F			340H	000FFF40H	—
CAN0	48	30	ICR16	450H	33CH	000FFF3CH	—
CAN1	49	31			338H	000FFF38H	—
System reserved	50	32	ICR17	451H	334H	000FFF34H	—
System reserved	51	33			330H	000FFF30H	—
System reserved	52	34	ICR18	452H	32CH	000FFF2CH	—
System reserved	53	35			328H	000FFF28H	—
LIN-USART 0 RX	54	36	ICR19	453H	324H	000FFF24H	6
LIN-USART 0 TX	55	37			320H	000FFF20H	7
LIN-USART 1 RX	56	38	ICR20	454H	31CH	000FFF1CH	8
LIN-USART 1 TX	57	39			318H	000FFF18H	9
LIN-USART 2 RX	58	3A	ICR21	455H	314H	000FFF14H	—
LIN-USART 2 TX	59	3B			310H	000FFF10H	—
LIN-USART 3 RX	60	3C	ICR22	456H	30CH	000FFF0CH	—
LIN-USART 3 TX	61	3D			308H	000FFF08H	—
System reserved	62	3E	ICR23*3	457H	304H	000FFF04H	—
Delay interrupt	63	3F			300H	000FFF00H	—

(Continued)

Interrupt source	Interrupt number		Interrupt level		Offset	TBR default address	Resource number*1
	Decimal	Hexadecimal	Setting register	Register address			
System reserved*2	64	40	(ICR24)	458H	2FCH	000FFEFCH	—
System reserved*2	65	41			2F8H	000FFEF8H	—
LIN-USART 4 RX	66	42	ICR25	459H	2F4H	000FFEF4H	10
LIN-USART 4 TX	67	43			2F0H	000FFEF0H	11
LIN-USART 5 RX	68	44	ICR26	45AH	2ECH	000FFEECH	12
LIN-USART 5 TX	69	45			2E8H	000FFEE8H	13
LIN-USART 6 RX	70	46	ICR27	45BH	2E4H	000FFEE4H	—
LIN-USART 6 TX	71	47			2E0H	000FFEE0H	—
System reserved	72	48	ICR28	45CH	2DCH	000FFEDCH	—
System reserved	73	49			2D8H	000FFED8H	—
I²C_0/I²C_2	74	4A	ICR29	45DH	2D4H	000FFED4H	—
I²C_1/I²C_3	75	4B			2D0H	000FFED0H	—
System reserved	76	4C	ICR30	45EH	2CCH	000FFECCH	—
System reserved	77	4D			2C8H	000FFEC8H	—
System reserved	78	4E	ICR31	45FH	2C4H	000FFEC4H	—
System reserved	79	4F			2C0H	000FFEC0H	—
System reserved	80	50	ICR32	460H	2BCH	000FFEBCH	—
System reserved	81	51			2B8H	000FFEB8H	—
System reserved	82	52	ICR33	461H	2B4H	000FFEB4H	—
System reserved	83	53			2B0H	000FFEB0H	—
System reserved	84	54	ICR34	462H	2ACH	000FFEACH	—
System reserved	85	55			2A8H	000FFEA8H	—
System reserved	86	56	ICR35	463H	2A4H	000FFEA4H	—
System reserved	87	57			2A0H	000FFEA0H	—
System reserved	88	58	ICR36	464H	29CH	000FFE9CH	—
System reserved	89	59			298H	000FFE98H	—
System reserved	90	5A	ICR37	465H	294H	000FFE94H	—
System reserved	91	5B			290H	000FFE90H	—
Input capture 0	92	5C	ICR38	466H	28CH	000FFE8CH	—
Input capture 1	93	5D			288H	000FFE88H	—
Input capture 2	94	5E	ICR39	467H	284H	000FFE84H	—
Input capture 3	95	5F			280H	000FFE80H	—

(Continued)

Interrupt source	Interrupt number		Interrupt level		Offset	TBR default address	Resource number*1
	Decimal	Hexadecimal	Setting register	Register address			
System reserved	96	60	ICR40	468H	27CH	000FFE7CH	—
System reserved	97	61			278H	000FFE78H	—
System reserved	98	62	ICR41	469H	274H	000FFE74H	—
System reserved	99	63			270H	000FFE70H	—
Output compare 0	100	64	ICR42	46AH	26CH	000FFE6CH	—
Output compare 1	101	65			268H	000FFE68H	—
Output compare 2	102	66	ICR43	46BH	264H	000FFE64H	—
Output compare 3	103	67			260H	000FFE60H	—
System reserved	104	68	ICR44	46CH	25CH	000FFE5CH	—
System reserved	105	69			258H	000FFE58H	—
System reserved	106	6A	ICR45	46DH	254H	000FFE54H	—
System reserved	107	6B			250H	000FFE50H	—
System reserved	108	6C	ICR46	46EH	24CH	000FFE4CH	—
System reserved	109	6D			248H	000FFE48H	—
System reserved	110	6E	ICR47*3	46FH	244H	000FFE44H	—
System reserved	111	6F			240H	000FFE40H	—
PPG0	112	70	ICR48	470H	23CH	000FFE3CH	15
PPG1	113	71			238H	000FFE38H	—
PPG2	114	72	ICR49	471H	234H	000FFE34H	—
PPG3	115	73			230H	000FFE30H	—
PPG4	116	74	ICR50	472H	22CH	000FFE2CH	—
PPG5	117	75			228H	000FFE28H	—
PPG6	118	76	ICR51	473H	224H	000FFE24H	—
PPG7	119	77			220H	000FFE20H	—
System reserved	120	78	ICR52	474H	21CH	000FFE1CH	—
System reserved	121	79			218H	000FFE18H	—
System reserved	122	7A	ICR53	475H	214H	000FFE14H	—
System reserved	123	7B			210H	000FFE10H	—
System reserved	124	7C	ICR54	476H	20CH	000FFE0CH	—
System reserved	125	7D			208H	000FFE08H	—
System reserved	126	7E	ICR55	477H	204H	000FFE04H	—
System reserved	127	7F			200H	000FFE00H	—

(Continued)

(Continued)

Interrupt source	Interrupt number		Interrupt level		Offset	TBR default address	Resource number*1
	Decimal	Hexadecimal	Setting register	Register address			
System reserved	128	80	ICR56	478H	1FCH	000FFDFCH	—
System reserved	129	81			1F8H	000FFDF8H	—
System reserved	130	82	ICR57	479H	1F4H	000FFDF4H	—
System reserved	131	83			1F0H	000FFDF0H	—
Real-time clock	132	84	ICR58	47AH	1ECH	000FFDECH	—
System reserved	133	85			1E8H	000FFDE8H	—
A/D converter 0	134	86	ICR59	47BH	1E4H	000FFDE4H	14
System reserved	135	87			1E0H	000FFDE0H	—
System reserved	136	88	ICR60	47CH	1DCH	000FFDDCH	—
System reserved	137	89			1D8H	000FFDD8H	—
System reserved	138	8A	ICR61	47DH	1D4H	000FFDD4H	—
System reserved	139	8B			1D0H	000FFDD0H	—
Time base overflow	140	8C	ICR62	47EH	1CCH	000FFDCCH	—
PLL clock gear	141	8D			1C8H	000FFDC8H	—
DMA controller	142	8E	ICR63	47FH	1C4H	000FFDC4H	—
Main/sub oscillation stabilization wait	143	8F			1C0H	000FFDC0H	—
System reserved	144	90	—	—	1BCH	000FFDBCH	—
Used by INT instruction	145 : 255	91 : FF	—	—	1B8H : 000H	000FFDB8H : 000FFC00H	—

*1 : The peripheral resources to which RN (Resource Number) is assigned are capable of being DMA transfer activation sources. In addition, RN has a one-to-one correspondence with an IS (Input Source) of the DMAC channel control register A(DMACA0 to DMACA4), and the IS (Input Source) can be obtained by representing RN in a binary number and adding “1” to the head of it.

*2 : Used by REALOS

*3 : ICR23 and ICR47 are interchangeable by setting REALOS bit (address 0C03H ISO[0]).

■ ELECTRICAL CHARACTERISTICS

1. Absolute maximum rating

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage 1*1	$V_{CC}3$	V_{SS} – 0.5	V_{SS} + 4.0	V	
Power supply voltage 2*1	$V_{CC}5$	V_{SS} – 0.5	V_{SS} + 6.0	V	
Analog power supply voltage*1	$AV_{CC}3$	V_{SS} – 0.5	V_{SS} + 4.0	V	*2
Analog power supply voltage*1	AVRH	V_{SS} – 0.5	V_{SS} + 4.0	V	*2
Input voltage 1*1	V_{I1}	V_{SS} – 0.3	$V_{CC}3$ + 0.3	V	
Input voltage 2*1	V_{I2}	V_{SS} – 0.3	$V_{CC}5$ + 0.3	V	
Analog pin input voltage*1	V_{IA}	V_{SS} – 0.3	$AV_{CC}3$ + 0.3	V	
Output voltage 1*1	V_{O1}	V_{SS} – 0.3	$V_{CC}3$ + 0.3	V	
Output voltage 2*1	V_{O2}	V_{SS} – 0.3	$V_{CC}3$ + 0.3	V	
Maximum clamp current	I_{CLAMP}	– 2.0	+ 2.0	mA	*6
Total maximum clamp current	$\Sigma \lvert I_{CLAMP} \rvert$	—	20	mA	*6
“L” level maximum output current	I_{OL}	—	10	mA	*3
“L” level average output current	I_{OLAV}	—	8	mA	*4
“L” level total maximum output current	ΣI_{OL}	—	100	mA	
“L” level total average output current	ΣI_{OLAV}	—	50	mA	*5
“H” level maximum output current	I_{OL}	—	– 10	mA	*3
“H” level average output current	I_{OHAV}	—	– 4	mA	*4
“H” level total maximum output current	ΣI_{OH}	—	– 50	mA	
“H” level total average output current	ΣI_{OHAV}	—	– 20	mA	*5
Power consumption	P_D	—	1000	mW	
Operation temperature	T_A	– 40	+ 85	°C	
Storage temperature	Tstg	– 55	+ 125	°C	

*1 : The parameter is based on $V_{SS} = AV_{SS} = 0.0$ V.

*2 : Do not let $AV_{CC}3$ and AVRH exceed V_{CC}+0.3 [V], for example, when the power is turned on. Also, do not let $AV_{CC}3$ exceed $V_{CC}3$.

*3 : Maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

*4 : Average output current is defined as the value of the average current flowing through any one of the corresponding pins for a 100 ms period.

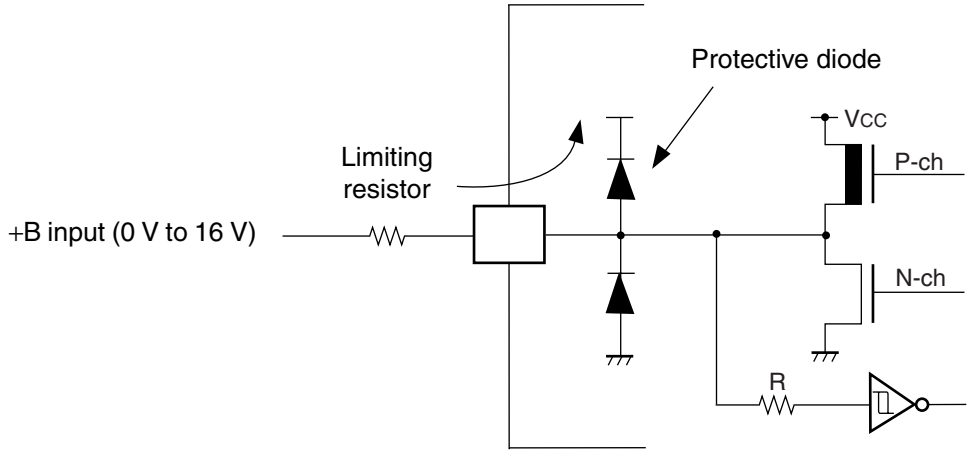
*5 : Total average output current is defined as the value of the average current flowing through all of the corresponding pins for a 100 ms period.

(Continued)

(Continued)

*6 :
- Corresponding pins: Pin number 2, 3, 116, 117, 120 to 125, 134 to 145, 148 to 160, 163 to 175
- Use within recommended operating conditions.
- Use at DC voltage (current).
- The +B signal is an input signal exceeding V_{CC} voltage. The +B signal should always be applied by connecting a limiting resistor between the +B signal and the microcontroller.
- The value of the limiting resistor should be set so that the current input to the microcontroller pin does not exceed rated values at any time regardless of instantaneously or constantly when the +B signal is input.
- Note that when the microcontroller drive current is low, such as in the low power consumption modes, the +B input potential can increase the potential at the V_{CC} pin via a protective diode, possibly affecting other devices.
- Note that if the +B signal is input when the microcontroller is off (not fixed at 0 V), since the power is supplied through the pin, the microcontroller may operate incompletely.
- Note that if the +B signal is input at power-on, since the power is supplied through the pin, the power supply voltage may become the voltage at which a power-on reset does not work.
- Do not leave +B input pin open.
- Note that analog input/output pins cannot accept +B signal input.
- Example of recommended circuit :

• Input/output equivalent circuit



WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended operating conditions

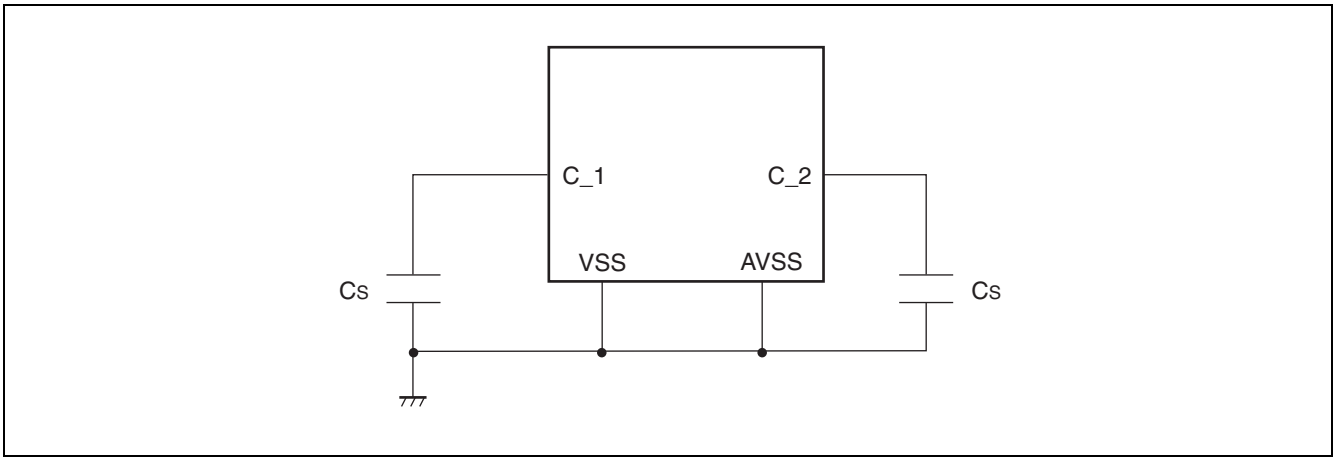
(V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	$V_{CC}5$	4.5	—	5.5	V	
	$V_{CC}3$	3.0	—	3.6	V	
	$AV_{CC}3$	3.0	—	3.6	V	
Smoothing capacitor	C_S	—	4.7 (accuracy within ± 50%)	—	µF	Use a ceramic capacitor or a capacitor having the similar frequency characteristic. For a smoothing capacitor of VCC pin, use one having a capacitance value greater than C_S.
Operating temperature	T_A	− 40	—	+ 85	°C	

WARNING: : The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.



3. DC characteristics

($V_{CC}5$ = 4.5 V to 5.5 V, $V_{CC}3$ = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, T_A = –40 °C to + 85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IH1}	P14_0 to P14_3, P15_0 to P15_3, P16_7, P17_0 to P17_7, P18_0 to P18_2, P19_0 to P19_2, P19_4 to P19_6, P20_0 to P20_2, P20_4 to P20_6, P21_0 to P21_2, P21_4 to P21_6, P22_0, P22_2, P22_3, P23_0 to P23_4, P23_6, P24_0 to P24_3, P24_6, P24_7, P28_0 to P28_4, P29_0 to P29_7, $\overline{NMI}$, BREAK, MD0 to MD3	—	0.8 × V_{CC}	—	V_{CC} + 0.3	V	CMOS hysteresis input*1
	V_{IH2}	P14_0 to P14_3, P15_0 to P15_3, P16_7, P17_0 to P17_7, P18_0 to P18_2, P19_0 to P19_2, P19_4 to P19_6, P20_0 to P20_2, P20_4 to P20_6, P21_0 to P21_2, P21_4 to P21_6, P22_0, P22_2, P22_3, P23_0 to P23_4, P23_6, P24_0 to P24_3, P24_6, P24_7, P28_0 to P28_4, P29_0 to P29_7, D16 to D31, DREQ0, RDY, BRQ, ICD0 to ICD3	—	0.7 × V_{CC}	—	V_{CC} + 0.3	V	CMOS input*1
	V_{IH3}	P22_4 to P22_7, P24_4, P24_5	—	0.7 × V_{CC}	—	$V_{CC}5$ + 0.3	V	I^2C input*2

(Continued)

($V_{CC}5$ = 4.5 V to 5.5 V, $V_{CC}3$ = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, T_A = –40 °C to + 85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
“L“ level input voltage	V_{IL1}	P14_0 to P14_3, P15_0 to P15_3, P16_7, P17_0 to P17_7, P18_0 to P18_2, P19_0 to P19_2, P19_4 to P19_6, P20_0 to P20_2, P20_4 to P20_6, P21_0 to P21_2, P21_4 to P21_6, P22_0, P22_2, P22_3, P23_0 to P23_4, P23_6, P24_0 to P24_3, P24_6, P24_7, P28_0 to P28_4, P29_0 to P29_7, $\overline{NMI}$, BREAK, MD0 to MD3	—	V_{SS}–0.3	—	0.2 × V_{CC}	V	CMOS hysteresis input*1
	V_{IL2}	P14_0 to P14_3, P15_0 to P15_3, P16_7, P17_0 to P17_7, P18_0 to P18_2, P19_0 to P19_2, P19_4 to P19_6, P20_0 to P20_2, P20_4 to P20_6, P21_0 to P21_2, P21_4 to P21_6, P22_0, P22_2, P22_3, P23_0 to P23_4, P23_6, P24_0 to P24_3, P24_6, P24_7, P28_0 to P28_4, P29_0 to P29_7, D16 to D31, DREQ0, RDY, BRQ, ICD0 to ICD3	—	V_{SS}–0.3	—	0.3 × V_{CC}	V	CMOS input*1
	V_{IL3}	P22_4 to P22_7, P24_4, P24_5	—	V_{SS}–0.3	—	0.3 × $V_{CC}3$	V	I^2C input*2

(Continued)

($V_{CC}5$ = 4.5 V to 5.5 V, $V_{CC}3$ = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, T_A = –40 °C to + 85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level output voltage	V_{OH1}	P14_0 to P14_3, P15_0 to P15_3, P17_0 to P17_3, P18_0 to P18_2, P19_0 to P19_2, P19_4 to P19_6, P20_0 to P20_2, P20_4 to P20_6, P21_0 to P21_2, P21_4 to P21_6, P22_0, P22_2, P22_3, P23_0 to P23_4, P23_6, P24_0 to P24_3, P24_6, P24_7	V_{CC} = 5.0 V, I_{OH} = 4.0 mA/ V_{CC} = 3.3 V, I_{OH} = 2.0 mA	V_{CC}–0.5	—	—	V	3.3 V, 5 V switch pin*3
	V_{OH2}	P16_7, P17_4 to P17_7, P28_0 to P18_4, P29_0 to P19_7, D16 to D31, ICD0 to ICD3, A00 to A23, $\overline{AS}$, $\overline{BGRNT}$, $\overline{CS0}$ to $\overline{CS4}$, DACK0, DEOP0, ICLK, ICS0 to ICS2, $\overline{IORD}$, $\overline{IOWR}$, $\overline{RD}$, SYSCLK, $\overline{WDRESET}$, $\overline{WR0}$, $\overline{WR1}$	$V_{CC}3$ = 3.3 V, I_{OH} = 4.0 mA	$V_{CC}3$–0.5	—	—	V	3.3 V dedicated pin

(Continued)

($V_{CC}5$ = 4.5 V to 5.5 V, $V_{CC}3$ = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, T_A = –40 °C to + 85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"L" level output voltage	V_{OL1}	P14_0 to P14_3, P15_0 to P15_3, P17_0 to P17_3, P18_0 to P18_2, P19_0 to P19_2, P19_4 to P19_6, P20_0 to P20_2, P20_4 to P20_6, P21_0 to P21_2, P21_4 to P21_6, P22_0, P22_2, P22_3, P23_0 to P23_4, P23_6, P24_0 to P24_3, P24_6, P24_7	V_{CC} = 5.0 V, I_{OL} = 4.0 mA/ V_{CC} = 3.3 V, I_{OL} = 2.0 mA	—	—	0.4	V	3.3 V, 5 V switch pin*3
	V_{OL2}	P16_7, P17_4 to P17_7, P28_0 to P28_4, P29_0 to P29_7, D16 to D31, ICD0 to ICD3, A00 to A23, $\overline{AS}$, $\overline{BGRNT}$, $\overline{CS0}$ to $\overline{CS4}$, DACK0, DEOP0, ICLK, ICS0 to ICS2, $\overline{IORD}$, $\overline{IOWR}$, $\overline{RD}$, SYSCLK, $\overline{WDRESET}$, $\overline{WR0}$, $\overline{WR1}$	$V_{CC}3$ = 3.3 V, I_{OL} = 4.0 mA	—	—	0.4	V	3.3 V dedicated pin
	V_{OL3}	P22_4 to P22_7, P24_4, P24_5	$V_{CC}3$ = 3.3 V, I_{OL} = 3.0 mA	—	—	0.4	V	I^2C output
Input leak current	I_{IL}	All input pins	V_{CC} = DV_{CC} = AV_{CC} = 5.0 V, V_{SS} < VI < V_{CC}	– 5	—	+5	µA	
Pull-up resistance value	P_{UP}	$\overline{INIT}$, pull-up pin	—	25	50	100	kΩ	
Pull-down resistance value	P_{DOWN}	$\overline{INIT}$, pull-up pin	—	25	50	100	kΩ	

(Continued)

(Continued)

($V_{CC}5$ = 4.5 V to 5.5 V, $V_{CC}3$ = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, T_A = –40 °C to + 85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current	$I_{CC}3$	VCC3	CPU core : 80 MHz, External bus : 40 MHz (no-load) Peripheral macro : 10 MHz CAN : 20 MHz	—	120	150	mA	
	$I_{CC}5$	VCC5	—		15	20	mA	
	I_{CCH}	VCC3	T_A = + 85 °C	—	1	3	mA	At stop
		VCC3	T_A = + 85 °C	—	10	50	µA	At shutdown
Input capacitance	C_{IN}	Except VCC3, VCC5, VSS, AVCC, AVSS, AVRH	f = 1 MHz	—	5	15	pF	

*1 : For a pin which can select the I/O power supply between 3.3 V and 5 V, the value is based on the power supply voltage currently used.
Although 5 V input is possible for $\overline{TRST}$, the input becomes CMOS hysteresis based on the input threshold value $V_{CC}3$.

*2 : Although 5 V input is possible for I^2C pin, the input is made based on the input threshold value $V_{CC}3$.

*3 : For a pin which can select the I/O power supply between 3.3 V and 5 V, the drive capability changes depending on the power supply voltage.

4. AC characteristics

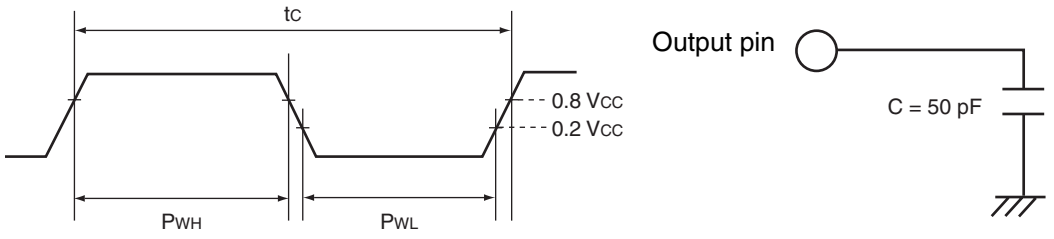
(1) Clock timing

($V_{CC}5$ = 4.5 V to 5.5 V, $V_{CC}3$ = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, T_A = –40 °C to + 85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	f_C	X0 X1	—	10	18.5	20	MHz	
Clock cycle time	t_C	X0 X1		50	54	100	ns	
Internal operation clock frequency	f_{CP}	—	—	4.6	—	80	MHz	CPU
	f_{CPP}			4.6	—	20	MHz	Peripheral
	f_{CPT}			4.6	—	40	MHz	External bus
	f_{CAN}			—	—	20	MHz	Clock after divided by CAN prescaler
Internal operation clock cycle time	t_{CP}	—		12.5	—	217	ns	CPU
	t_{CPP}			50	—	217	ns	Peripheral
	t_{CPT}			26.7	—	217	ns	External bus
	t_{CAN}			50	—	—	ns	Clock after divided by CAN prescaler

Note : These values are assumed based on the division setting of each clock set to 16.

• Conditions for measuring the clock timing ratings

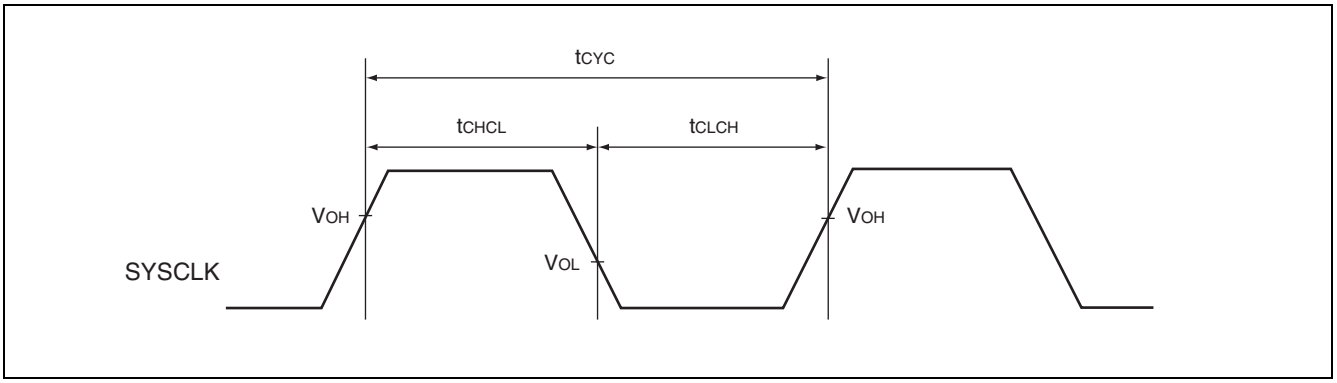


(2) Clock output timing

($V_{CC}5$ = 4.5 V to 5.5 V, $V_{CC}3$ = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, T_A = –40 °C to + 85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Cycle time	t_{CYC}	SYSCLK	—	t_{CPT}	—	ns	*
SYSCLK↑→SYSCLK↓	t_{CHCL}	SYSCLK		12.5	108.5	ns	
SYSCLK↓→SYSCLK↑	t_{CLCH}	SYSCLK		12.5	108.5	ns	

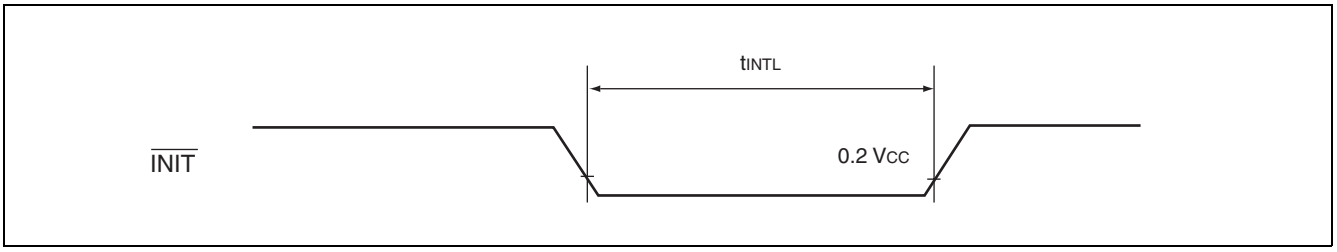
* : t_{CYC} is the frequency of 1 clock cycle.



(3) Reset input ratings

($V_{CC}5$ = 4.5 V to 5.5 V, $V_{CC}3$ = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, T_A = –40 °C to + 85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
$\overline{INIT}$ input time (at power-on, at return from shutdown mode)	t_{INTL}	$\overline{INIT}$	—	8	—	ms
$\overline{INIT}$ input time (other than the above)				20	—	µs

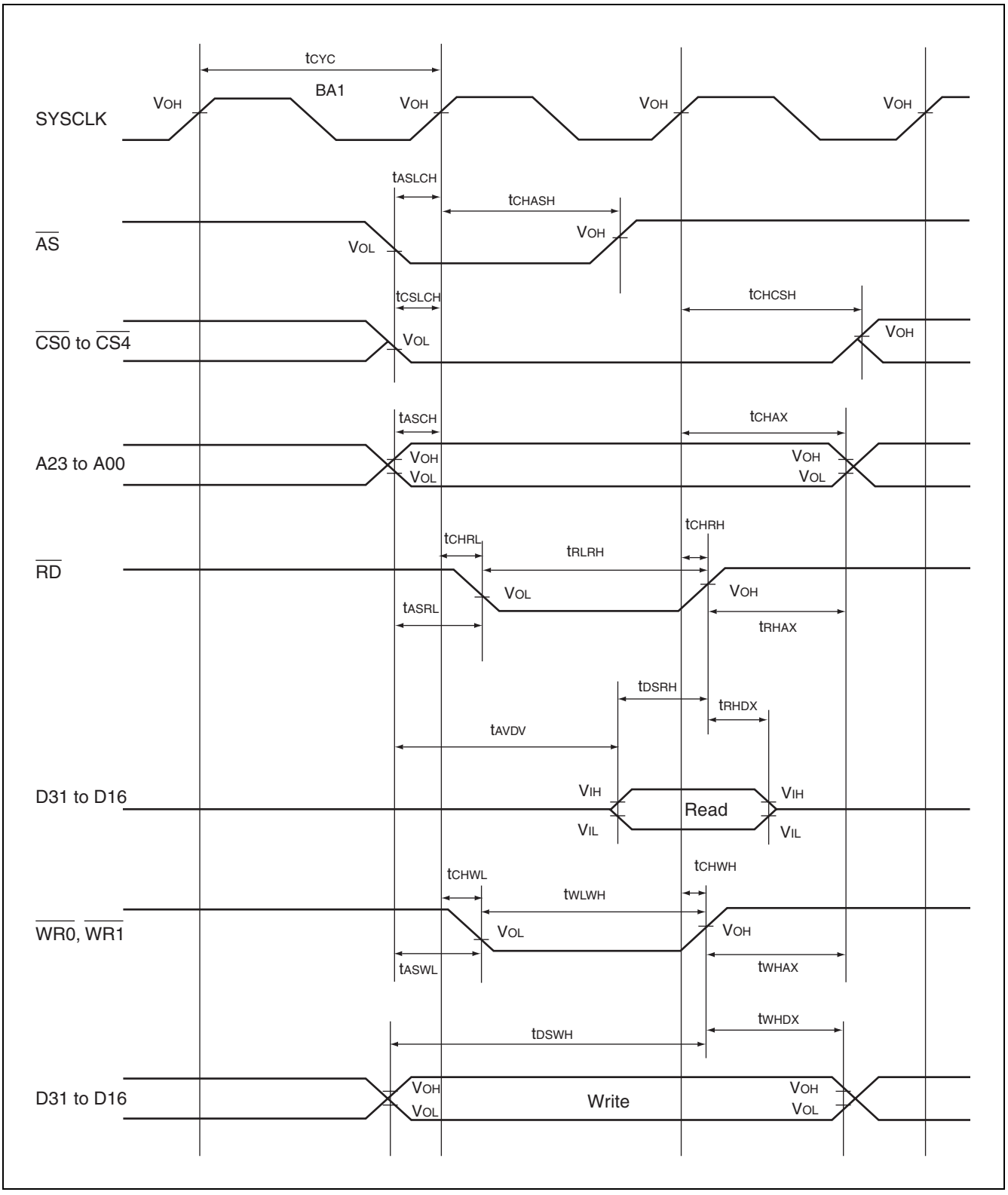


(4) Normal bus access read/write operation

($V_{CC}3$ = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, T_A = –40 °C to + 85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
$\overline{CS0}$ to $\overline{CS4}$ setup	t_{CSLCH}	SYSCLK $\overline{CS0}$ to $\overline{CS4}$	—	3	—	ns	
	t_{CSDLCH}			– 3	—	ns	
$\overline{CS0}$ to $\overline{CS4}$ hold	t_{CHCSH}			3	$t_{CYC}/2 + 6$	ns	
Address setup	t_{ASCH}	SYSCLK A23 to A00		3	—	ns	
	t_{ASWL}	$\overline{WR0}$, $\overline{WR1}$ A23 to A00		3	—	ns	
	t_{ASRL}	$\overline{RD}$ A23 to A00		3	—	ns	
Address hold	t_{CHAX}	SYSCLK A23 to A00		3	$t_{CYC}/2 + 6$	ns	
	t_{WHAX}	$\overline{WR0}$, $\overline{WR1}$ A23 to A00		3	—	ns	
	t_{RHAX}	$\overline{RD}$ A23 to A00		3	—	ns	
Valid address/valid data input time	t_{AVDV}	A23 to A00 D31 to D16		—	$3/2 \times t_{CYC} - 15$	ns	*
$\overline{WR0}$, $\overline{WR1}$ delay time	t_{CHWL}	SYSCLK $\overline{WR0}$, $\overline{WR1}$		—	6	ns	
	t_{CHWH}			—	6	ns	
Data setup time ($\overline{WRn}$ rising)	t_{DSWH}	D31 to D16 $\overline{WR0}$, $\overline{WR1}$		$t_{CYC} - 3$	—	ns	
Data hold time ($\overline{WRn}$ rising)	t_{WHDX}	D31 to D16 $\overline{WR0}$, $\overline{WR1}$		3	—	ns	
$\overline{WR0}$, $\overline{WR1}$ minimum pulse width	t_{WLWH}	$\overline{WR0}$, $\overline{WR1}$		$t_{CYC} - 3$	—	ns	
$\overline{RD}$ delay time	t_{CHRL}	SYSCLK $\overline{RD}$		—	6	ns	
	t_{CHRH}			—	6	ns	
Data setup time ($\overline{RD}$ rising)	t_{DSRH}	D31 to D16 $\overline{RD}$		20	—	ns	
Data hold time ($\overline{RD}$ rising)	t_{RHDX}	D31 to D16 $\overline{RD}$		0	—	ns	
$\overline{RD}$ minimum pulse width	t_{RLRH}	$\overline{RD}$		$t_{CYC} - 3$	—	ns	
$\overline{AS}$ setup	t_{ASLCH}	SYSCLK $\overline{AS}$		3	—	ns	
$\overline{AS}$ hold	t_{CHASH}			3	$t_{CYC}/2 + 6$	ns	

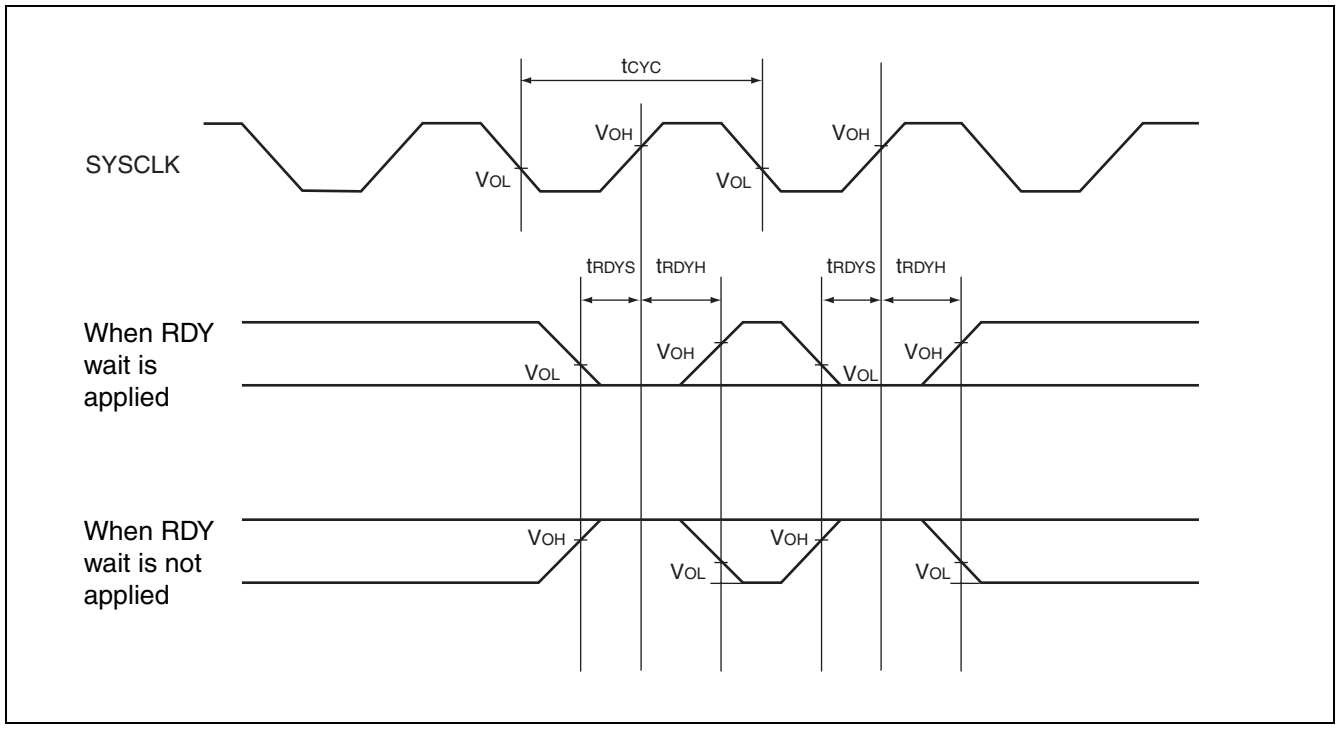
* : When the bus timing is delayed by automatic wait insertion or RDY input, add the time (t_{CYC} × the number of cycles added for the delay) to this rating.


tCYC
BA1
SYSCLK
VOH
VOH
VOH
VOH
tASLCH
tCHASH
AS
VOL
VOH
tCSLCH
tCHCSH
CS0 to CS4
VOL
VOH
tASCH
tCHAX
A23 to A00
VOH
VOL
VOH
VOL
tCHRH
tCHRL
tRLRH
RD
VOL
VOH
tASRL
tRHAX
tDSRH
tRHDX
tAVDV
D31 to D16
VIH
VIH
Read
VIL
VIL
tCHWH
tCHWL
tWLWH
WR0, WR1
VOL
VOH
tASWL
tWHAX
tWHDX
tDSWH
D31 to D16
VOH
VOL
Write
VOH
VOL

(5) Ready input timing

($V_{CC}3$ = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, T_A = –40 °C to + 85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
RDY setup time → SYSCLK ↓	t_{RDYS}	SYSCLK RDY	—	10	—	ns
SYSCLK ↑ → RDY hold time	t_{RDYH}	SYSCLK RDY		0	—	ns

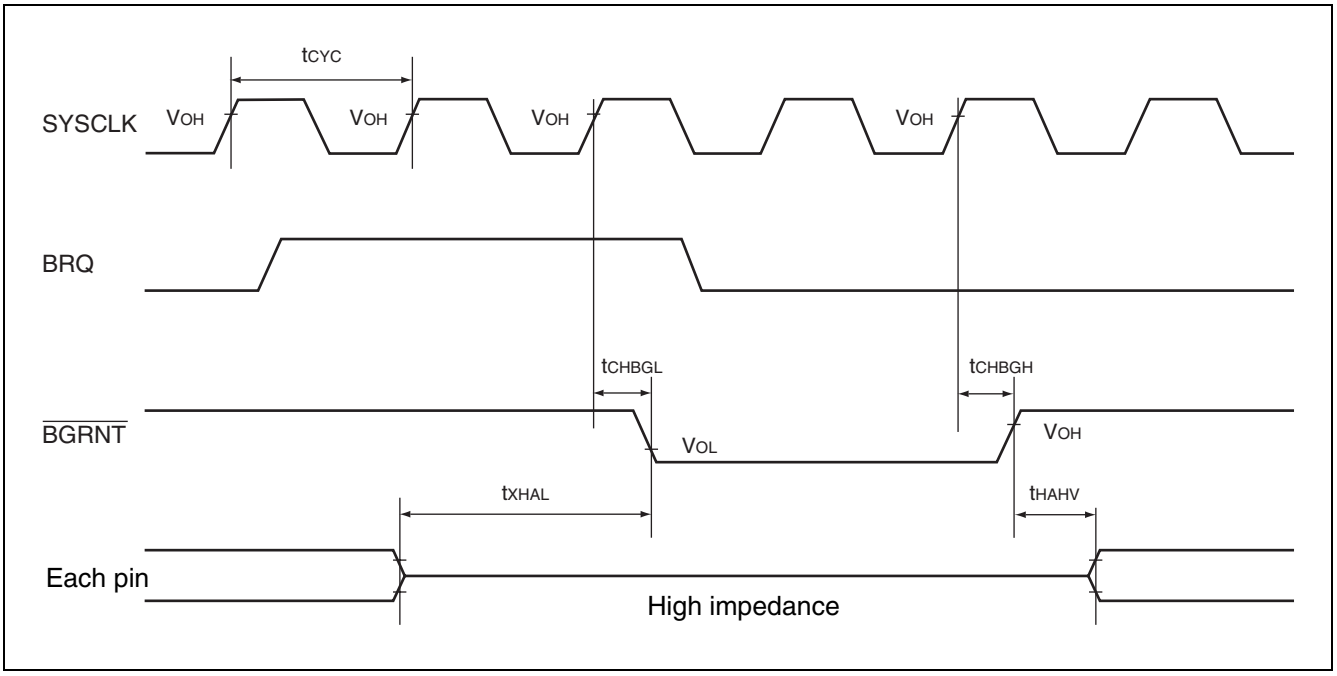


(6) Hold timing

($V_{CC}3$ = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, T_A = –40 °C to + 85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
$\overline{BGRNT}$ delay time	t_{CHBGL}	SYSCLK $\overline{BGRNT}$	—	—	10	ns
	t_{CHBGH}			—	10	ns
$\overline{BGRNT}$ rising from pin floating	t_{XHAL}	—		t_{CYC} – 10	t_{CYC} + 10	ns
$\overline{BGRNT}$ rising from pin valid	t_{HAHV}	$\overline{BGRNT}$		t_{CYC} – 10	t_{CYC} + 10	ns

Note : After a BRQ is captured, a minimum of 1 cycle is required before $\overline{BGRNT}$ changes.



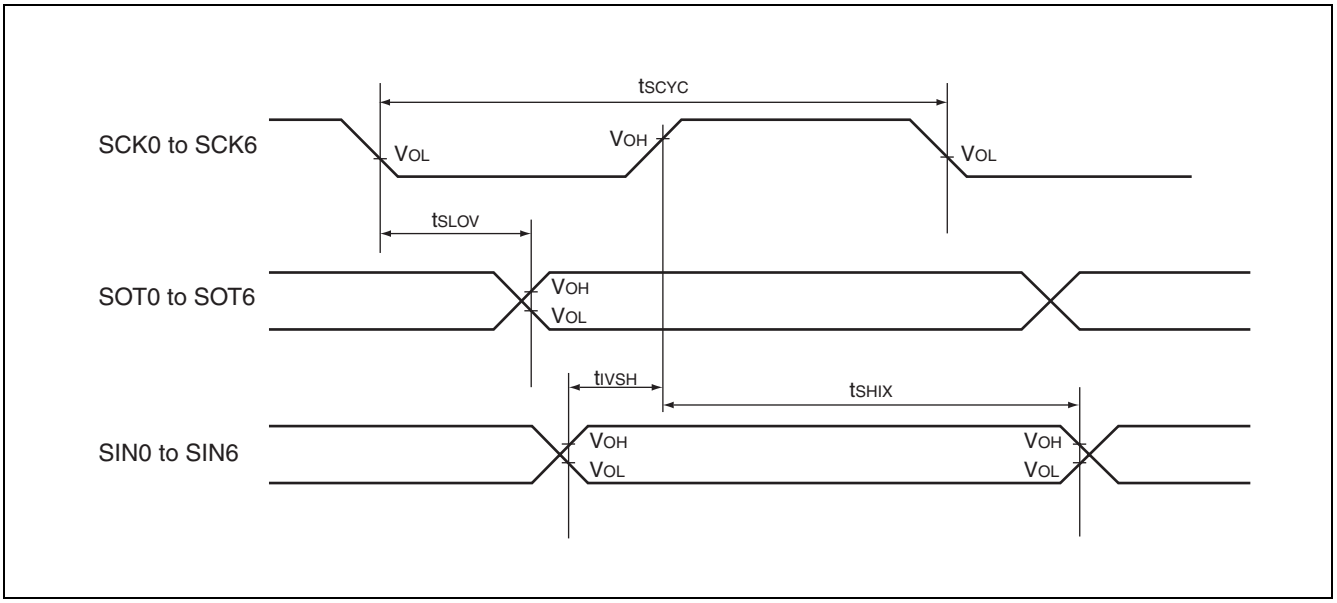
(7) LIN-UART timing

($V_{CC}5$ = 4.5 V to 5.5 V, $V_{CC}3$ = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, T_A = –40 °C to + 85 °C)

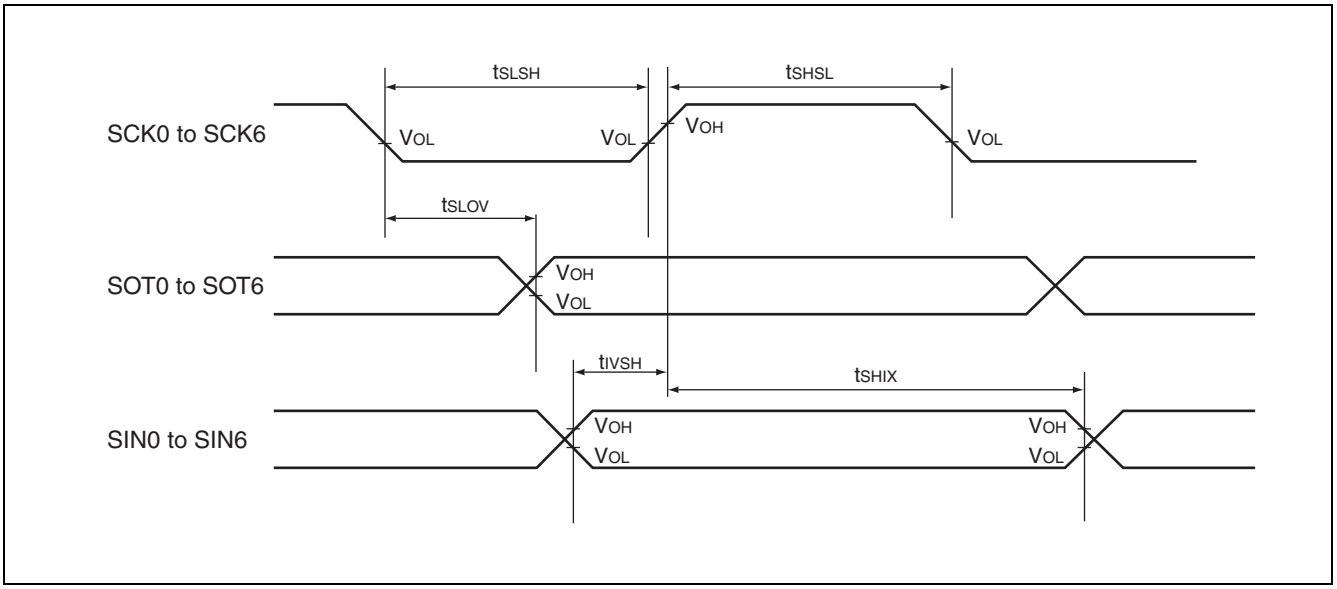
Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0 to SCK6	Internal shift clock mode	$5t_{CYCP}$	—	ns
SCK ↓ → SOT delay time	t_{SLOV}	SCK0 to SCK6, SOT0 to SOT6		– 50	+ 50	ns
Valid SIN → SCK ↑	t_{IVSH}	SCK0 to SCK6, SIN0 to SIN6		t_{CYCP} + 80	—	ns
SCK ↑ → valid SIN hold time	t_{SHIX}	SCK0 to SCK6, SIN0 to SIN6		0	—	ns
Serial clock ”H” pulse width	t_{SHSL}	SCK0 to SCK6	External shift clock mode	t_{CYCP} + 10	—	ns
Serial clock ”L” pulse width	t_{SLSH}	SCK0 to SCK6		$3t_{CYCP}$	—	ns
SCK ↓ → SOT delay time	t_{SLOV}	SCK0 to SCK6, SOT0 to SOT6		—	150	ns
Valid SIN → SCK ↑	t_{IVSH}	SCK0 to SCK6, SIN0 to SIN6		30	—	ns
SCK ↑ → valid SIN hold time	t_{SHIX}	SCK0 to SCK6, SIN0 to SIN6		t_{CYCP} + 30	—	ns
SCK rising time	t_F	SCK0 to SCK6		—	10	ns
SCK falling time	t_R	SCK0 to SCK6		—	10	ns

Notes : • Above values are AC characteristics for CLK synchronous mode.
• t_{CYCP} is the cycle time of the peripheral clock.

• Internal shift clock mode



• External shift clock mode

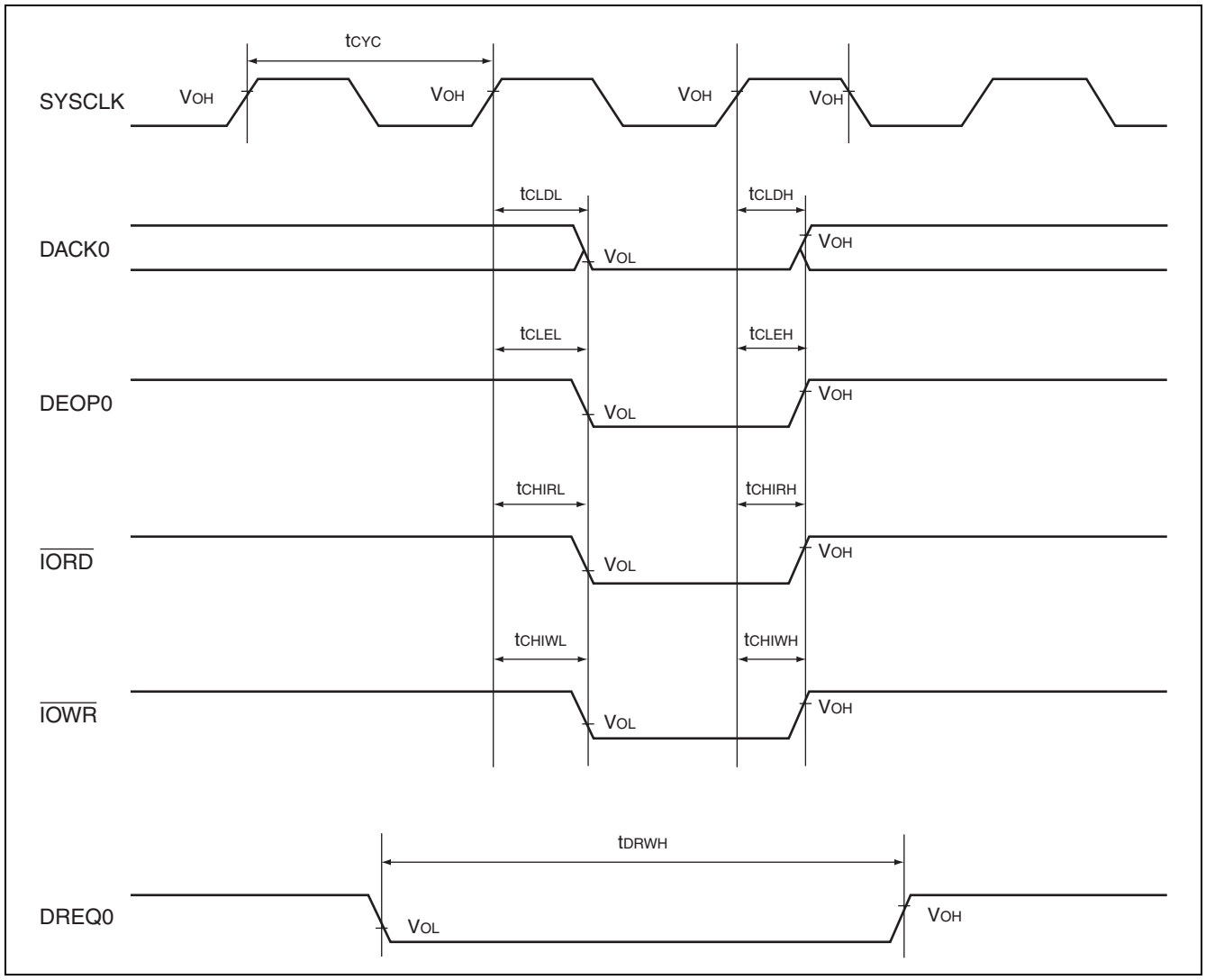


(8) DMA controller timing

($V_{CC}3$ = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, T_A = –40 °C to + 85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
DREQ0 input pulse	t_{DRWH}	DREQ0	—	—	10	ns
DACK0 delay time	t_{CLDL}	DACK0		—	10	ns
	t_{CLDH}			—	10	ns
DEOP0 delay time	t_{CLEL}	DEOP0		—	10	ns
	t_{CLEH}			—	10	ns
$\overline{IORD}$ delay time	t_{CHIRL}	$\overline{IORD}$		—	10	ns
	t_{CHIRH}			—	10	ns
$\overline{IOWR}$ delay time	t_{CHIWL}	$\overline{IOWR}$		—	10	ns
	t_{CHIWH}			—	10	ns

Note : After a BREQ is captured, a minimum of 1 cycle is required before $\overline{BGRNT}$ changes.

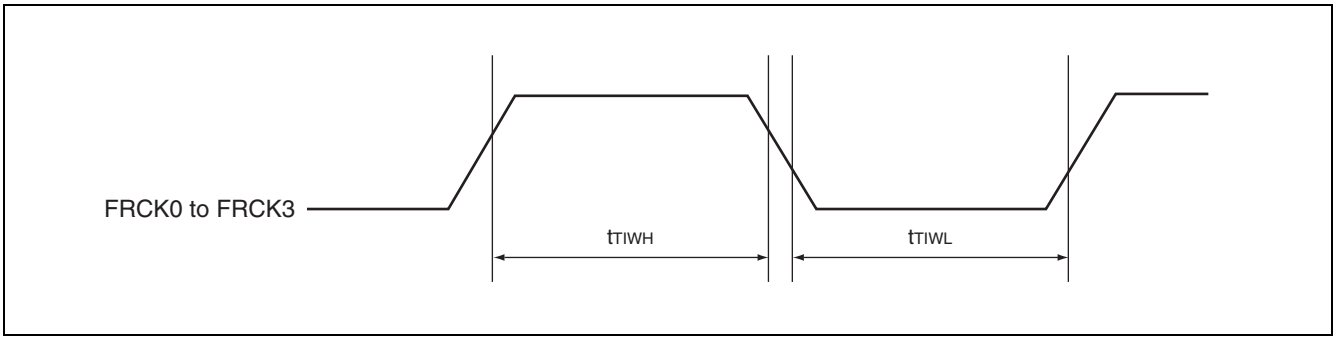


(9) Free-run timer clock

($V_{CC}5$ = 4.0 V to 5.5 V, $V_{CC}3$ = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, T_A = –40 °C to + 85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Input pulse width	t_{TIWH} t_{TIWL}	FRCK0 to FRCK3	—	$4t_{CYCP}$	—	ns

Note : t_{CYCP} is the cycle time of the peripheral clock.

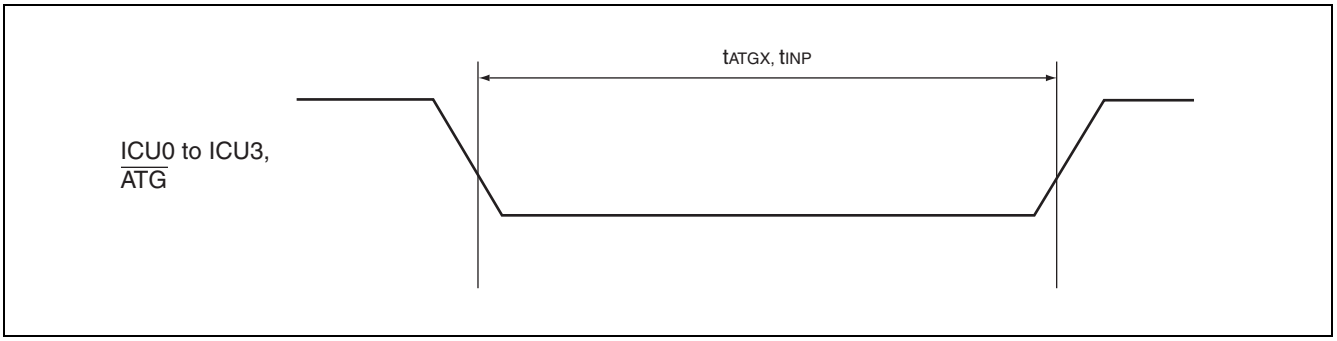


(10) Trigger input timing

($V_{CC}5$ = 4.0 V to 5.5 V, $V_{CC}3$ = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, T_A = –40 °C to + 85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Input capture input trigger	t_{INP}	ICU0 to ICU3	—	$5t_{CYCP}$	—	ns
A/D converter trigger	t_{ATGX}	$\overline{ATG}$	—	$5t_{CYCP}$	—	ns

Note : t_{CYCP} is the cycle time of the peripheral clock.



5. A/D converter

(1) Electrical characteristics

($V_{CC}3$ = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, T_A = –40 °C to + 85 °C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error*1	—	—	—	—	± 3	LSB	At $AV_{CC}3$ = 3.3 V, AVRH = 3.3 V
Linearity error*1	—	—	—	—	± 2.5	LSB	
Differential linearity error*1	—	—	—	—	± 1.9	LSB	
Zero transition voltage*1	V_{OT}	AN0 to AN12	AVRL–1.5	AVRL–0.5	AVRL–2.5	LSB	
Full transition voltage*1	V_{FST}	AN0 to AN12	AVRH–3.5	AVRH–1.5	AVRH–0.5	LSB	
Conversion time	—	—	1 *2	—	—	µs	
Analog port input current	I_{AIN}	AN0 to AN12	—	—	10	µA	
Analog input voltage	V_{AIN}	AN0 to AN12	AV_{SS}	—	AVRH	V	
Reference voltage	—	AVRH	AV_{SS}	—	$AV_{CC}3$	V	
Analog power supply current (analog + digital)	I_A	AVCC3	—	1.5	2.5	mA	Including reference supply
	I_{AH}*3		—	—	10	µA	
Analog input equivalent capacity	Cin	AN0 to AN12	—	—	14.7	pF	
Analog input equivalent resistance	Rin	AN0 to AN12	—	—	1.9	kΩ	$AV_{CC}3 \geq 2.7$ V
Output impedance of analog signal source	Rext	—	—	—	1.9	kΩ	$AV_{CC}3 \geq 2.7$ V

*1 : Measured in the CPU sleep state

*2 : Set the peripheral clock and conversion time setting register to set a time equal to or longer than this time.

*3 : The current when A/D converter is not operating, or in the CPU stop mode (at $V_{CC}3$ = $AV_{CC}3$ = AVRH = 3.3 V).

(2) Cautions Relating to the A/D Converter

The diagram below shows the equivalent circuit of the sampling circuit in the A/D converter.

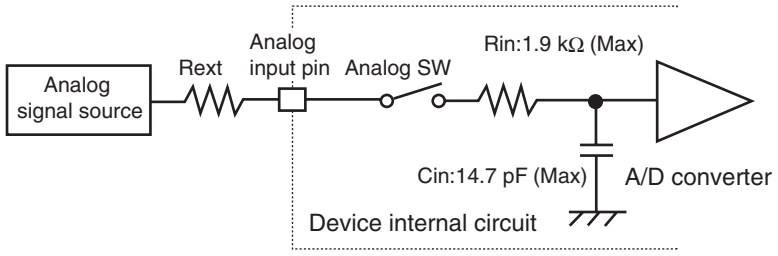
The output impedance of the external circuit connected to the analog input must satisfy the following criteria.

- The recommended output impedance for the external circuit is 1.9 kΩ or less.
- If an external capacitor is used, remember to consider the capacitive voltage divider effect due to the external capacitor and the internal capacitor in the chip. Accordingly, an external capacitance several thousand times that of the internal capacitance is recommended.
- The analog voltage sampling period may be too short if the output impedance of the external circuit is high. In this case, select Rext and Tsamp such that they satisfy the following condition.

$$Rext = Tsamp / (7 \times Cin) - Rin$$

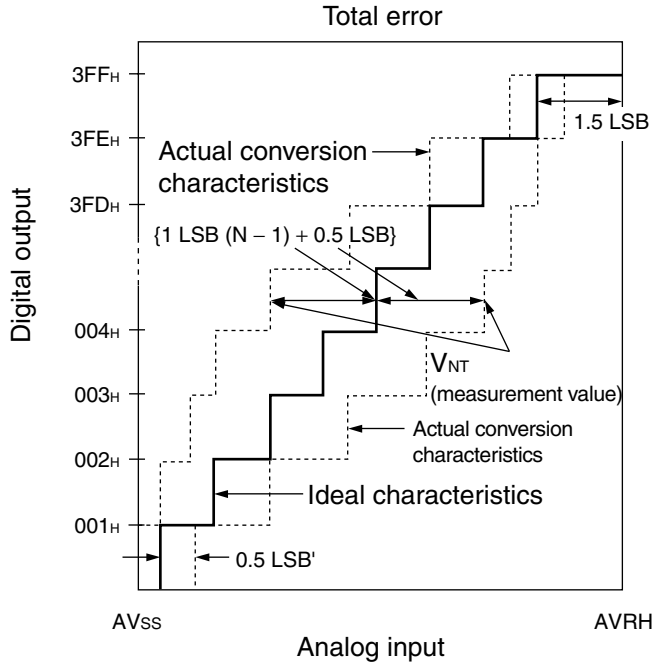
Rext	: Output impedance of the analog signal source
Tsamp	: Sampling time
Cin	: Equivalent capacitance of analog input
Rin	: Equivalent resistance of analog input

- Input impedance



(3) Definition of A/D converter terms

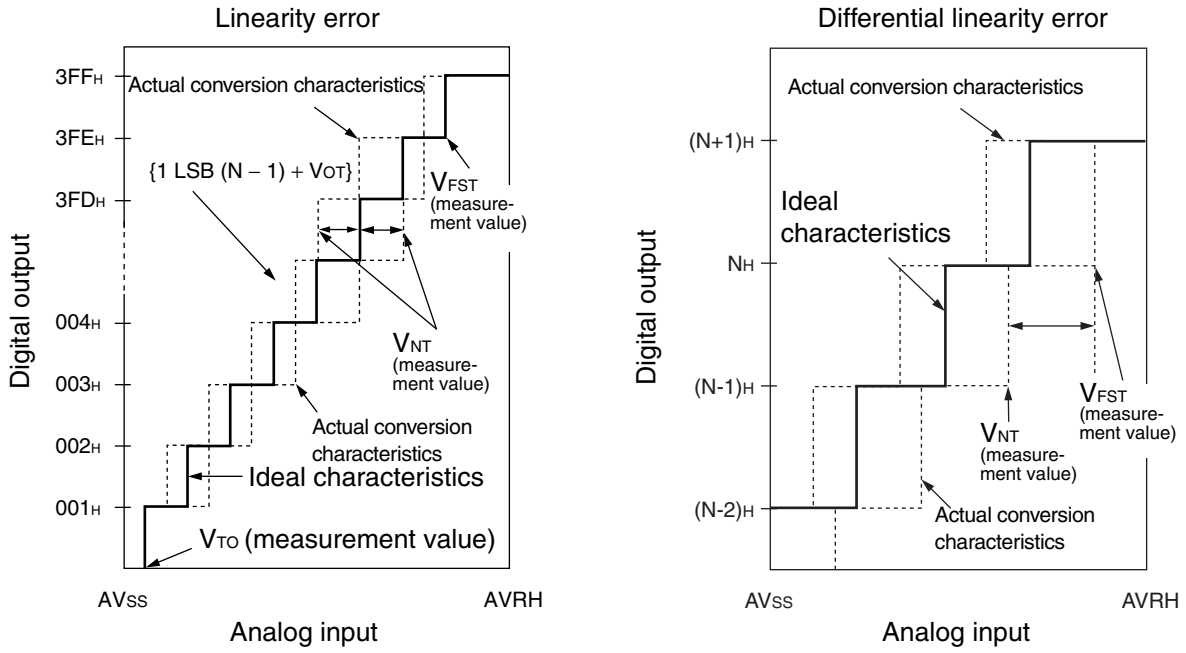
- Resolution
  Analog variation that is recognizable by an A/D converter.
- Linearity error
  Deviation between actual conversion characteristics and a straight line connecting zero transition point (00 0000 0000 ↔ 00 0000 0001) and full scale transition point (11 1111 1110 ↔ 11 1111 1111).
- Differential linearity error
  Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.
- Total error
  This error indicates the difference between actual and theoretical values, including the zero transition error/ full scale transition error/linearity error.



$$1LSB' \text{ (ideal value)} = \frac{AVRH - AV_{SS}}{1024} \text{ [V]}$$

$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ LSB' \times (N - 1) + 0.5\ LSB'\}}{1\ LSB'}$$

N : A/D converter digital output value
V_{OT}' (ideal value) = AV_{SS} + 0.5 LSB' [V]
V_{FST}' (ideal value) = AV – 1.5 LSB' [V]
V_{NT} : A voltage at which digital output transits from $(N + 1)_H$ to N_H



$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{OT}\}}{1LSB} \text{ [LSB]}$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} \text{ [LSB]}$$

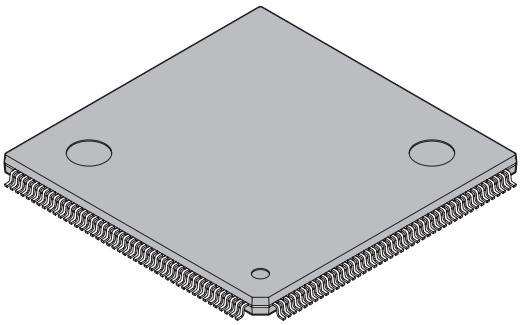
$$1LSB = \frac{V_{FST} - V_{OT}}{1022} \text{ [V]}$$

N : A/D converter digital output value
V_{OT} : A voltage at which digital output transits from 000_H to 001_H.
V_{FST} : A voltage at which digital output transits from $3FE_H$ to $3FF_H$.

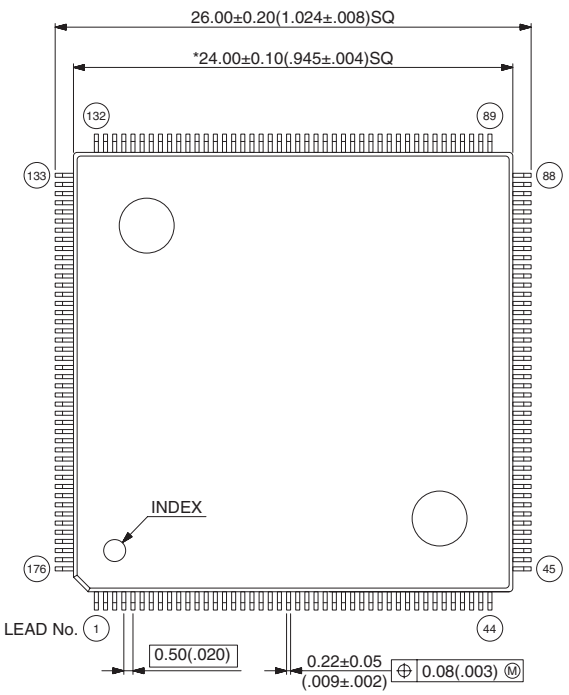
■ ORDERING INFORMATION

Part number	Package	Remarks
MB91461PMC-GSE1	176-pin, plastic LQFP (FPT-176P-M07)	Lead-free package

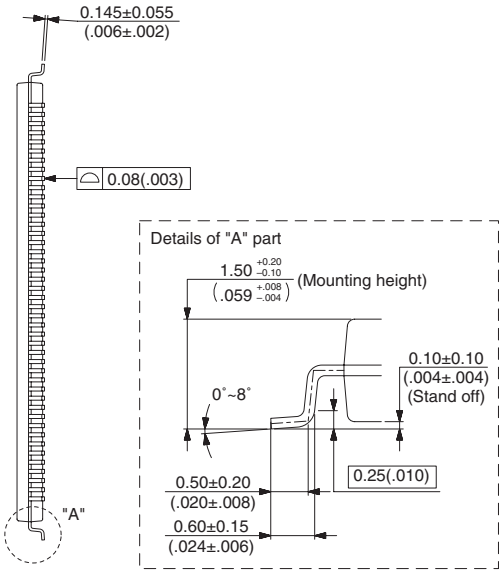
■ PACKAGE DIMENSION

176-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	24.0 × 24.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Code (Reference)	P-LQFP-0176-2424-0.50
(FPT-176P-M07)		

176-pin plastic LQFP
(FPT-176P-M07)



Note 1) * : Values do not include resin protrusion.
Resin protrusion is +0.25(.010)Max(each side).
Note 2) Pins width and pins thickness include plating thickness
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/fj/DATASHEET/ef-ovpklv.html

The information for microcontroller supports is shown in the following homepage.
http://www.fujitsu.com/global/services/microelectronics/product/micom/support/index.html

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