STD4LNK60Z
STF4LNK60Z

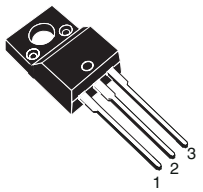
N-channel 600 V, 2.2 Ω, 3.3 A, TO-220FP, DPAK Zener-protected SuperMESH™ Power MOSFET

Preliminary Data

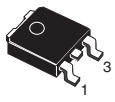
Features

Type	V_{DSS}	$R_{DS(on)}$ max	I_D	Pw
STD4LNK60Z	600 V	< 2.7 Ω	3.3 A	70 W
STF4LNK60Z	600 V	< 2.7 Ω	3.3 A	25 W

- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitances
- Improved ESD capability



TO-220FP



DPAK

Application

- Switching applications

Description

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST's full range of high voltage Power MOSFETs including revolutionary MDmesh™ products.

Figure 1. Internal schematic diagram

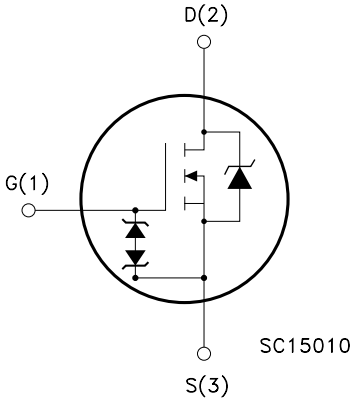


Table 1. Device summary

Order codes	Marking	Package	Packaging
STD4LNK60Z	4LNK60Z	DPAK	Tape and reel
STF4LNK60Z	4LNK60Z	TO-220FP	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220FP	DPAK	
V_{DS}	Drain-source voltage (V_{GS} = 0)	600		V
V_{GS}	Gate-source voltage	± 30		V
I_D	Drain current (continuous) at T_C = 25 °C	3.3 (1)	3.3	A
I_D	Drain current (continuous) at T_C = 100 °C	2 (1)	2	A
I_{DM}	Drain current (pulsed)	13.2(1)	13.2	A
P_{TOT}	Total dissipation at T_C = 25 °C	25	70	W
	Derating factor	0.2	0.56	W/°C
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s;T_C=25 °C)	2500	--	V
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 150		°C

1. Limited by package

Table 3. Thermal data

Symbol	Parameter	Value		Unit
		TO-220FP	DPAK	
$R_{thj\text{-}case}$	Thermal resistance junction-case	5	1.79	°C/W
$R_{thj\text{-}pcb}$	Thermal resistance junction-pcb(1)	--	50	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-amb	62.5	--	°C/W
T_l	Maximum lead temperature for soldering purpose	300		°C

1. Minimum footprint

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by Tjmax)	TBD	A
E_{AS}	Single pulse avalanche energy (1)	TBD	mJ

1. Starting Tj = 25 °C, I_D = I_{AR}, V_{DD} = 50 V

2 Electrical characteristics

(T_{CASE}=25 °C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS}= 0	600			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating, V_{DS} = Max rating,Tc=125 °C			1 50	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ± 30 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 50 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS}= 10 V, I_D= 2.7 A		2.2	2.7	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} =25 V, f=1 MHz, V_{GS}=0		400 50 10		pF pF pF
$C_{oss\ eq.}$	Equivalent output capacitance	V_{DS} = 0 to 480 V, V_{GS} =0		44.4		pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD}= 480 V, I_D = 3.3 A V_{GS} = 10 V *(see Figure 3)*		14 TBD TBD		nC nC nC

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	V_{DD}= 300 V, I_D= 3.3 A, R_G=4.7 Ω, V_{GS}=10 V *(see Figure 2)*		7.5 19.5		ns ns
$t_{d(off)}$ t_f	Turn-off delay time Fall time	V_{DD}=300 V, I_D= 3.3 A, R_G=4.7 Ω, V_{GS}= 10 V *(see Figure 2)*		28 24		ns ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}(1)	Source-drain current Source-drain current (pulsed)				3.3 13.2	A A
V_{SD}(2)	Forward on voltage	I_{SD}= 3.3 A, V_{GS}=0			TBD	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD}= 3.3 A, di/dt = 100 A/µs, V_{DD}=480 V, Tj=150°C *(see Figure 7)*		TBD TBD TBD		ns nC A

1. Pulse width limited by package
2. Pulsed: pulse duration = 300µs, duty cycle 1.5%

3 Test circuits

Figure 2. Switching times test circuit for resistive load

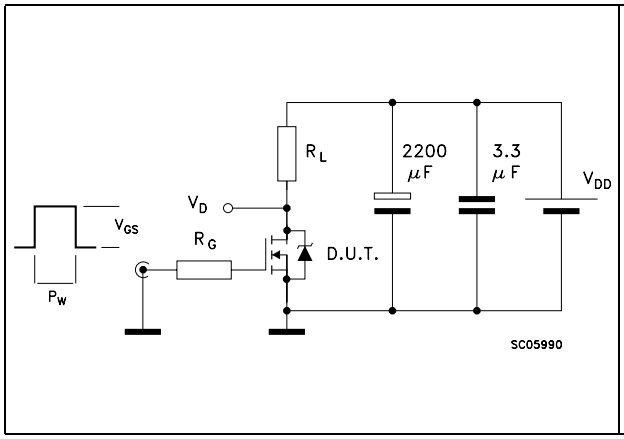


Figure 3. Gate charge test circuit

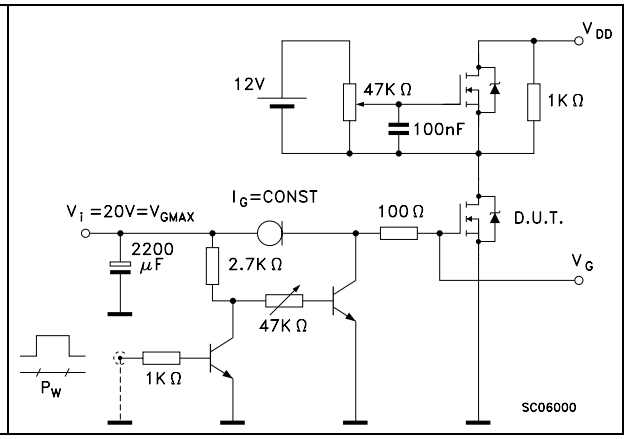


Figure 4. Test circuit for inductive load switching and diode recovery times

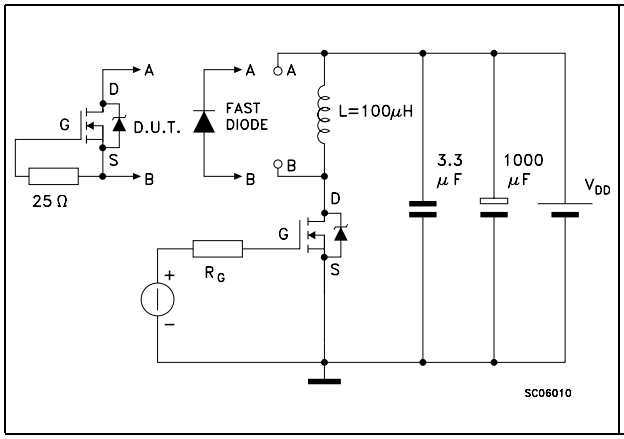


Figure 5. Unclamped inductive load test circuit

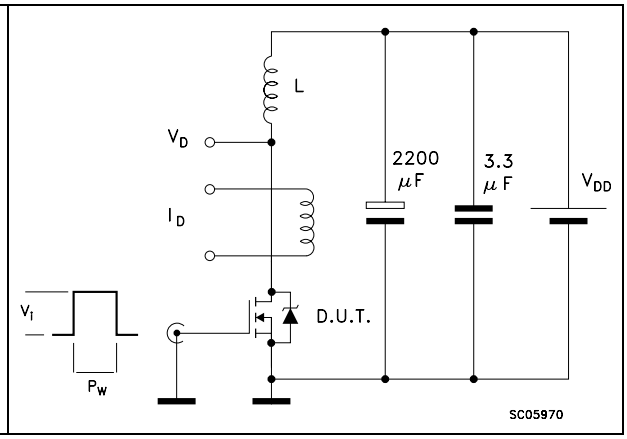


Figure 6. Unclamped inductive waveform

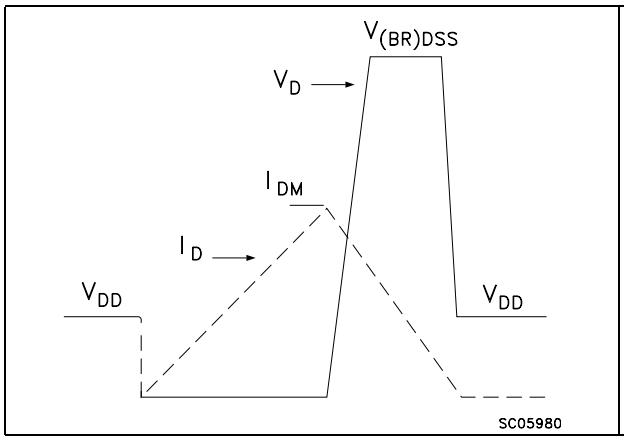
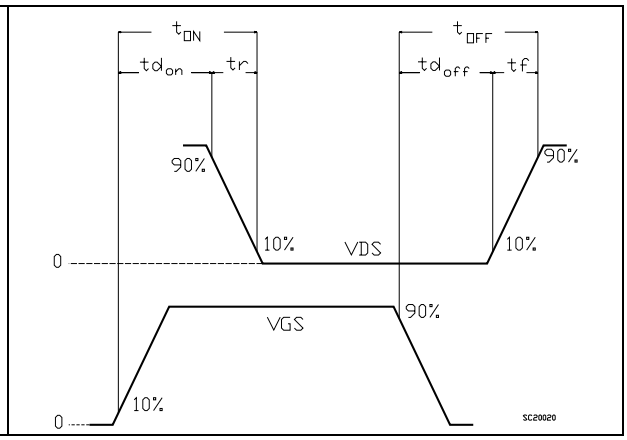


Figure 7. Switching time waveform

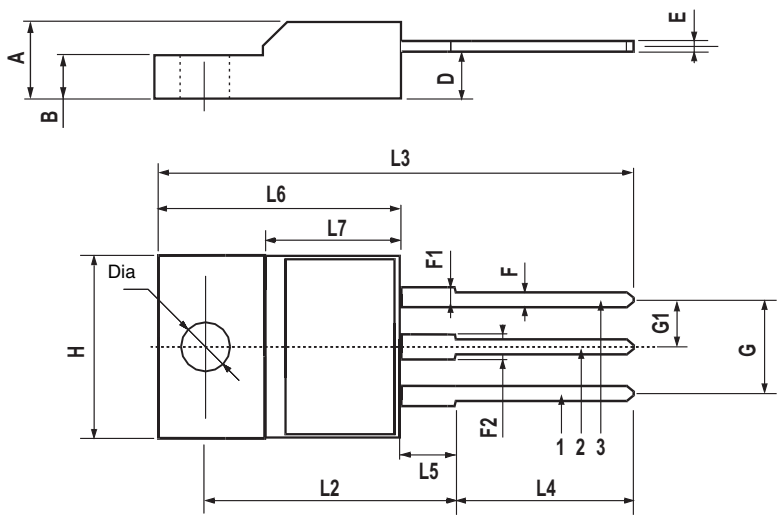


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*

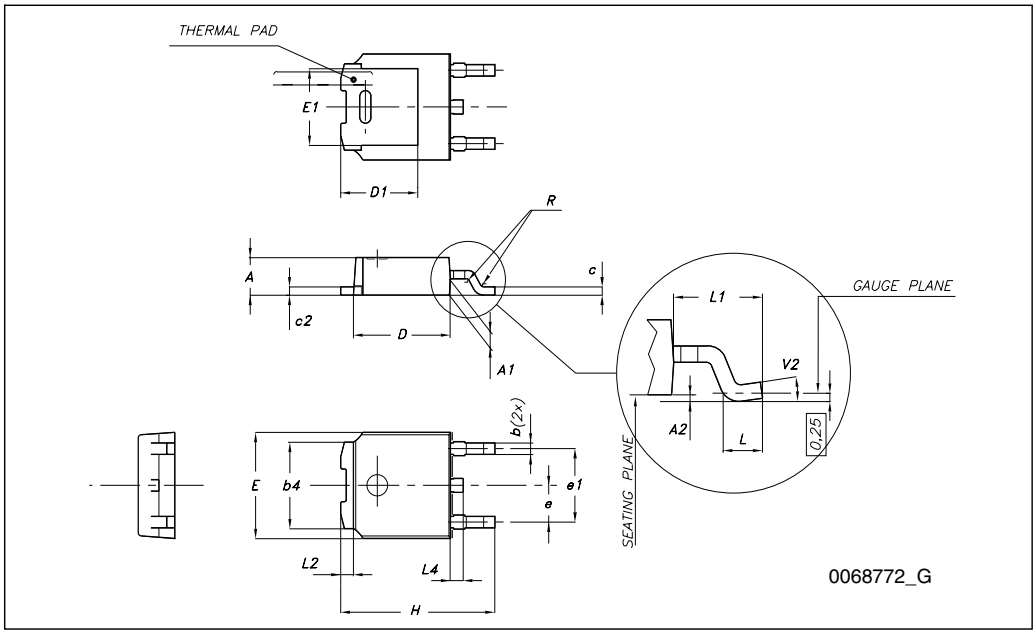
TO-220FP mechanical data

Dim.	mm.			inch		
	Min.	Typ	Max.	Min.	Typ.	Max.
A	4.40		4.60	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.70	0.017		0.027
F	0.75		1.00	0.030		0.039
F1	1.15		1.50	0.045		0.067
F2	1.15		1.50	0.045		0.067
G	4.95		5.20	0.195		0.204
G1	2.40		2.70	0.094		0.106
H	10		10.40	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.80		10.60	0.385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.90		16.40	0.626		0.645
L7	9		9.30	0.354		0.366
Dia	3		3.2	0.118		0.126



TO-252 (DPAK) mechanical data

DIM.	mm.		
	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0 °		8 °



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
24-Jul-2008	1	Initial release.

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