



# STB270N4F3 STI270N4F3 - STP270N4F3

N-channel 40 V - 2.1 mΩ - 160 A - TO-220 - D<sup>2</sup>PAK - I<sup>2</sup>PAK  
STripFET™ Power MOSFET

## Features

Type	V <sub>DSS</sub>	R <sub>DS(on) max</sub>	I <sub>D</sub>	P <sub>TOT</sub>
STB270N4F3	40 V	< 2.5 mΩ	160 A	330 W
STI270N4F3	40 V	< 2.9 mΩ	120 A	330 W
STP270N4F3	40 V	< 2.9 mΩ	120 A	330 W

- 100% avalanche tested
- Standard threshold drive

## Applications

- High current, switching application
- Automotive

## Description

This n-channel enhancement mode Power MOSFET is the latest refinement of STMicroelectronics unique “single feature size” strip-based process with less critical alignment steps and therefore a remarkable manufacturing reproducibility. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and low gate charge.

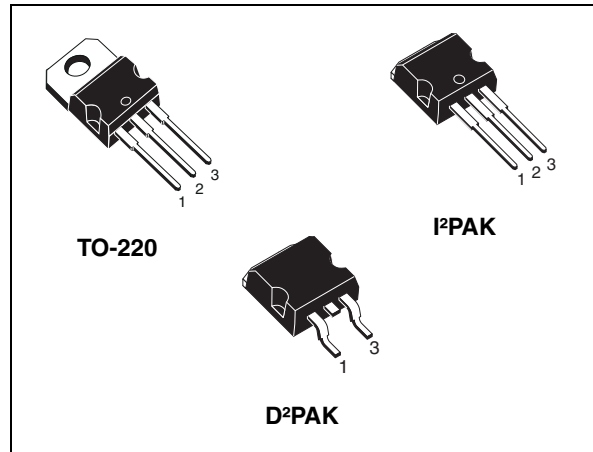


Figure 1. Internal schematic diagram

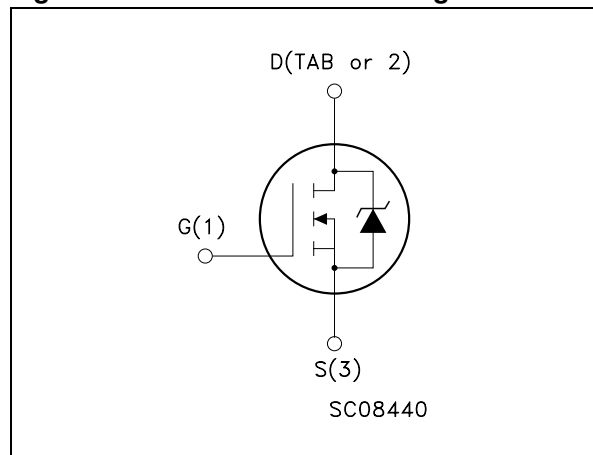


Table 1. Device summary

Order codes	Marking	Package	Packaging
STB270N4F3	270N4F3	D <sup>2</sup> PAK	Tape and reel
STI270N4F3	270N4F3	I <sup>2</sup> PAK	Tube
STP270N4F3	270N4F3	TO-220	Tube

## Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value		Unit
		TO-220/I <sup>2</sup> PAK	D <sup>2</sup> PAK	
V <sub>DS</sub>	Drain-source voltage (V <sub>GS</sub> = 0)	40		V
V <sub>GS</sub>	Gate-source voltage	± 20		V
I <sub>D</sub> <sup>(1)</sup>	Drain current (continuous) at T <sub>C</sub> = 25 °C	120	160	A
I <sub>D</sub> <sup>(1)</sup>	Drain current (continuous) at T <sub>C</sub> =100 °C	120	160	A
I <sub>DM</sub> <sup>(2)</sup>	Drain current (pulsed)	480	640	A
P <sub>TOT</sub>	Total dissipation at T <sub>C</sub> = 25 °C	330		W
	Derating factor	2.2		W/°C
dv/dt <sup>(3)</sup>	Peak diode recovery voltage slope	3.5		V/n
E <sub>AS</sub> <sup>(4)</sup>	Single pulse avalanche energy	1		J
T <sub>J</sub> T <sub>stg</sub>	Operating junction temperature Storage temperature	-55 to 175		°C

1. Current limited by package
2. Pulse width limited by safe operating area
3. I<sub>SD</sub> ≤ 120A, di/dt ≤ 200A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>j</sub> ≤ T<sub>JMAX</sub>
4. Starting T<sub>j</sub>=25°C, I<sub>D</sub> =80A, V<sub>DD</sub>= 32V

**Table 3. Thermal data**

Symbol	Parameter	Value		Unit
		TO-220/I <sup>2</sup> PAK	D <sup>2</sup> PAK	
R <sub>thj-case</sub>	Thermal resistance junction-case max	0.45		°C/W
R <sub>thj-pcb</sub> <sup>(1)</sup>	Thermal resistance junction-pcb max	--	35	°C/W
R <sub>thj-a</sub>	Thermal resistance junction-ambient max	62.5	--	°C/W
T <sub>I</sub>	Maximum lead temperature for soldering purpose (for 10 sec, 1.6 mm from case)	300	--	°C

1. When mounted on 1inch<sup>2</sup> FR-4 board, 2 oz Cu.

## 2 Electrical characteristics

( $T_{CASE}=25\text{ °C}$  unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\ \mu\text{A}$ , $V_{GS} = 0$	40			V	
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max rating}$ , $V_{DS} = \text{Max rating}$ @125 °C			10	$\mu\text{A}$	
					100	$\mu\text{A}$	
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20\ \text{V}$			$\pm 200$	nA	
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\ \mu\text{A}$	2		4	V	
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\ \text{V}$ , $I_D = 80\ \text{A}$	<b>TO-220</b>		2.5	2.9	m $\Omega$
			<b>I<sup>2</sup>PAK</b>				
			<b>D<sup>2</sup>PAK</b>		2.1	2.5	m $\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15\ \text{V}$ , $I_D = 80\ \text{A}$		200		S
$C_{iss}$	Input capacitance	$V_{DS} = 25\ \text{V}$ , $f = 1\ \text{MHz}$ , $V_{GS} = 0$		7400		pF
$C_{oss}$	Output capacitance			1800		pF
$C_{rss}$	Reverse transfer capacitance			47		pF
$Q_g$	Total gate charge	$V_{DD} = 20\ \text{V}$ , $I_D = 160\ \text{A}$		110	150	nC
$Q_{gs}$	Gate-source charge	$V_{GS} = 10\ \text{V}$		27		nC
$Q_{gd}$	gate-drain charge	(see Figure 14)		25		nC

1. Pulsed: pulse duration=300 $\mu\text{s}$ , duty cycle 1.5%

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ $t_r$	Turn-on delay time Rise time	$V_{DD}=20\text{ V}$ , $I_D=80\text{ A}$ , $R_G=4.7\ \Omega$ , $V_{GS}=10\text{ V}$ (see Figure 16)		22 180		ns ns
$t_{d(off)}$ $t_f$	Turn-off delay time Fall time	$V_{DD}=20\text{ V}$ , $I_D=80\text{ A}$ , $R_G=4.7\ \Omega$ , $V_{GS}=10\text{ V}$ (see Figure 16)		110 45		ns ns

**Table 7. Source drain diode**

Symbol	Parameter		Test conditions	Min	Typ.	Max	Unit
$I_{SD}$	Source-drain current	D <sup>2</sup> PAK				160	A
		TO-220				120	A
		I <sup>2</sup> PAK					
$I_{SDM}^{(1)}$	Source-drain current (pulsed)	D <sup>2</sup> PAK				640	A
		TO-220				480	A
		I <sup>2</sup> PAK					
$V_{SD}^{(2)}$	Forward on voltage		$I_{SD}=80\text{ A}$ , $V_{GS}=0$			1.5	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse recovery time Reverse recovery charge Reverse recovery current		$I_{SD}=160\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD}=32\text{ V}$ , $T_j=150\text{ }^\circ\text{C}$ (see Figure 15)		70 225 3.2		ns nC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

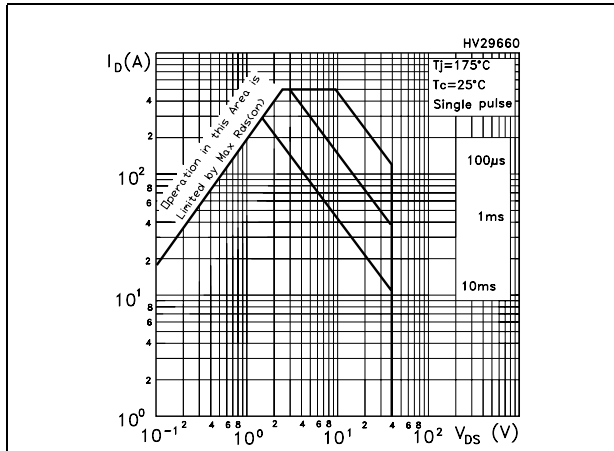


Figure 3. Thermal impedance

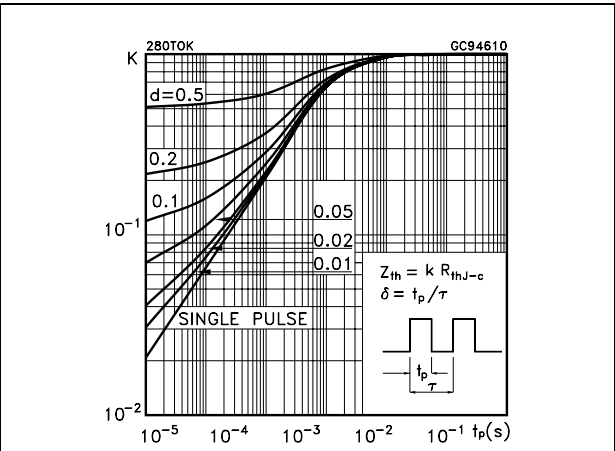


Figure 4. Output characteristics

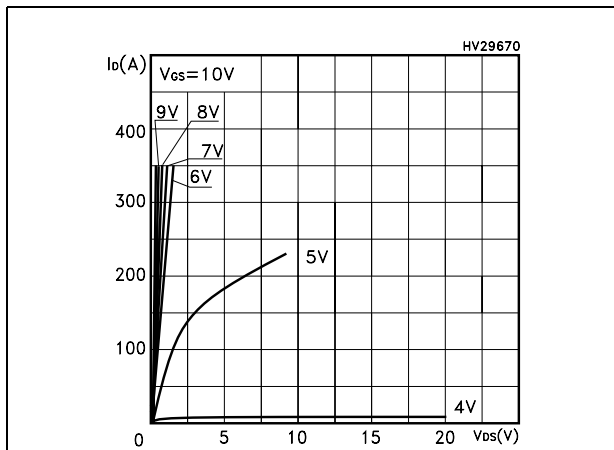


Figure 5. Transfer characteristics

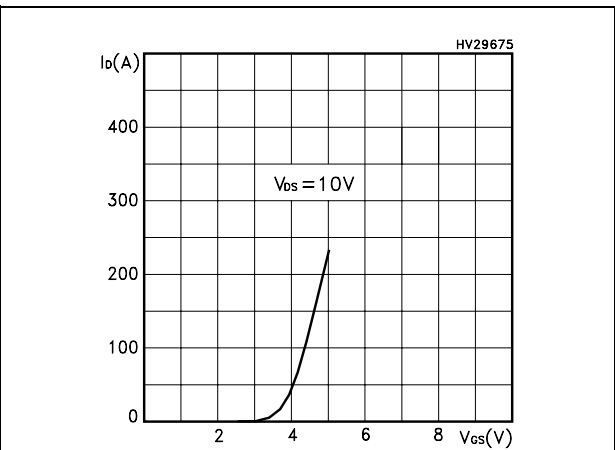


Figure 6. Static drain-source on resistance

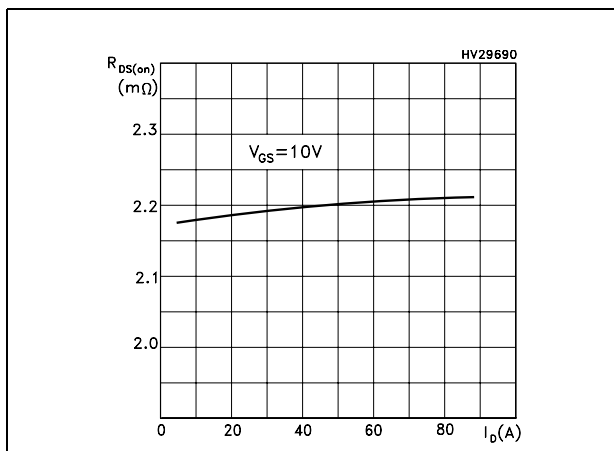


Figure 7. Normalized  $B_{V_{DS}}$  vs temperature

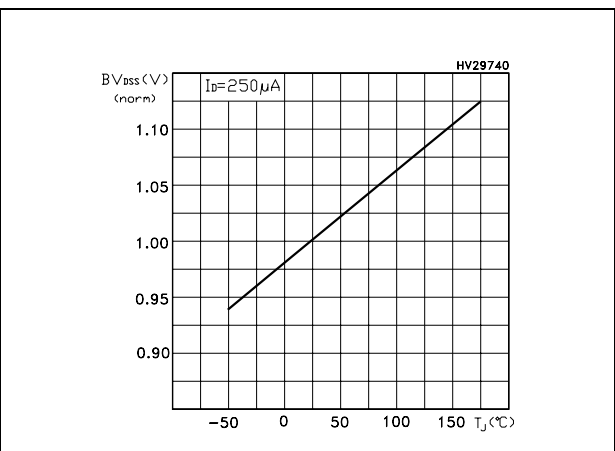


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

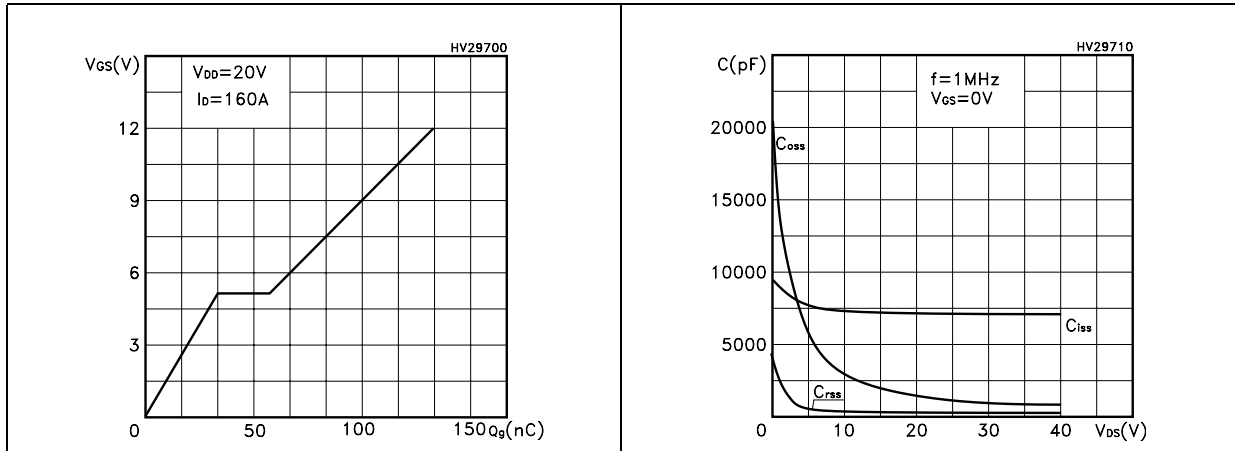


Figure 10. Normalized gate threshold voltage vs temperature

Figure 11. Normalized on resistance vs temperature

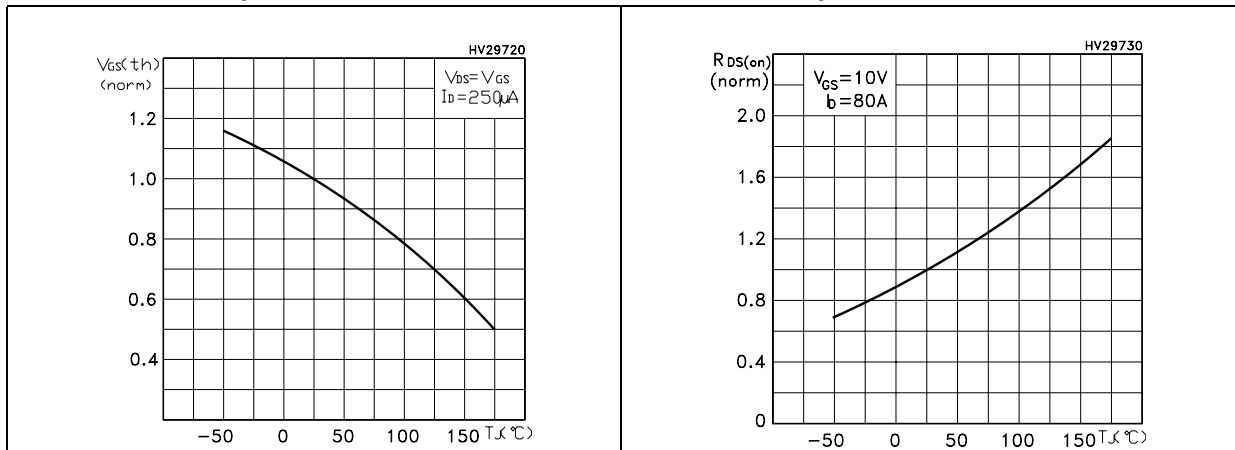
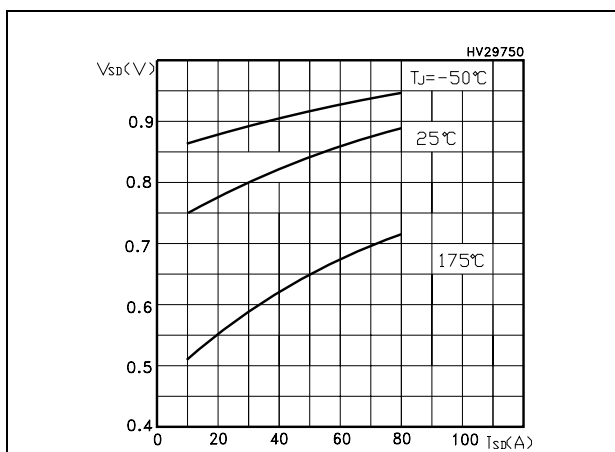


Figure 12. Source-drain diode forward characteristics



### 3 Test circuit

Figure 13. Switching times test circuit for resistive load

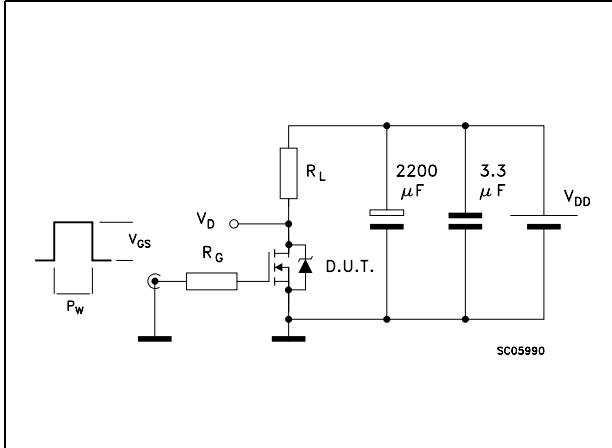


Figure 14. Gate charge test circuit



Figure 15. Test circuit for inductive load switching and diode recovery times

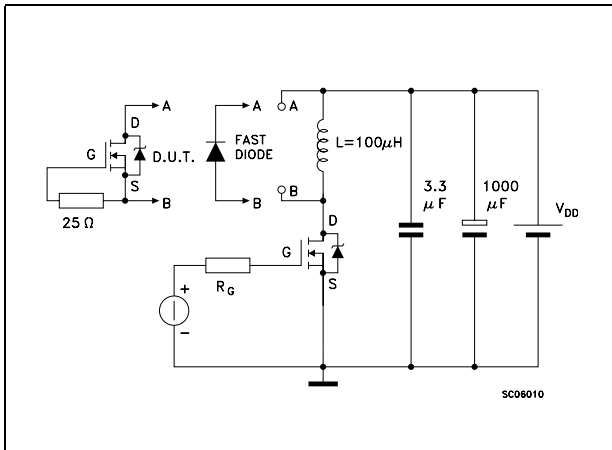


Figure 16. Unclamped Inductive load test circuit



Figure 17. Unclamped inductive waveform

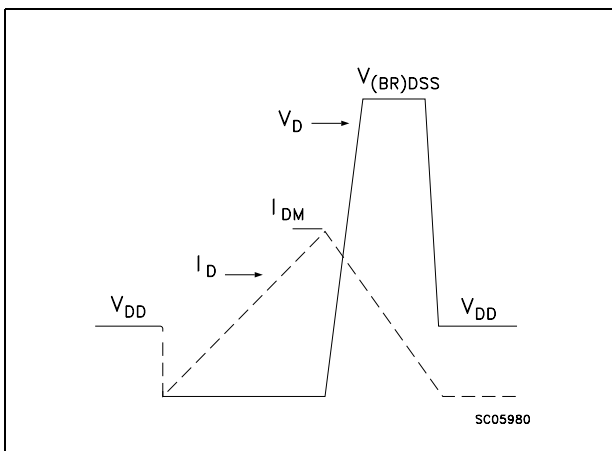


Figure 18. Switching time waveform



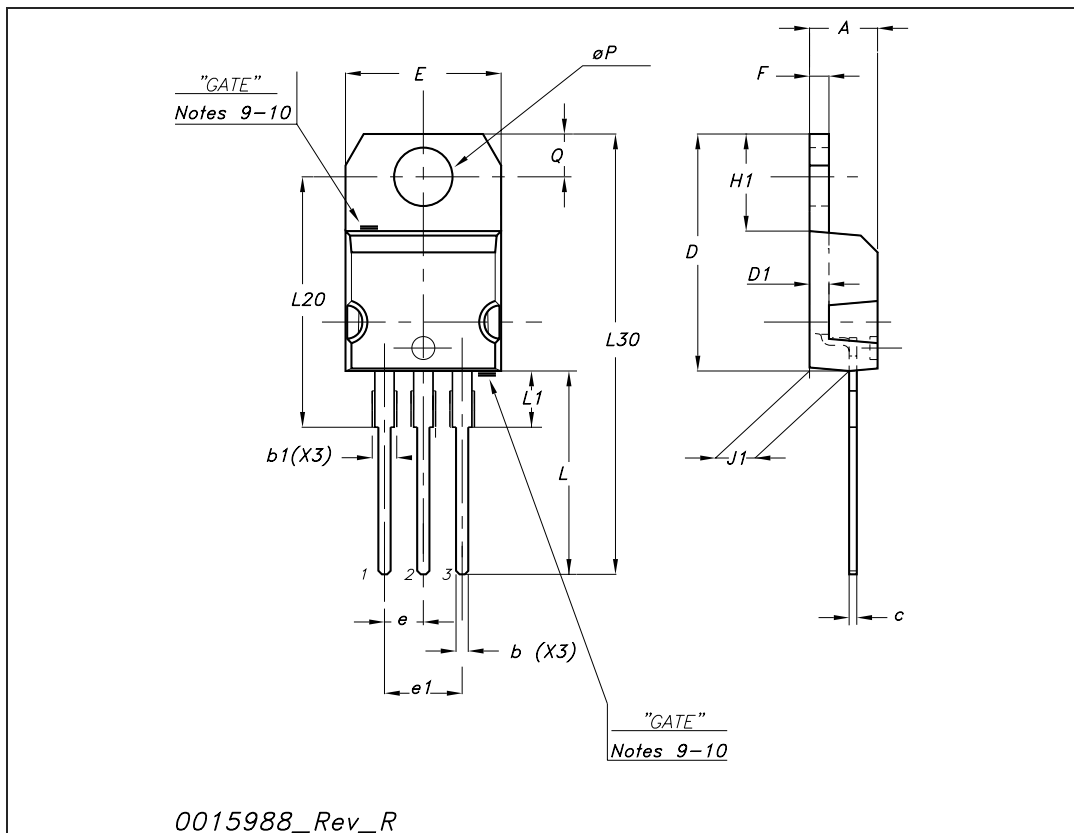


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

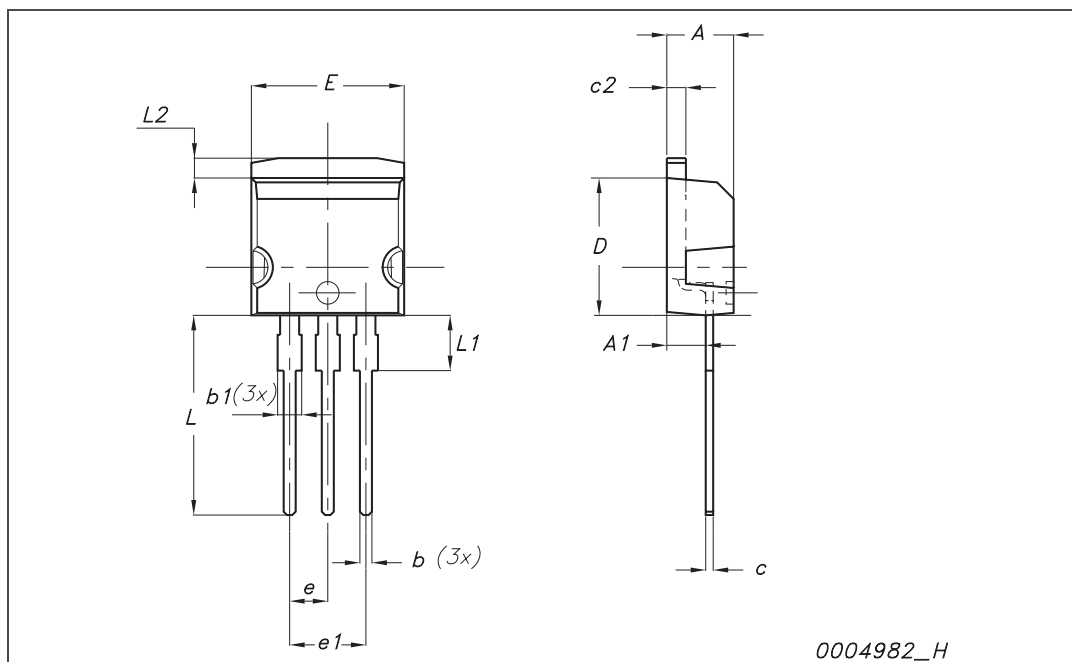
TO-220 mechanical data

Dim	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.14		1.70	0.044		0.066
c	0.48		0.70	0.019		0.027
D	15.25		15.75	0.6		0.62
D1		1.27			0.050	
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.051
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
∅P	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



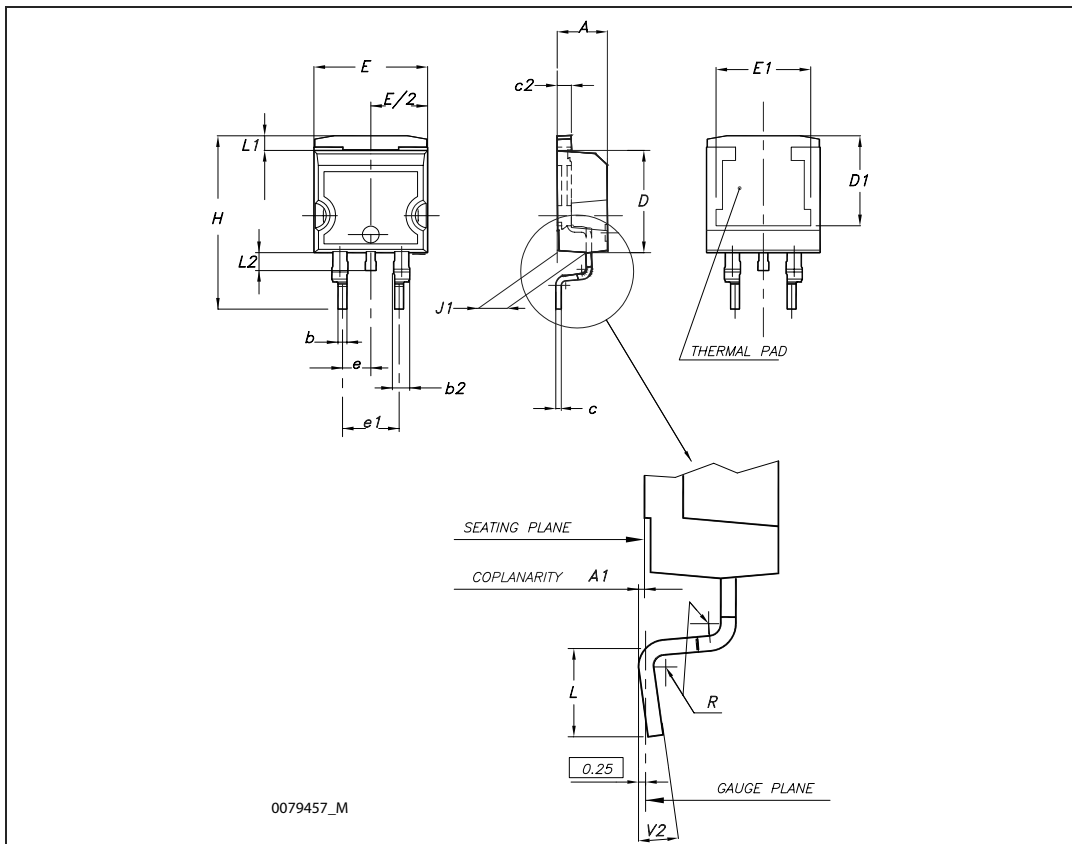
I<sup>2</sup>PAK (TO-262) mechanical data

Dim	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	4.40		4.60	0.173		0.181
A1	2.40		2.72	0.094		0.107
b	0.61		0.88	0.024		0.034
b1	1.14		1.70	0.044		0.066
c	0.49		0.70	0.019		0.027
c2	1.23		1.32	0.048		0.052
D	8.95		9.35	0.352		0.368
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
E	10		10.40	0.393		0.410
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L2	1.27		1.40	0.050		0.055



**D<sup>2</sup>PAK (TO-263) mechanical data**

Dim	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	4.40		4.60	0.173		0.181
A1	0.03		0.23	0.001		0.009
b	0.70		0.93	0.027		0.037
b2	1.14		1.70	0.045		0.067
c	0.45		0.60	0.017		0.024
c2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1	7.50			0.295		
E	10		10.40	0.394		0.409
E1	8.50			0.334		
e		2.54			0.1	
e1	4.88		5.28	0.192		0.208
H	15		15.85	0.590		0.624
J1	2.49		2.69	0.099		0.106
L	2.29		2.79	0.090		0.110
L1	1.27		1.40	0.05		0.055
L2	1.30		1.75	0.051		0.069
R		0.4			0.016	
V2	0°		8°	0°		8°



# 5 Packaging mechanical data

## D<sup>2</sup>PAK FOOTPRINT



## TAPE AND REEL SHIPMENT

**TAPE MECHANICAL DATA**

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	10.5	10.7	0.413	0.421
B0	15.7	15.9	0.618	0.626
D	1.5	1.6	0.059	0.063
D1	1.59	1.61	0.062	0.063
E	1.65	1.85	0.065	0.073
F	11.4	11.6	0.449	0.456
K0	4.8	5.0	0.189	0.197
P0	3.9	4.1	0.153	0.161
P1	11.9	12.1	0.468	0.476
P2	1.9	2.1	0.075	0.082
R	50		1.574	
T	0.25	0.35	0.0098	0.0137
W	23.7	24.3	0.933	0.956

**REEL MECHANICAL DATA**

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	24.4	26.4	0.960	1.039
N	100		3.937	
T		30.4		1.197

BASE QTY	BULK QTY
1000	1000

10 pitches cumulative tolerance on tape +/- 0.2 mm

TRL

FEED DIRECTION

Bending radius R min.

\* on sales type

## 6 Revision history

**Table 8. Revision history**

Date	Revision	Changes
07-Feb-2007	1	Initial release.
02-Apr-2008	2	Some value changes on <a href="#">Table 2</a>

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