Ordering number : ENA0891A

SANYO Semiconductors
DATA SHEET

LV24230LP-A — Bi-CMOS LSI Compact Portable Equipment 1-Chip FM Tuner IC

Overview

The LV24230LP-A is an I²C-controlled single-chip FM tuner IC that integrates external components which are necessary for tuning in a compact VQLP package with dimensions of only 4×4×0.8mm³. Equipped with a state machine, the LV24230LP-A has the capability to perform automatic tuning/seek and dissipates less power than conventional LV24000series tuner ICs.

Features

- FM FE
- FM IF
- MPX stereo decoder
- Tuning
- Standby

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max	Analog block supply voltage	5.0	V
	V_{DD} max	Digital block supply voltage	4.0	V
Maximum input voltage	$V_{IN}1$ max	SCL, SDA, Int	V_{DD}+0.3	V
	$V_{IN}2$ max	External_clk_in	V_{DD}+0.3	V
Allowable power dissipation	Pd max	Ta ≤ 70°C	140	mW
Operating temperature	Topr		-20 to +70	°C
Storage temperature	Tstg		-40 to +125	°C

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Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}	Analog block supply voltage	3.0	V
	V_{DD}	Digital block supply voltage	3.0	V
Operating supply voltage range	V_{CC} op		2.6 to 4.0	V
	V_{DD} op		2.5 to 4.0	V
	V_{IO} op	Interface voltage	1.62 to 4.0	V

Note : Supply voltage V_{IO} equal V_{DD}, or $V_{IO} < V_{DD}$ & $V_{IO} > 0.65\ V_{DD}$

Operating Characteristics at Ta = 25°C, V_{CC} = 3.0V, V_{DD} = 3.0V, Volume set at maximum, Soft Mute = 1/Soft Stereo = off with the designated test circuit

Output level set with Radio Control 1 of control register map (0Dh Bit0, Bit1 set to '1', '1')

In addition, Set IF_OSC = 150kHz, IF_BW = 100% (Radio Control 1 : 0D Bit6, Bit7 set to '1', '1')

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Current drain (in operation)	$I_{CC}A$	Analog block at 60dBμV EMF input		12	17	mA
	$I_{CC}D$	Digital block at 60 dBμV EMF input		0.3	0.8	mA
Current drain (in standby)	$I_{CC}A$	Analog standby mode		3	30	μA
	$I_{CC}D$	Digital standby mode		3	30	μA
FM receive band	F_range	Refer to PCB mounting conditions to cover the FM receive band of 76M to 108MHz	76		108	MHz
FM receive characteristics; MONO : fc = 80MHz, fm = 1kHz, 22.5kHzdev. Note that Soft_mute = 1, Soft_stereo function OFF, IHF-BPF used						
3dB sensitivity	-3dB LS	60dBμV, 22.5kHzdev output standard, -3dB input.		5	17	dBμV EMF
Practical sensitivity 1	QS1	Input at S/N = 30dB De-emphasis = 75μs, SG open display		8	16	dBμV EMF
Practical sensitivity 2 (Reference)	QS2	Input at S/N = 26dB De-emphasis = 75μs, SG terminal display		1.10		μV
Demodulation output	Vo	60dBμV EMF, pin 19 output	80	110	160	mVrms
Channel balance	CB	60dBμV EMF, pin 18 output/pin 19 output	-2	0	2	dB
Signal-to-noise ratio	S/N	60dBμV EMF, pin 19 output	48	58		dB
Total harmonic distortion 1 (MONO)	THD1	60dBμV EMF, pin 19 output, 22.5kHz dev.		0.4	1.5	%
Total harmonic distortion 2 (MONO)	THD2	60dBμV EMF, pin 19 output, 75.0kHz dev.		1.3	3	%
Field intensity display level	FS	Reg1Dh_bit0 = OFF Input level at which Reg02h_bit1-3 change from 1 to 2.	3	10	20	dBμV EMF
Mute attenuation	Mute-Att.	60dBμV EMF, pin 19 output	60	70		dB
FM receive characteristics ; STEREO characteristics : fc = 80MHz, fm = 1kHz, V_{IN} = 60dBμV EMF, Pilot = 10% (7.5kHzdev), MPX-Filter used						
Separation	SEP	L-mod, pin 19 / pin 18 output L+R signals = 30% (22.5kHz dev.)	20	35		dB
Total harmonic distortion (Main)	THD-ST1	Main-mod (for L + R input), 19 output IHF_BPF L+R signals = 30% (22.5kHzdev.)		0.6	1.8	%

Interface block allowable operation range at Ta = -20 to +70°C, V_{SS} = 0V

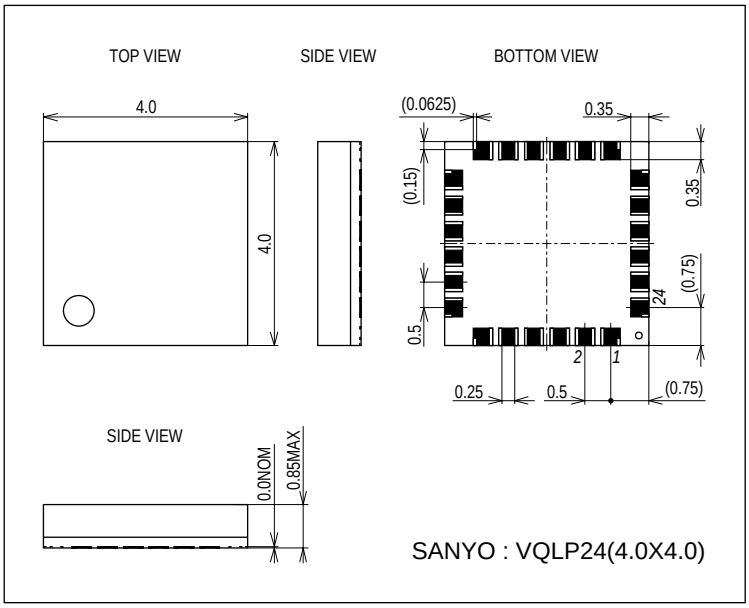
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}		2.5		4.0	V
Digital block input	V_{IH}	High-level input voltage range	$0.7V_{DD}$		V_{DD}	V
	V_{IL}	Low-level input voltage range	0		$0.1V_{DD}$	V
Digital block output	I_{OL}	Output current at Low level	2.0			mA
	V_{OL}	Output voltage at Low level I_{OL} = 2mA			0.6	V
External clock operating frequency	fclk_ext	Clock frequency for external input	32k	32.768k	20M	Hz

Note : External clock input (pin 12) allows also input of the sine wave signal.

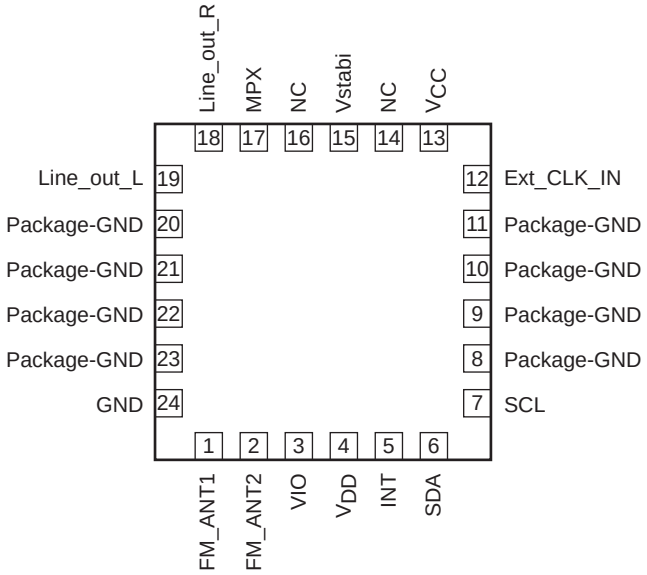
Package Dimensions

unit : mm (typ)

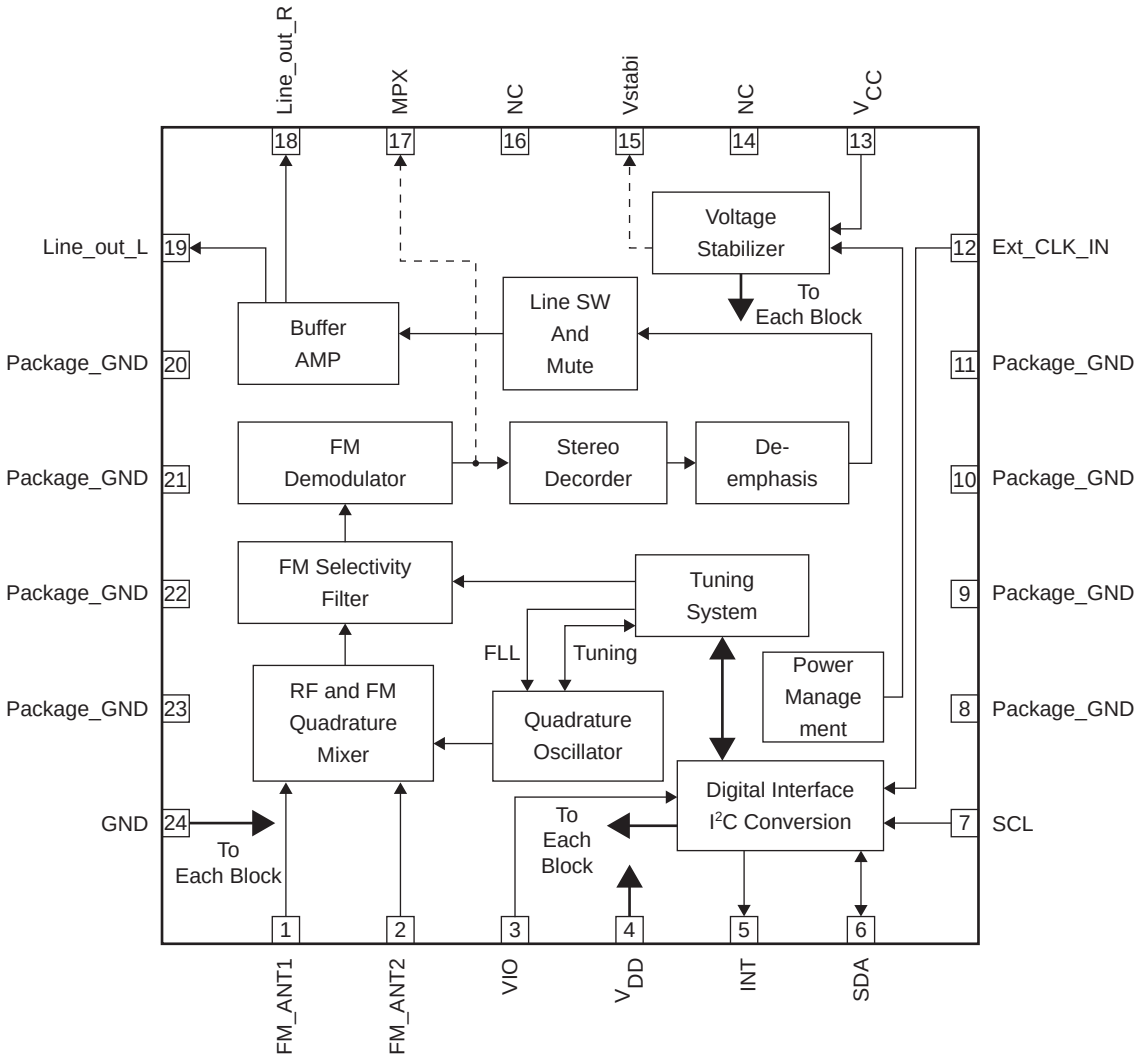
3347



Pin Assignment



Block Diagram



Pin Function

Pin No.	Pin name	Description	Pin voltage	Supplement
1	FM-ANT1	Antenna input	1V	Antenna input pin
2	FM-ANT2	Antenna GND	1V	Antenna input pin. For pin 1 single input, pin 2 is set to AC_GND via capacity
3	VI/O	Digital interface supply voltage		Power pin dedicated to the interface input/output elements
4	V_{DD}	Digital supply voltage		Power pin for digital block
5	INT	Interrupt line		Output pin dedicated to interrupt (hardware output: used for options) Addition of pull-up or pull-down resistor recommended to cope with initial instability
6	SDA	Digital interface DATA ine)		Bidirectional data line. Pull up to Vio line with 2.2k resistor
7	SCL	Digital interface Clock line)		Clock wire. Pull up to Vio line with 2.2k resistor
8	Package-GND	GND for package-shield		BND pin for package shield
9	Package-GND	GND for package-shield		BND pin for package shield
10	Package-GND	GND for package-shield		BND pin for package shield
11	Package-GND	GND for package-shield		BND pin for package shield
12	Ext_CLK_IN	Reference clock-source input for measurement		External standard CLK input pin. Connect X'tal, if used, to GND. (CITIZEN CFS-206, CM31S recommended)
13	V_{CC}	Analog supply voltage		Power pin for analog (tuner) block
14	NC			Keep this open.
15	Vstabi.	Stabilizer voltage	2.6V	Local oscillator reference bias pin. NC pin to be used
16	NC			Keep this open.
17	MPX	MPX-signal output	2.3V	Stereo decoder input monitor pin. NC pin to be used
18	LINE-OUT-R	Radio Rch Line-output	1.2V	Audio R_ch output
19	LINE-OUT-L	Radio Lch Line-output	1.2V	Audio L_ch output
20	Package-GND	GND for package-shield		GND pin for package shield
21	Package-GND	GND for package-shield		GND pin for package shield
22	Package-GND	GND for package-shield		GND pin for package shield
23	Package-GND	GND for package-shield		GND pin for package shield
24	GND	GND (Analog and Digital GND)		GND pin for analog (FM tuner) block and digital (control) block

Format of Bus Transfers

Bus transfers are primarily based on the I²C primitives

- Start condition
- Repeated start condition
- Stop condition
- Byte write
- Byte read

Start, restart, and stop conditions are specified as shown in Table 1 below.

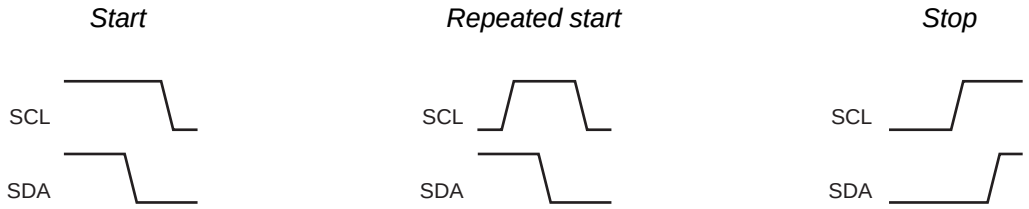


Fig. 1 the I²C start, repeated start and stop conditions.

For details, like timing, etc., refer to specifications of I²C.

8-bit write

8-bit data is sent from the master microcomputer to LV24230LP-A.
Data bit consists of MSB first and LSB last.
Data transmission is latched at the rising edge of SCL in synchronization with the SCL clock generated at the master IC.
Do not change data while SCL remains HIGH.
LV24230LP-A outputs the ACK bit between eighth and ninth falling edges of SCL

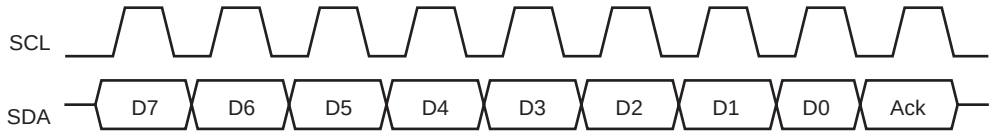


Fig. 2 Signal pattern of the I²C byte write

Read is of the same form as write, only except that the data direction is opposite.
Eight data bits are sent from LV24230LP-A to the master while Ack is sent from the master to LV24230LP-A.

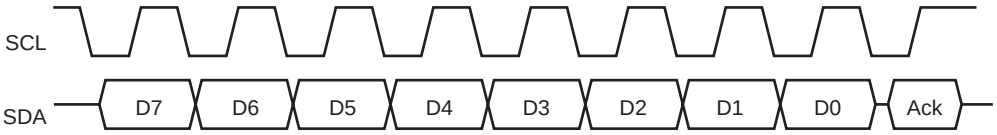


Fig. 3 Signal pattern of the I²C byte read

The serial clock SCL is supplied from the master side. It is essential that data bit is output from LV24230LP-A in synchronization with the falling edge while the master side performs latching at the rising edge.

LV24230LP-A latches ACK at the rising edge.
The sequence to write data D into the register A of LV24230LP-A is shown below.

- Start condition
- write the device address (C0h)
- write the register address, A
- write the target data, D
- stop condition

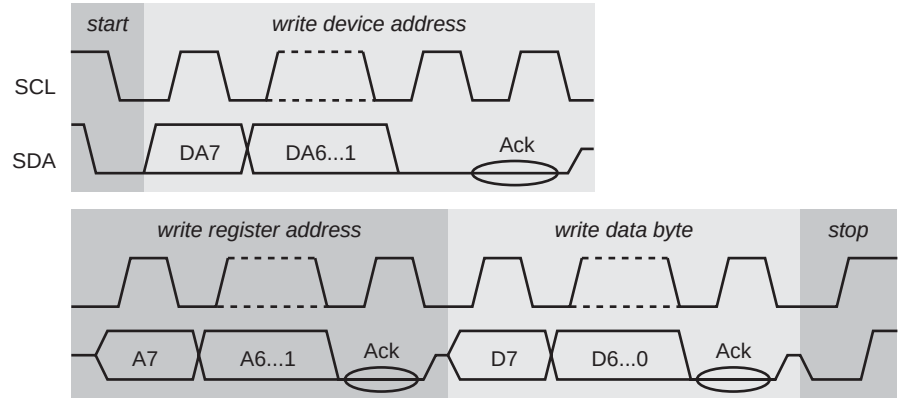


Fig. 4 Register write through I²C

When one or more data has been provided for writing, only the first data is allowed to be written.

Read sequence

- start condition
- write the device address (C0h)
- write the register address, A
- repeated start condition (or stop + start in a single master network)
- write the device address + 1 (C1h)
- read the register contents D, transmit NACK (no more data to be read)
- stop condition

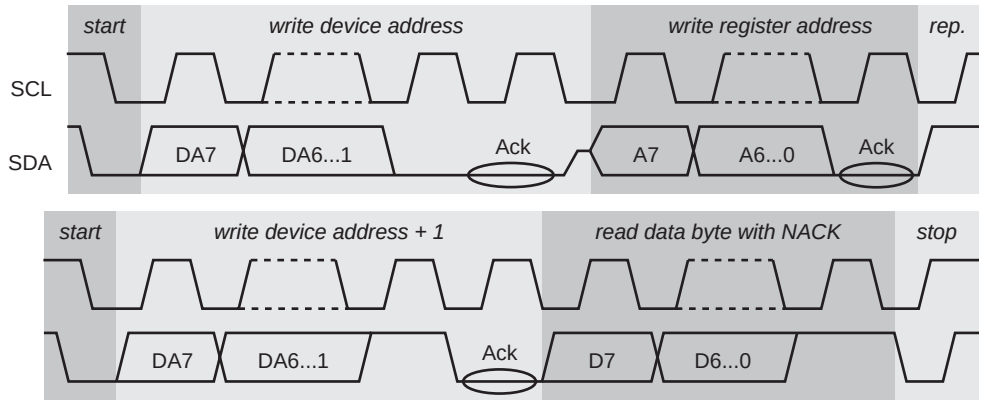


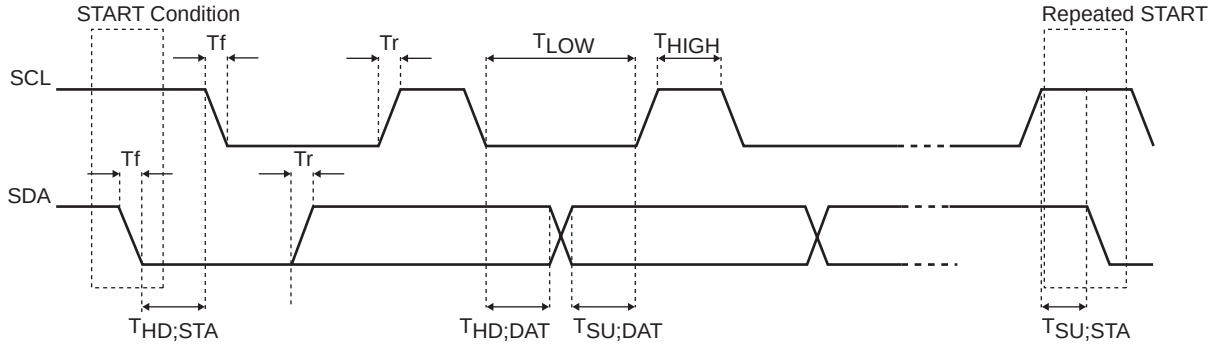
Fig. 5 Register read through I²C

Interrupt Pin INT

LV24230LP-A has the dedicated interrupt output pin. For the active level to the host, either LOW or HIGH can be selected. The INT output pin is kept floating while the PWRAD bit is cleared during initialization.
Therefore, to avoid influence on the CPU side during initialization, it is recommended to secure the non-active state by means of the pull-up or pull-down resistor.
This enables direct INT output connection to non-masking interruption of the host CPU.

Digital interface specification (interface specification : reference)

(1). Characteristics of SDA and SCL bus line relative to the I²C bus interface



Parameter	Symbol	Standard-mode		High_Speed-mode		unit
		min	max	min	max	
SCL clock frequency	F_{SCL}	0	100	0	400	kHz
Fall time of both SDA and SCL	Tf		300	20+0.1Cb	300	ns
Rise time of both SDA and SCL	Tr		1000	20+0.1Cb	300	ns
High time of SCL	T_{HIGH}	4.0		0.6		μs
Low time of SCL	T_{LOW}	4.7		1.3		μs
Hold time of STAT condition	$T_{HD\ ;\ STA}$	4.0		0.6		μs
Hold time of Data	$T_{HD\ ;\ DAT}$	0	3.45	0	0.9	μs
Set-up time of STAT condition	$T_{SU\ ;\ STA}$	4.7		0.6		μs
Set-up time of STOP condition	$T_{SU\ ;\ STO}$	4.0		0.6		μs
Set-up time of Data	$T_{SU\ ;\ DAT}$	250		100		ns
Bus free time between a STOP and	T_{BUF}	4.7		1.3		μs
Capacitivie load for each bus line	Cb		400		400	pF

*Cb = Total capacitance of one bus line

(2). Register map (On Register Map)

Following is Sub address map of LV24230LP-A. Each register becomes 8-bit constitution.

Address	Register Name	Mode	Remark
00h	CHIP_ID	R/W	Chip ID
02h	RADIO_STAT	R	Status of Radio Station
0Bh	RFCAP	R/W	RF Cap bank
0Dh	RADIO_CTRL1	R/W	Radio Control 1
0Eh	RADIO_CTRL2	R/W	Radio Control 2
0Fh	RADIO_CTRL3	R/W	Radio Control 3
10h	TNPL	R	Tune Position Low
11h	TNPH_STAT	R	Tune Position High and Status
19h	REF_CLK_PRS	R/W	Reference clock pre-scalar
1Ah	REF_CLK_DIV	R/W	Reference clock divider
1Bh	REF_CLK_OFF	R/W	Reference clock offset
1Dh	SCN_CTRL	R/W	Scan control
1Eh	TARGET_VAL_L	R/W	Target value Low
1Fh	TARGET_VAL_H	R/W	Target value High

R : Read only register R/W : Read and Write register

(3). Register description (ON Contents of each Register)

Register 00h – CHIP_ID – Chip identify register (Read/Write)

7	6	5	4	3	2	1	0
ID [7 : 0]							

bit 7-0 : **ID [7 : 0] :** 8-bit chip ID.
LV24230LP-A : 12h

Note : To abort the command, write any value in this register.

Register 02h – RADIO_STAT – Radio station status (Read-Only)

7	6	5	4	3	2	1	0
RAD_IF	N/A	N/A	MO_ST	FS [2 : 0]			SF5DB

bit 7 : **RAD_IF :** Radio interrupt flag.
0 = no interrupt
1 = interrupt
Note :
When status (field strength, stereo/mono) changes, this bit is set.
If Interrupt of IRQ pin is enabled, Interrupt pin is set by following IPOL register condition.
This bit is cleared by register read. In stand-by mode (PW_RAD = 0), this bit is 1

bit 6-5 : **NA [1 : 0] :** NA 0 fixed

bit 4 : **MO_ST :** Mono/stereo indicator
0 = Forced monaural
1 = Normal (Receiving in stereo mode)

bit 3-1 **FS [2 : 0] :** Fieldstrength :
0 = Low field strength
…
7 = High field strength

bit 0 : **SF5DB :** Fieldstrength +5dB :
0 = FS5dB no UP
1 = FS5dB UP

For details, refer to Application note.

Register 0Bh – RFCAP – RF Cap bank (Read/Write)

7	6	5	4	3	2	1	0
RFCAP [7 : 0]							

bit 7-0 : **RFCAP [7 : 0] :** RF Oscillator CAP bank

Register 0Dh – RADIO_CTRL1 – Radio control 1 (Read/Write)

7	6	5	4	3	2	1	0
IF_SEL	IFBWSEL	AGC_SPD	DEEM	ST_M	nMUTE	VOL [1 : 0]	

bit 7 : **IF_SEL :** IF Frequency Setting
0 = 130kHz
1 = 150kHz

bit 6 : **IFBWSEL :** IF band width setting
0 = 50%
1 = 100%

bit 5 : **AGC_SPD :** AGC Speed setting
0 = Normal
1 = High

bit 4 : **DEEM :** de-emphasis
0 = 50μs : Korea, China, Europe, Japan
1 = 75μs : USA

bit 3 : **ST_M :** Stereo/mono setting
0 = Stereo enabled
1 = Stereo disabled (mono mode)

bit 2 : **nMUTE :** Audio Mute
0 = Mute On
1 = Mute Off

bit 1-0 : **VOL [1 : 0] :** Volume Setting
0 : Min
…
3 : Max

Register 0Eh – RADIO_CTRL2 – Radio control 2 (Read/Write)

7	6	5	4	3	2	1	0
SOFTST [2 : 0]			SOFTMU [2 : 0]			N/A	STABI_BP

bit 7-5 : **SOFTST [2 : 0] :** Soft Stereo setting
000b = Soft stereo level 3
001b = Disable soft stereo
010b = Soft stereo level 1 (*)
100b = Soft stereo level 2
Note : do not use without these value.
(*) : recommended setting

bit 4-2 : **SOFTMU [2 : 0] :** Soft audio mute setting
000b = Soft audio mute level 3
001b = Disable soft audio mute
010b = Soft audio mute level 1
100b = Soft audio mute level 2 (*)
Note : do not use without these value.
(*) : recommended setting

bit 1 : Reserved : 0 (Fix)

bit 0 : **STABI_BP :** Internal regulator by-pass bit
0 = Internal regulator operate (normal)
1 = Internal regulator by-pass

Register 0Fh – RADIO_CTRL3 – Radio control 3 (Read/Write)

7	6	5	4	3	2	1	0
IPOL	SM_IE	RAD_IE	SD_PM	nIF_PM	EXT_CLK_CFG [1 : 0]		PW_RAD

bit 7 : **IPOL :** Interrupt (IRQ) Polarity
0 = IRQ active high
1 = IRQ active low

bit 6 : **SM_IE :** Command end interrupt
0 = Disable
1 = Enable

bit 5 : **RAD_IE :** Radio Interrupt (field strength/stereo changes)
0 = Disable
1 = Enable

bit 4 : **SD_PM :** Stereo decoder clock PLL mute
0 = SD PLL On (Normal Operation)
1 = SD PLL Off (Adjustment)

bit 3 : **nIF_PM :** IF PLL mute
0 = IF PLL Off (Adjustment)
1 = IF PLL On (Normal Operation)

bit 2-1 : **EXT_CLK_CFG [1 : 0] :** External Clock Setting

EXT_CLK_CFG [1 : 0]	**Reference clock**
00	Off
01	32768Hz crystal oscillator
10	Oscillator clock source / 32 (for high frequency source)
11	Oscillator clock source (for low frequency source)

bit 0 : **PW_RAD :** Radio Circuit Power
0 = Power Off (Stand-by).
1 = Power On
Note : At the time of start, PW_RAD becomes 0 (Stand-by)

Register 10h – TNPL – Tune position low (Read-Only)

7	6	5	4	3	2	1	0
TUNEPOS [7 : 0]							

bit 7-0 : **TUNEPOS [7 : 0] :** Current RF Frequency (Low 8bit)

Register 11h – TNPH_STAT – Tune position high/status (Read-Only)

7	6	5	4	3	2	1	0
ERROR [2 : 0]			SM_IF	TUNED	NA	TUNEPOS [9 : 8]	

bit 7-5 : **ERROR [2 : 0] :** Error Code

ERROR [2 : 0]	Remark
0	OK, Command end (No Error)
1	Default value after or during reset
2	Band Limit Error
3	DAC Limit Error
6	Command forced End
7	Command busy

bit 4 : **SM_IF :** Command End interrupt flag
0 = No Interrupt
1 = Interrupt

This bit is set when the command is over. When the IRQ pin interrupt is allowed, the pin status is changed, Reading this register causes clearing.

bit 3 : **TUNED :** Radio tuning Flag
0 = No tune
1 = Tuned
Note : This flag is set when Tuned or a station search succeeded.
This flag is cleared under 3 conditions as below.
(1) PW_RAD = 0
(2) Tuning Frequency
(3) FM station searching

bit 2 : **NA :** 0 (Fix)

bit 1 : 0 : **TUNEPOS [9 : 8] :** Current RF frequency (High 2 bit)

Register 19h – REF_CLK_PRS – Reference clock prescaler (Read/Write)

7	6	5	4	3	2	1	0
REFPRE [2 : 0]			REFMOD [4 : 0]				

bit [7 : 5] : **REFPRE [2 : 0] :** Reference Clock pre- scaler
0 = 1 : 1
1 = 1 : 2
…
7 = 1:128

bit [4 : 0] : **REFMOD [4 : 0] :** 5-bit slope correction

Register 1Ah – REF_CLK_DIV – Reference clock divider (Read/Write)

7	6	5	4	3	2	1	0
REFDIV [7 : 0]							

Bit 7-0 : **REFDIV [7 : 0] :** Reference Clock Divider
0 : Divider Value = 1
1 : Divider Value = 2
…
255 : Divider Value = 256

Register 1Bh –REF_CLK_OFF – Reference clock offset (Read/Write)

7	6	5	4	3	2	1	0
REFOFFS [7 : 0]							

Bit 7-0 : **REFOFFS [7 : 0] :** Offset register for the spread of reference clock

Register 1Dh – SCN_CTRL – Scan control (Read/Write)

7	6	5	4	3	2	1	0
GRID [1 : 0]		FLL_ON	FLL_MODE	FS [2 : 0]			SHF5DB

bit 7-6 : **GRID [1 : 0] :** FM station search frequency interval :
0 = IFSD set
1 = 50kHz grid
2 = 100kHz grid
3 = 200kHz grid

bit 5 : **FLL_ON :** FLL Control
0 = FLL OFF
1 = FLL ON
During setting of the FM frequency and during seek, keep this OFF. Turn it ON after tuning.

bit 4 : Reserved : 0 (Fix)

bit 3-1 : **FS [2 : 0] :** Field strength setting at the time of FM station search and a frequency adjustment bit
Set 1 for setting of IFSD.

bit 0 : **SHF5DB :** Scan stop level +5dB

Register1Eh – TARGET_VAL_L – Target Value Low Register (Read/Write)

7	6	5	4	3	2	1	0
TARGET [7 : 0]							

bit 7-0 : **TARGET [7 : 0] :** Target frequency low 8 bit :
Tuning frequency or Limit Frequency for FM Station Search

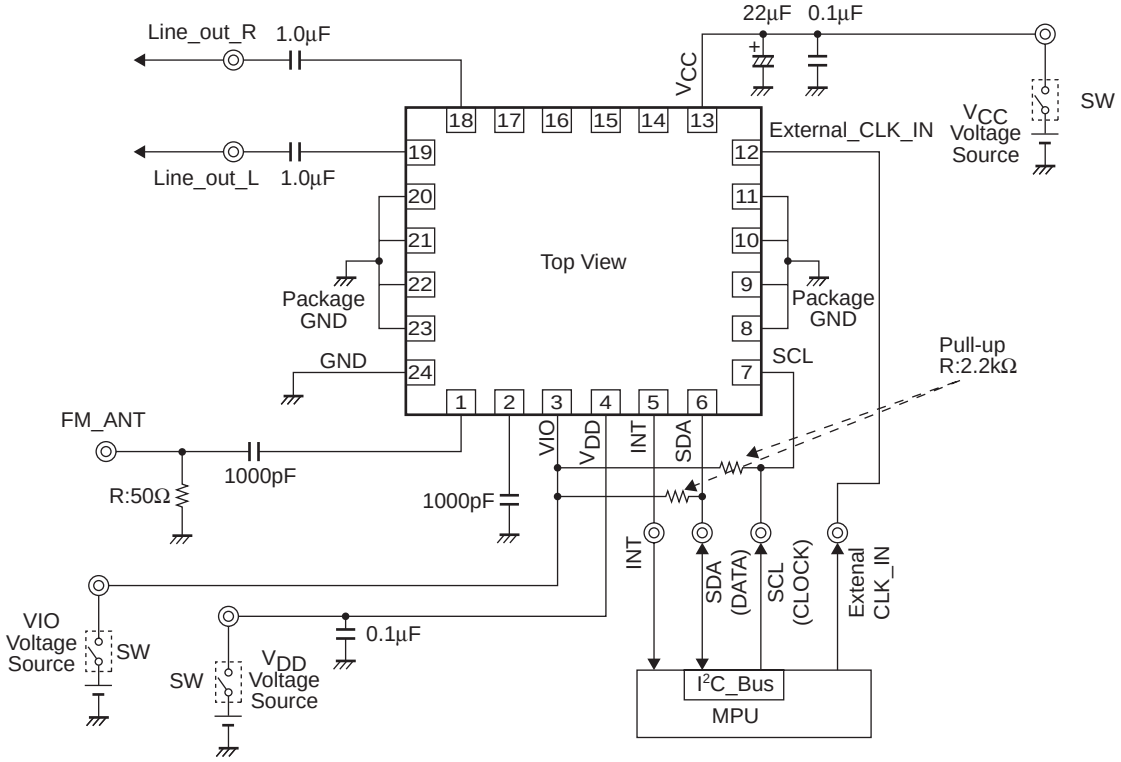
Register 1Fh – TARGET_VAL_H – Target Value High Register (Read/Write)

7	6	5	4	3	2	1	0
TARGET [15 : 8]							

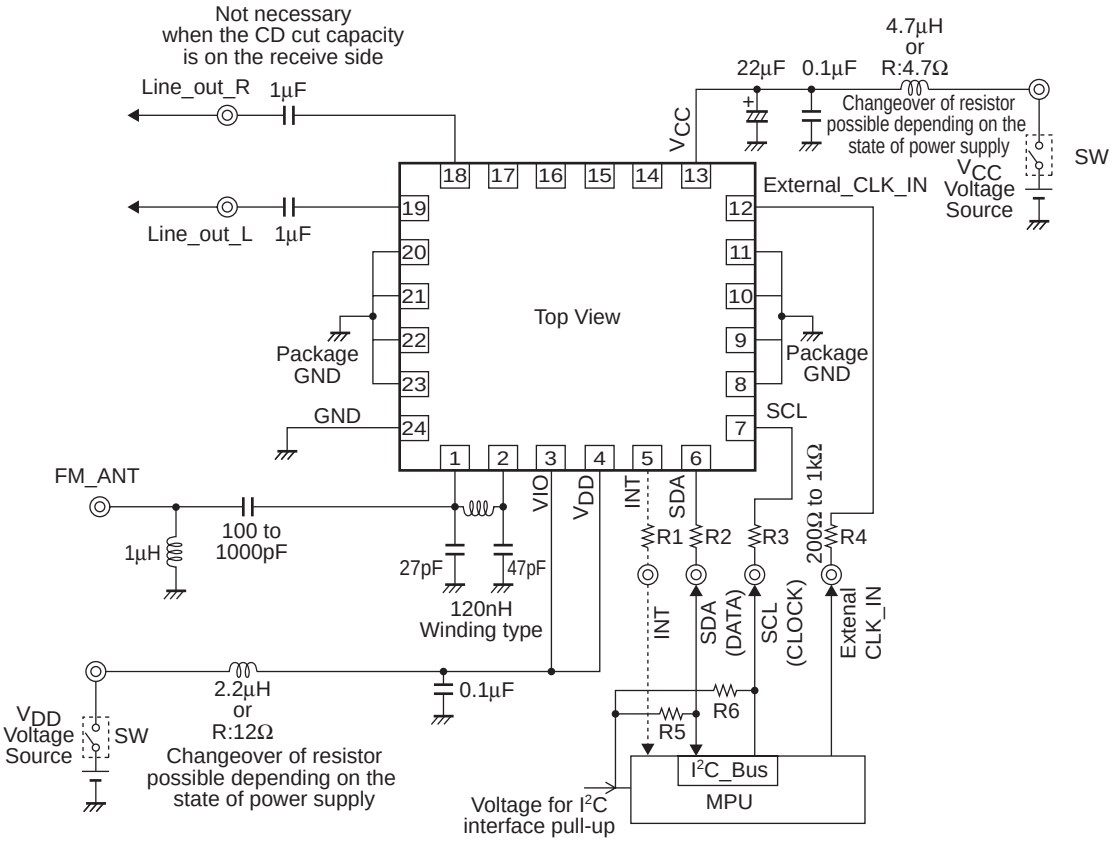
bit 7-0 : **TARGET [15 : 8] :** Target frequency High 8 bit :
Target value of oscillator calibration, Tuning frequency value or limit frequency value for station search
Note : GRID [1 : 0] is not 0 TARGET [15 : 14] has different definition

With radio power ON, lower eight bits of the target frequency are set. Then, set higher eight bits of the target frequency to this register. The command is executed.

Test Circuit



Application Circuit



Cautions for mounting of IC

Note1 : For external part constant, the recommended value is described. Since the constant may differ during actual use with the set mounted, be sure to consider optimization.

Note2 : The differential input antenna application is described. Single input with pin 1 only is also possible.

Note3 : If the spike noise between MPU and IC is large during communication, it is recommended to add limiting resistors R1, R2, and R3 between MPU and IC. 0Ω at 1.8V.

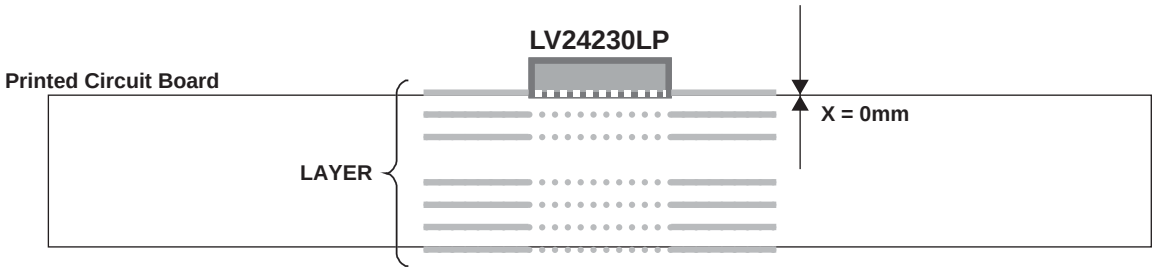
Note4 : To reduce noise from power supply, add a capacitor between V_{CC} - GND and between V_{DD} - GND.

Note5 : The I²C bus communication line requires pull-up resistors R5 and R6. The commonly-employed resistance value is 2.2k. Set the pull-up voltage to the same one of VIO of LV24230LP-A. (Supply from the same source as VIO and V_{DD} is recommended.

Note6 : Please use the INT pin arbitrarily. Recommended to open when unused.
The INT pin becomes unstable at IC startup. To protect MPU from any effects during startup, it is recommended to add either the pull-up or pull-down resistor to set the non-active mode. (This is not necessary when the MPU can be set to non-active by a software during initialization.

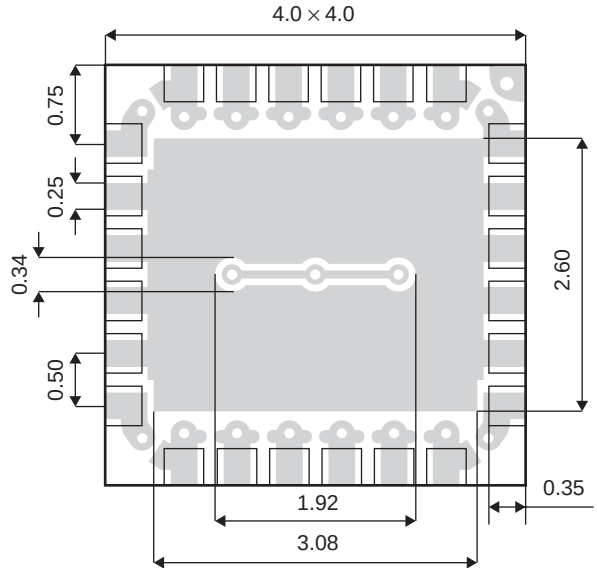
PCB Mounting Conditions to cover the FM Receiving Area of 76M to 108MHz

LV24230LP-A's PCB mounting conditions

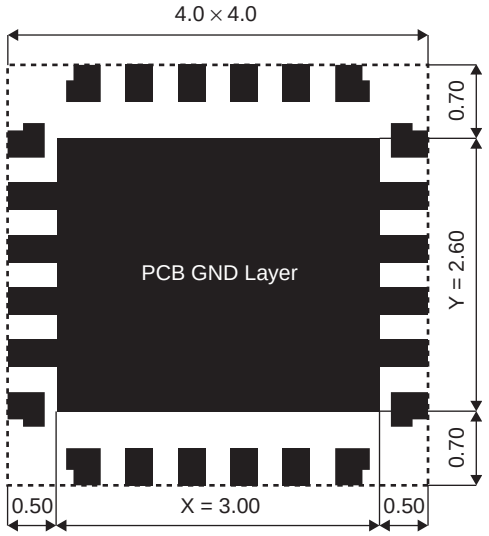


- LV24230LP-A has an inductor for local oscillator on the package bottom side.
  In order to cover the receiving frequency range of 76MHz to 108MHz, provide the GND layer to the first layer of Side A of PCB that is directly below the package bottom side, as shown in the figure.

Recommended layout of PCB substrate



IC backside_LV24230LP-A



IC directly-below_PCB recommended GND patten diagram

- With this SPL, the receiving frequency is measured under the following conditions :
- The X-value can be set freely between Min = 2.4mm and Max = 3.0mm with reference to IC.
  (The X-value for Sanyo Demo Board is 2.8mm.)
- The Y-value can be set freely between Min = 2.0mm and Max = 3.0mm with reference to IC.
  (The Y-value for Sanyo Demo Board is 2.6mm.)
- Avoid providing another wiring within 0.4mm of bottom layer of PCB_GND as much as possible.