

RQK2501YGDQA

Silicon N Channel MOS FET
Power Switching

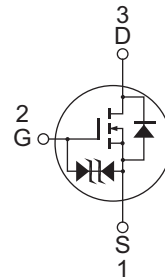
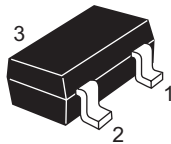
REJ03G1521-0200
Rev.2.00
Nov 06, 2007

Features

- High drain to source voltage and Low gate drive
 V_{DSS} : 250 V and 2.5 V gate drive
- Low drive current
- High speed switching
- Small traditional package (MPAK)

Outline

RENESAS Package code: PLSP0003ZB-A
(Package name: MPAK)



1. Source
2. Gate
3. Drain

Absolute Maximum Ratings

($T_a = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	250	V
Gate to source voltage	V_{GSS}	± 10	V
Drain current	I_D	0.4	A
Drain peak current	$I_{D(pulse)}$ ^{Note1}	1.6	A
Body - drain diode reverse drain current	I_{DR}	0.4	A
Channel dissipation	P_{ch} ^{Note2}	0.8	W
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

Notes: 1. $PW \leq 10 \mu\text{s}$, Duty cycle $\leq 1\%$

2. When using the glass epoxy board (FR-4 40 × 40 × 1 mm)

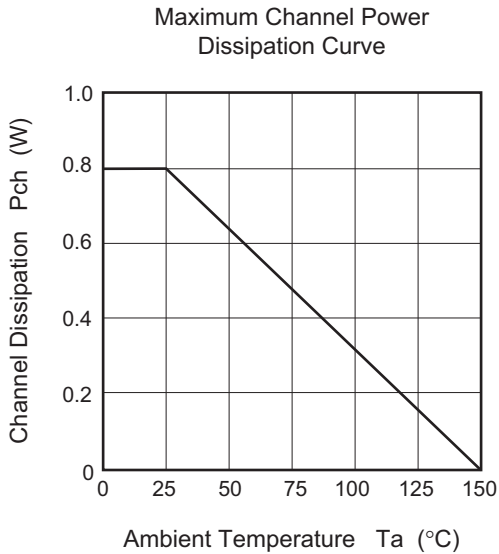
Electrical Characteristics

(Ta = 25°C)

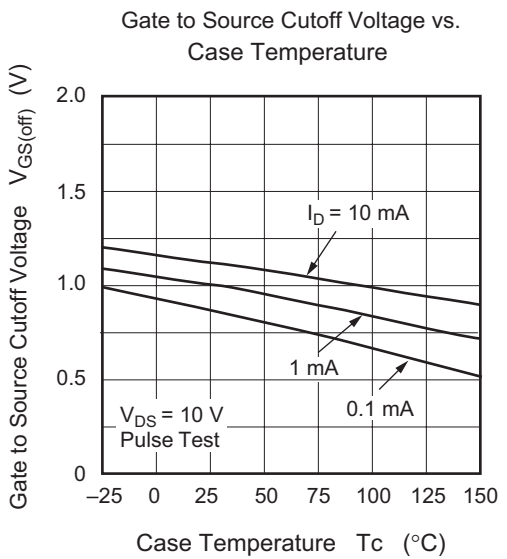
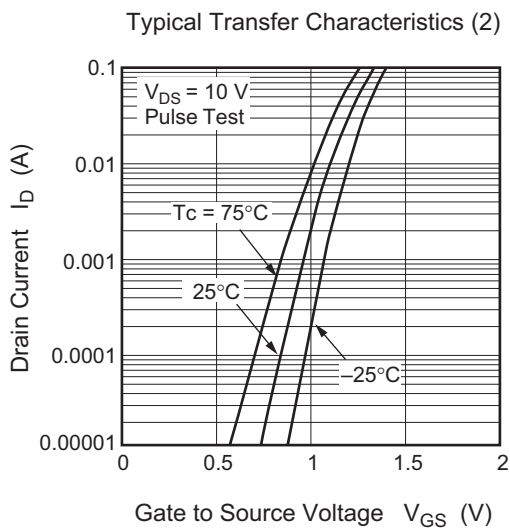
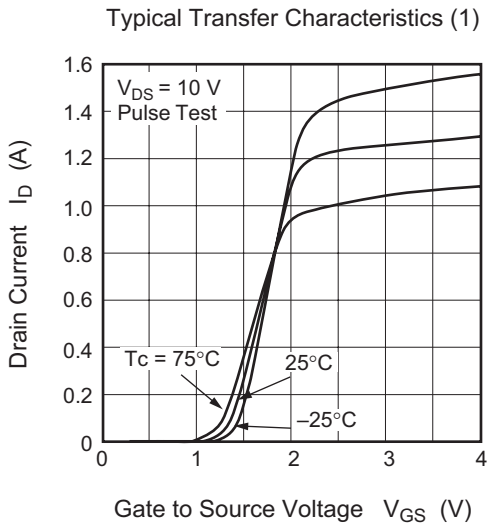
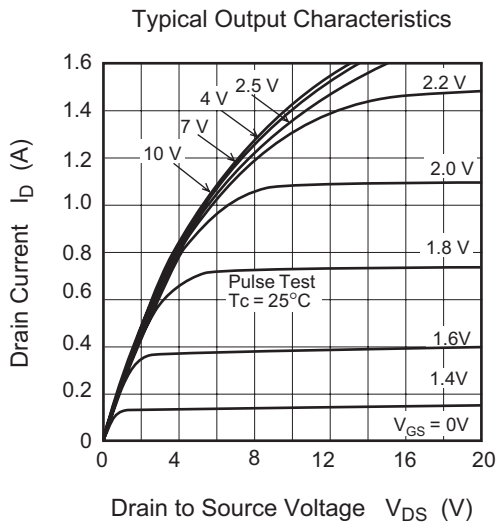
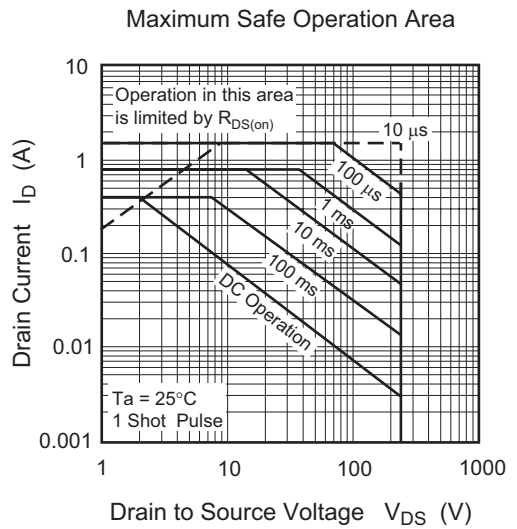
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	250	—	—	V	$I_D = 10 \text{ mA}, V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	+10	—	—	V	$I_G = +100 \mu\text{A}, V_{DS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	-10	—	—	V	$I_G = -100 \mu\text{A}, V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	+10	μA	$V_{GS} = +8 \text{ V}, V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	-10	μA	$V_{GS} = -8 \text{ V}, V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS} = 250 \text{ V}, V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	0.5	—	1.5	V	$V_{DS} = 10 \text{ V}, I_D = 1 \text{ mA}$
Drain to source on state resistance	$R_{DS(on)}$	—	4.0	5.4	Ω	$I_D = 0.2 \text{ A}, V_{GS} = 4 \text{ V}$ ^{Note3}
Drain to source on state resistance	$R_{DS(on)}$	—	4.1	5.6	Ω	$I_D = 0.2 \text{ A}, V_{GS} = 2.5 \text{ V}$ ^{Note3}
Forward transfer admittance	$ y_{fs} $	0.6	0.95	—	S	$I_D = 0.2 \text{ A}, V_{DS} = 10 \text{ V}$ ^{Note3}
Input capacitance	C_{iss}	—	80	—	pF	$V_{DS} = 25 \text{ V}$
Output capacitance	C_{oss}	—	10	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	3	—	pF	$f = 1 \text{ MHz}$
Turn - on delay time	$t_{d(on)}$	—	15	—	ns	$V_{DD} = 125 \text{ V}, V_{GS} = 4 \text{ V}$
Rise time	t_r	—	16	—	ns	$I_D = 0.2 \text{ A}$
Turn - off delay time	$t_{d(off)}$	—	40	—	ns	$R_L = 625 \Omega$
Fall time	t_f	—	38	—	ns	$R_g = 10 \Omega$
Total gate charge	Q_g	—	4.0	—	nC	$V_{DD} = 200 \text{ V}$
Gate to Source charge	Q_{gs}	—	0.5	—	nC	$V_{GS} = 4 \text{ V}$
Gate to drain charge	Q_{gd}	—	2.6	—	nC	$I_D = 0.4 \text{ A}$
Body - drain diode forward voltage	V_{DF}	—	0.8	1.2	V	$I_F = 0.4 \text{ A}, V_{GS} = 0$ ^{Note3}

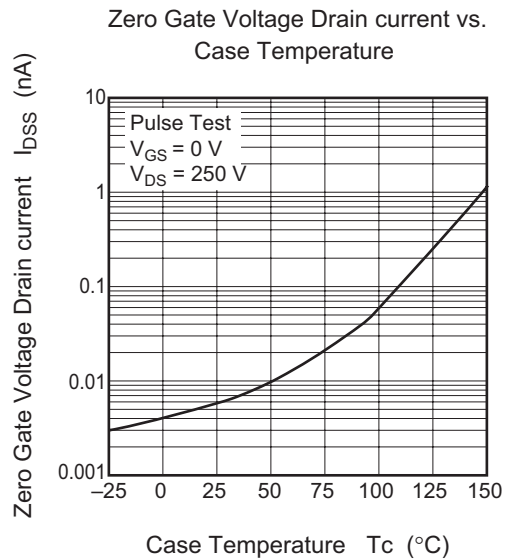
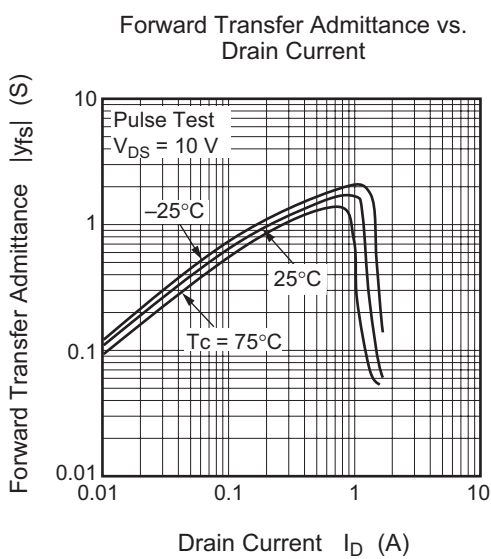
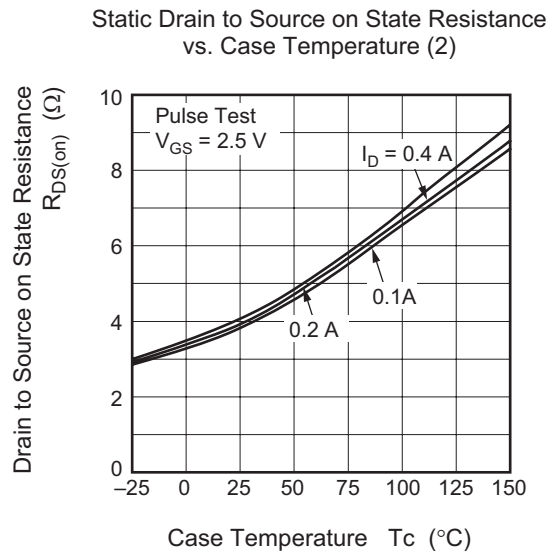
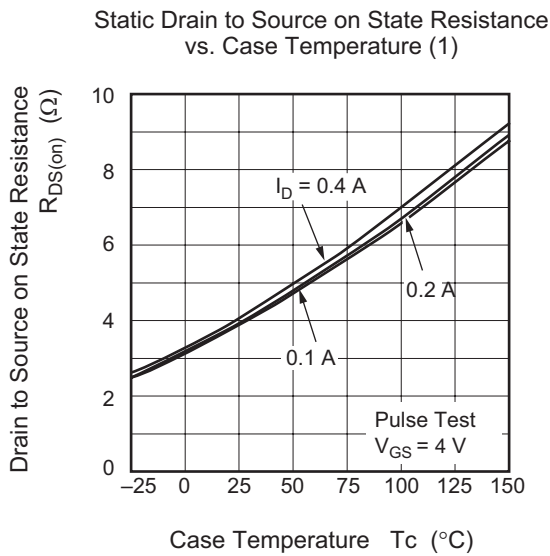
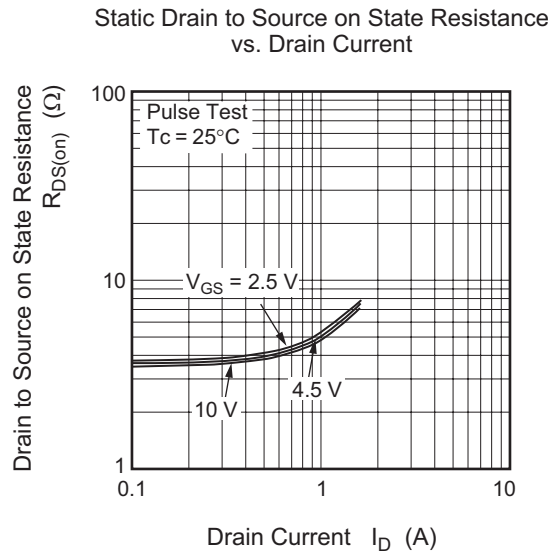
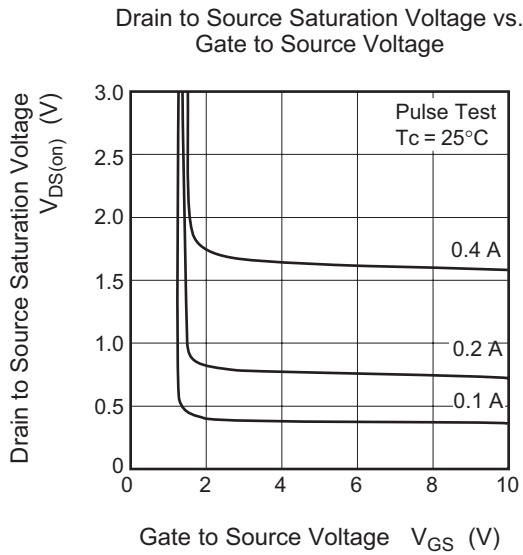
Notes: 3. Pulse test

Main Characteristics

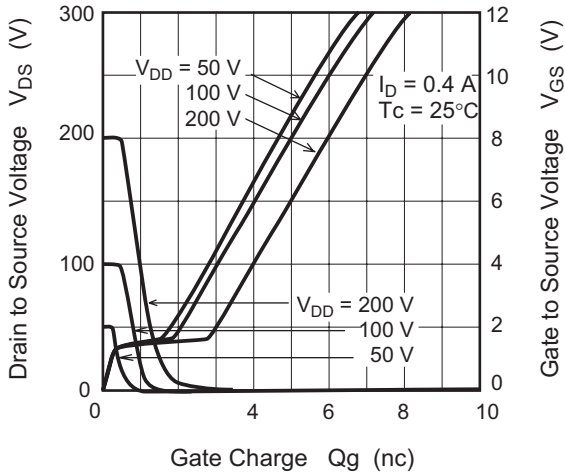


*When using the glass epoxy board (FR-4 40 x 40 x 1 mm)

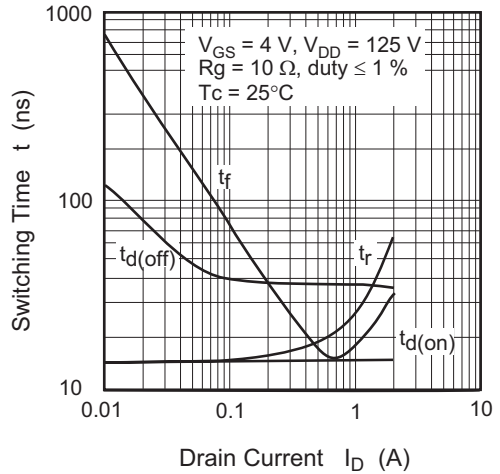




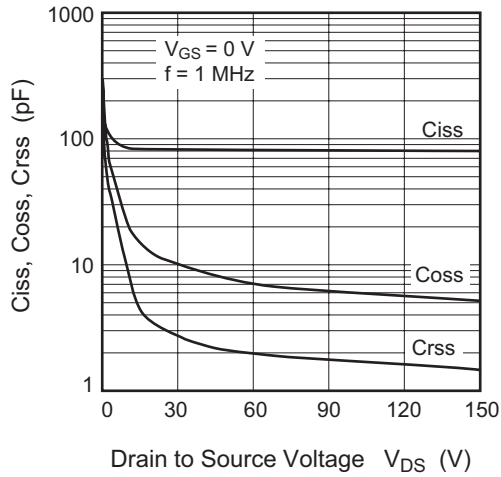
Dynamic Input Characteristics



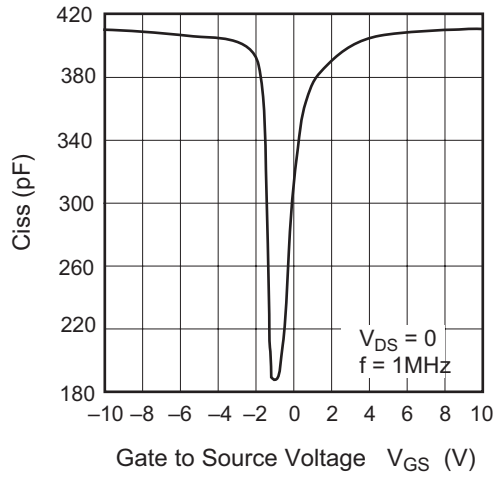
Switching Characteristics



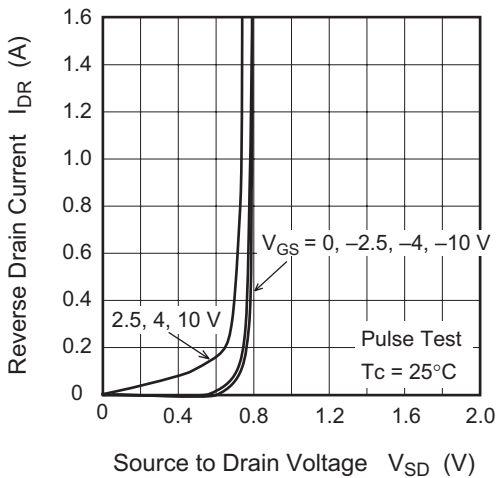
Typical Capacitance vs. Drain to Source Voltage



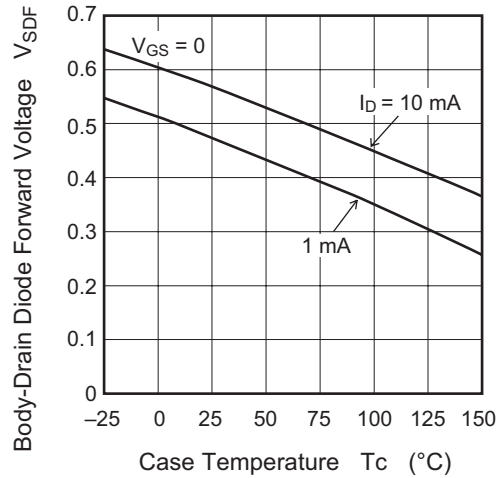
Input Capacitance vs. Gate to Source Voltage



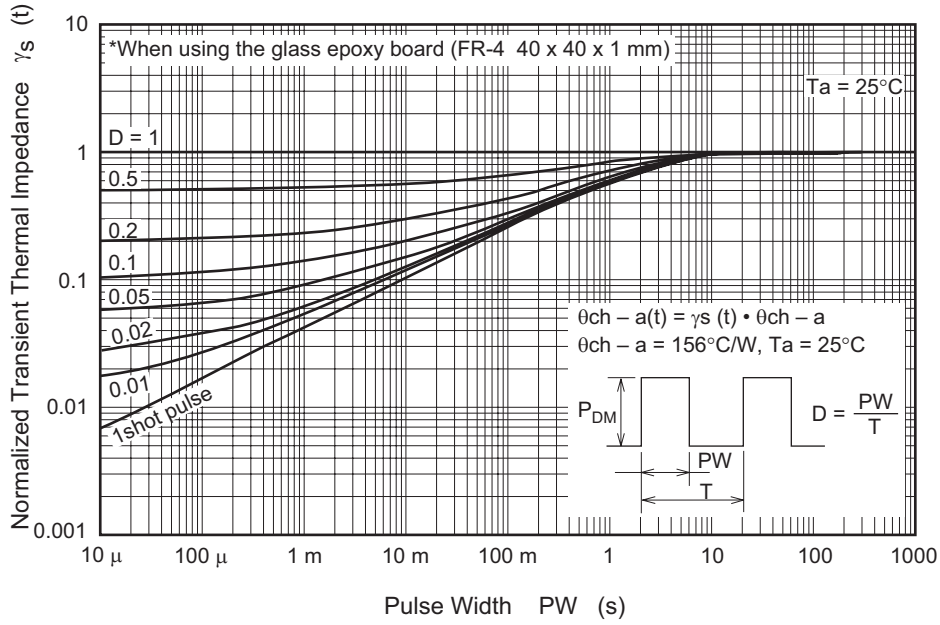
Reverse Drain Current vs. Source to Drain Voltage



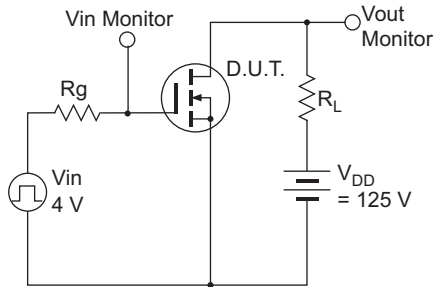
Body-Drain Diode Forward Voltage vs. Case Temperature



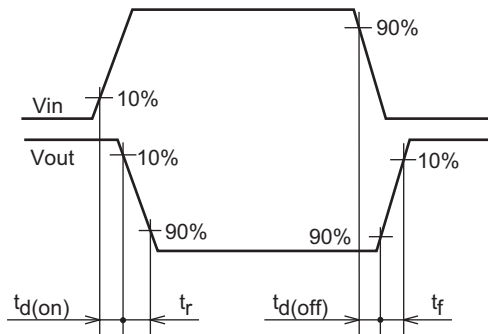
Normalized Transient Thermal Impedance vs. Pulse Width



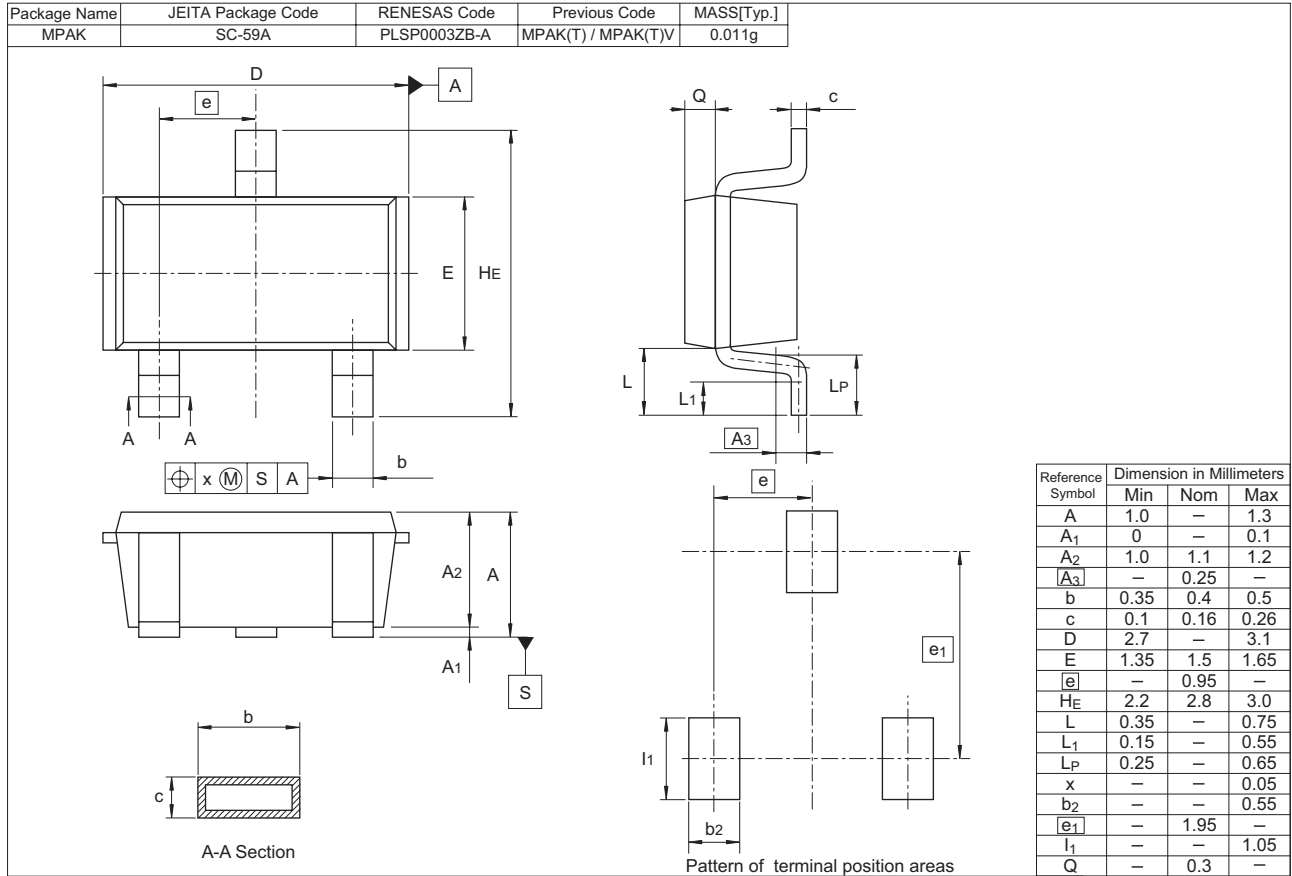
Switching Time Test Circuit



Switching Time Waveform



Package Dimensions



Ordering Information

Part No.	Quantity	Shipping Container
RQK2501YGDQATL-E	3000 pcs.	φ178 mm reel, 8 mm Emboss taping

Notes:

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