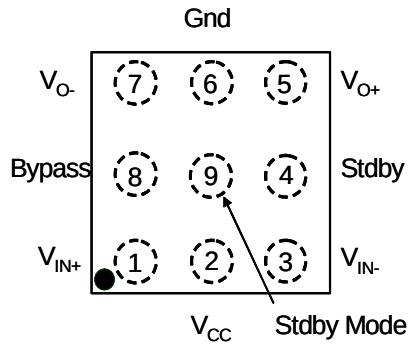
TS4994FC

1.2 W differential input/output audio power amplifier with selectable standby

Features

- Differential inputs
- Near-zero pop & click
- 100dB PSRR @ 217Hz with grounded inputs
- Operating range from V_{CC} = 2.5V to 5.5V
- 1.2W rail-to-rail output power @ V_{CC} = 5V, THD = 1%, F = 1kHz, with 8Ω load
- 90dB CMRR @ 217Hz
- Ultra-low consumption in standby mode (10nA)
- Selectable standby mode (active low or active high)
- Ultra fast startup time: 15ms typ.
- Available in 9-bump flip-chip (300mm bump diameter)
- Lead-free package

TS4994EIJT - Flip-chip (9 bumps)



Description

The TS4994 is an audio power amplifier capable of delivering 1W of continuous RMS output power into an 8Ω load @ 5V. Due to its differential inputs, it exhibits outstanding noise immunity.

An external standby mode control reduces the supply current to less than 10nA. An STBY MODE pin allows the standby to be active HIGH or LOW. An internal thermal shutdown protection is also provided, making the device capable of sustaining short-circuits.

The device is equipped with common mode feedback circuitry allowing outputs to be always biased at V_{CC}/2 regardless of the input common mode voltage.

The TS4994 is designed for high quality audio applications such as mobile phones and requires few external components.

Applications

- Mobile phones (cellular / cordless)
- Laptop / notebook computers
- PDAs
- Portable audio devices

Order codes

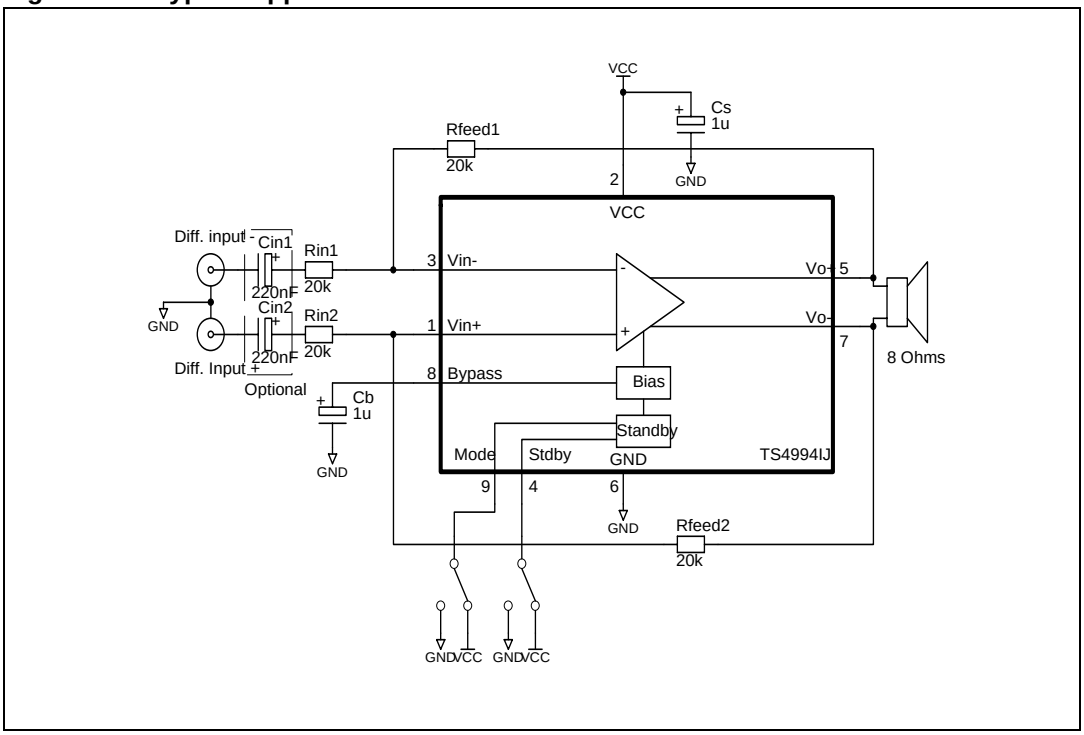
Part number	Temperature range	Package	Packaging	Marking
TS4994EIKJT	-40°C, +85°C	FC9 with back coating	Tape & reel	A94
TS4994EIJT		Lead free flip-chip9		A94

Contents

1 Application component information

Components	Functional description
C_s	Supply bypass capacitor that provides power supply filtering.
C_b	Bypass capacitor that provides half supply filtering.
R_{feed}	Feedback resistor that sets the closed loop gain in conjunction with R_{in} A_V = closed loop gain = R_{feed}/R_{in}.
R_{in}	Inverting input resistor that sets the closed loop gain in conjunction with R_{feed}.
C_{in}	Optional input capacitor making a high pass filter together with R_{in}. (F_{CL} = $1/(2\pi R_{in}C_{in})$.

Figure 1. Typical application



2 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (1)	6	V
V_i	Input voltage (2)	GND to V_{CC}	V
T_{oper}	Operating free air temperature range	-40 to + 85	°C
T_{stg}	Storage temperature	-65 to +150	°C
T_j	Maximum junction temperature	150	°C
R_{thja}	Thermal resistance junction to ambient (3)	250	°C/W
P_{diss}	Power dissipation	internally limited	W
ESD	Human body model	2	kV
	Machine model	200	V
	Latch-up immunity	200	mA
	Lead temperature (soldering, 10sec)	260	°C

1. All voltage values are measured with respect to the ground pin.
2. The magnitude of the input signal must never exceed V_{CC} + 0.3V / GND - 0.3V.
3. The device is protected by a thermal shutdown active at 150°C.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	2.5 to 5.5	V
V_{SM}	Standby mode voltage input: Standby active LOW Standby active HIGH	 V_{SM}=GND V_{SM}=V_{CC}	V
V_{STBY}	Standby voltage input: Device ON (V_{SM} = GND) or device OFF (V_{SM} = V_{CC}) Device OFF (V_{SM} = GND) or device ON (V_{SM} = V_{CC})	 $1.5 \leq V_{STBY} \leq V_{CC}$ $GND \leq V_{STBY} \leq 0.4$ (1)	V
T_{SD}	Thermal shutdown temperature	150	°C
R_L	Load resistor	≥ 4	Ω
R_{thja}	Thermal resistance junction to ambient	100	°C/W

1. The minimum current consumption (I_{STBY}) is guaranteed when V_{STBY} = GND or V_{CC} (i.e. supply rails) for the whole temperature range.

3 Electrical characteristics

Table 3. Electrical characteristics for V_{CC} = +5V, GND = 0V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current No input signal, no load		4	7	mA
I_{STBY}	Standby current No input signal, V_{STBY} = V_{SM} = GND, R_L = 8Ω No input signal, V_{STBY} = V_{SM} = V_{CC}, R_L = 8Ω		10	1000	nA
V_{oo}	Differential output offset voltage No input signal, R_L = 8Ω		0.1	10	mV
V_{ICM}	Input common mode voltage CMRR ≤ -60dB	0.6		V_{CC} - 0.9	V
P_{out}	Output power THD = 1% Max, F= 1kHz, R_L = 8Ω	0.8	1.2		W
THD + N	Total harmonic distortion + noise P_{out} = 850mW rms, A_V = 1, 20Hz ≤ F ≤ 20kHz, R_L = 8Ω		0.5		%
$PSRR_{IG}$	Power supply rejection ratio with inputs grounded(1) F = 217Hz, R = 8Ω, A_V = 1, C_{in} = 4.7µF, C_b =1µF V_{ripple} = 200mV_{PP}		100		dB
CMRR	Common mode rejection ratio F = 217Hz, R_L = 8Ω, A_V = 1, C_{in} = 4.7µF, C_b =1µF V_{ic} = 200mV_{PP}		90		dB
SNR	Signal-to-noise ratio (A-weighted filter, A_V = 2.5) R_L = 8Ω, THD +N < 0.7%, 20Hz ≤ F ≤ 20kHz		100		dB
GBP	Gain bandwidth product R_L = 8Ω		2		MHz
V_N	Output voltage noise, 20Hz ≤ F ≤ 20kHz, R_L = 8Ω Unweighted, A_V = 1 A-weighted, A_V = 1 Unweighted, A_V = 2.5 A-weighted, A_V = 2.5 Unweighted, A_V = 7.5 A-weighted, A_V = 7.5 Unweighted, Standby A-weighted, Standby		 6 5.5 12 10.5 33 28 1.5 1		µV_{RMS}
t_{WU}	Wake-up time(2) C_b =1µF		15		ms

1. Dynamic measurements - 20*log(rms(V_{out})/rms (V_{ripple})). V_{ripple} is the super-imposed sinus signal relative to V_{CC}.
2. Transition time from standby mode to fully operational amplifier.

Table 4. Electrical characteristics for V_{CC} = +3.3V (all electrical values are guaranteed with correlation measurements at 2.6V and 5V), GND = 0V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current no input signal, no load		3	7	mA
I_{STBY}	Standby current No input signal, V_{STBY} = V_{SM} = GND, R_L = 8Ω No input signal, V_{STBY} = V_{SM} = V_{CC}, R_L = 8Ω		10	1000	nA
V_{oo}	Differential output offset voltage No input signal, R_L = 8Ω		0.1	10	mV
V_{ICM}	Input common mode voltage CMRR ≤ -60dB	0.6		V_{CC} - 0.9	V
P_{out}	Output power THD = 1% max, F= 1kHz, R_L = 8Ω	300	500		mW
THD + N	Total harmonic distortion + noise P_{out} = 300mW rms, A_V = 1, 20Hz ≤ F ≤ 20kHz, R_L = 8Ω		0.5		%
$PSRR_{IG}$	Power supply rejection ratio with inputs grounded(1) F = 217Hz, R = 8Ω, A_V = 1, C_{in} = 4.7µF, C_b =1µF V_{ripple} = 200mV_{PP}		100		dB
CMRR	Common mode rejection ratio F = 217Hz, R_L = 8Ω, A_V = 1, C_{in} = 4.7µF, C_b =1µF V_{ic} = 200mV_{PP}		90		dB
SNR	Signal-to-noise ratio (A-weighted filter, A_V = 2.5) R_L = 8Ω, THD +N < 0.7%, 20Hz ≤ F ≤ 20kHz		100		dB
GBP	Gain bandwidth product R_L = 8Ω		2		MHz
V_N	Output voltage noise, 20Hz ≤ F ≤ 20kHz, R_L = 8Ω Unweighted, A_V = 1 A-weighted, A_V = 1 Unweighted, A_V = 2.5 A-weighted, A_V = 2.5 Unweighted, A_V = 7.5 A-weighted, A_V = 7.5 Unweighted, Standby A-weighted, Standby		 6 5.5 12 10.5 33 28 1.5 1		μV_{RMS}
t_{WU}	Wake-up time(2) C_b =1µF		15		ms

1. Dynamic measurements - 20*log(rms(V_{out})/rms (V_{ripple})). V_{ripple} is the super-imposed sinus signal relative to V_{CC}.
2. Transition time from standby mode to fully operational amplifier.

Table 5. Electrical characteristics for V_{CC} = +2.6V, GND = 0V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current No input signal, no load		3	7	mA
I_{STBY}	Standby current No input signal, V_{STBY} = V_{SM} = GND, R_L = 8Ω No input signal, V_{STBY} = V_{SM} = V_{CC}, R_L = 8Ω		10	1000	nA
V_{oo}	Differential output offset voltage No input signal, R_L = 8Ω		0.1	10	mV
V_{ICM}	Input common mode voltage CMRR ≤-60dB	0.6		V_{CC}- 0.9	V
P_{out}	Output power THD = 1% max, F= 1kHz, R_L = 8Ω	200	300		mW
THD + N	Total harmonic distortion + noise P_{out} = 225mW rms, A_V = 1, 20Hz ≤ F ≤ 20kHz, R_L = 8Ω		0.5		%
$PSRR_{IG}$	Power supply rejection ratio with inputs grounded(1) F = 217Hz, R = 8Ω, A_V = 1, C_{in} = 4.7µF, C_b =1µF V_{ripple} = 200mV_{PP}		100		dB
CMRR	Common mode rejection ratio F = 217Hz, R_L = 8Ω, A_V = 1, C_{in} = 4.7µF, C_b =1µF V_{ic} = 200mV_{PP}		90		dB
SNR	Signal-to-noise ratio (A-weighted filter, A_V = 2.5) R_L = 8Ω, THD +N < 0.7%, 20Hz ≤ F ≤ 20kHz		100		dB
GBP	Gain bandwidth product R_L = 8Ω		2		MHz
V_N	Output voltage noise, 20Hz ≤ F ≤ 20kHz, R_L = 8Ω Unweighted, A_V = 1 A-weighted, A_V = 1 Unweighted, A_V = 2.5 A-weighted, A_V = 2.5 Unweighted, A_V = 7.5 A-weighted, A_V = 7.5 Unweighted, Standby A-weighted, Standby		 6 5.5 12 10.5 33 28 1.5 1		μV_{RMS}
t_{WU}	Wake-up time(2) C_b =1µF		15		ms

1. Dynamic measurements - 20*log(rms(V_{out})/rms (V_{ripple})). V_{ripple} is the super-imposed sinus signal relative to V_{CC}.
2. Transition time from standby mode to fully operational amplifier.

Figure 2. Current consumption vs. power supply voltage

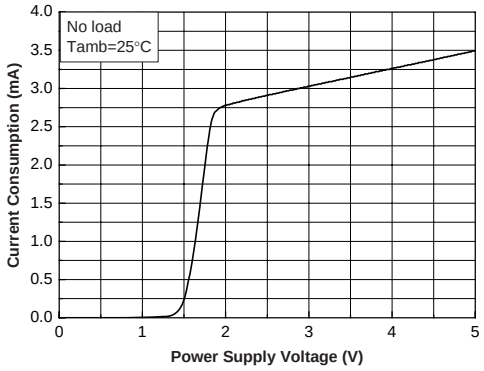


Figure 3. Current consumption vs. standby voltage

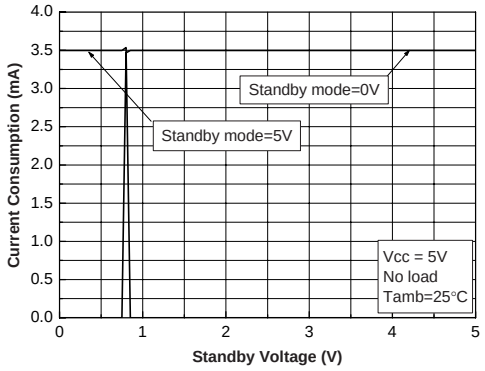


Figure 4. Current consumption vs. standby voltage

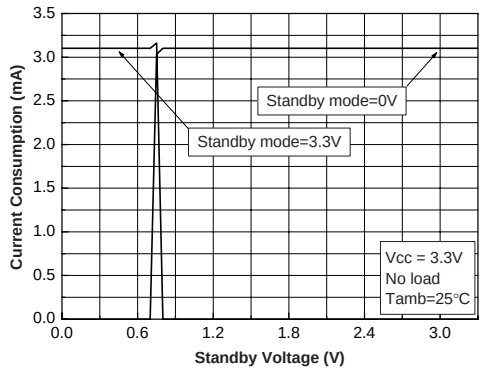


Figure 5. Current consumption vs. standby voltage

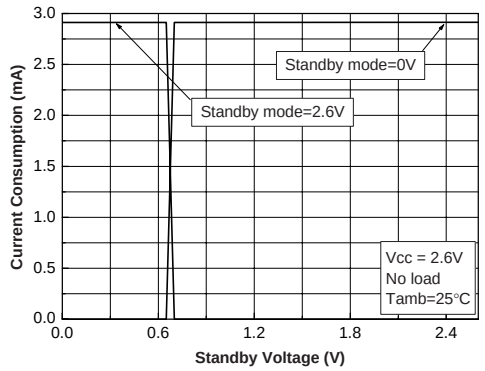


Figure 6. Differential DC output voltage vs. common mode input voltage

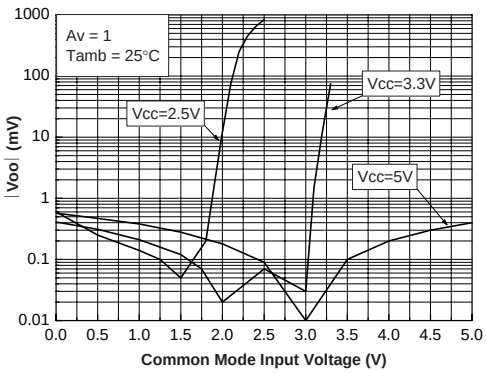


Figure 7. Power dissipation vs. output power

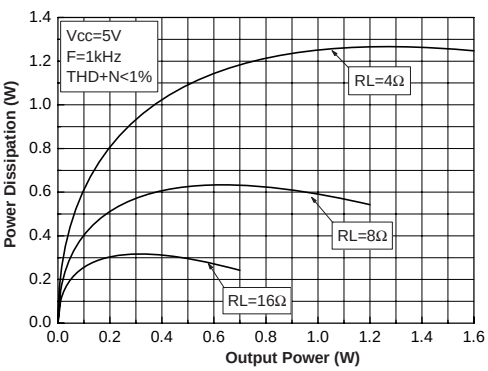


Figure 8. Power dissipation vs. output power

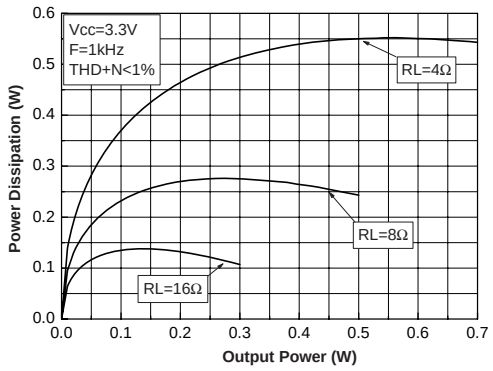


Figure 9. Power dissipation vs. output power

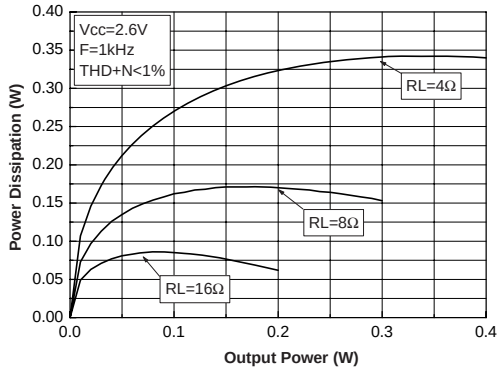


Figure 10. Output power vs. power supply voltage

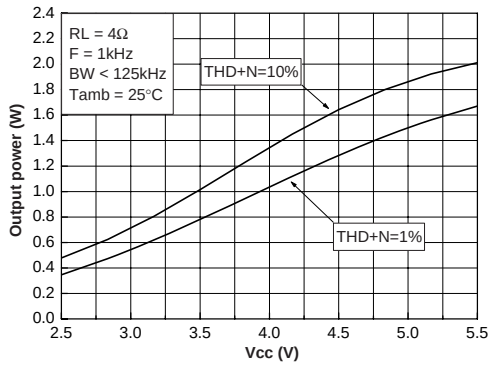


Figure 11. Output power vs. power supply voltage

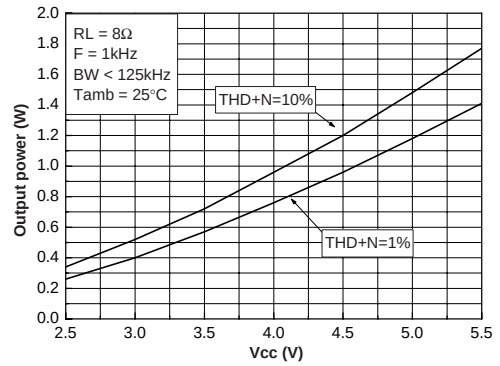


Figure 12. Output power vs. power supply voltage

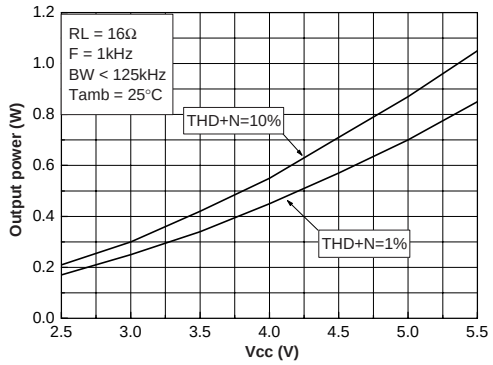


Figure 13. Output power vs. power supply voltage

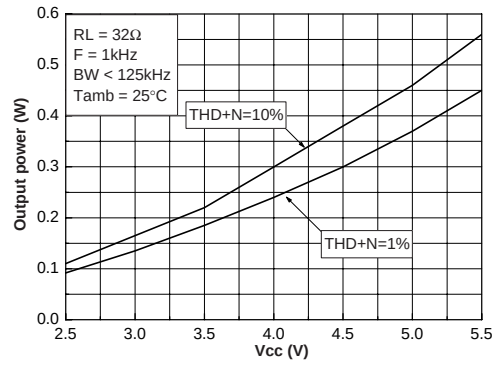


Figure 14. Power derating curves

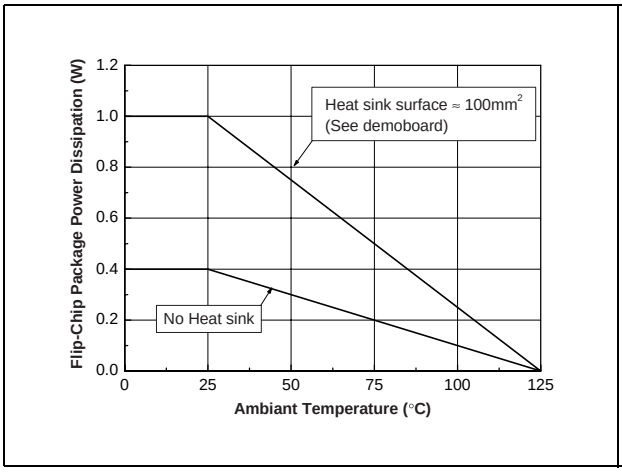


Figure 15. Open loop gain vs. frequency

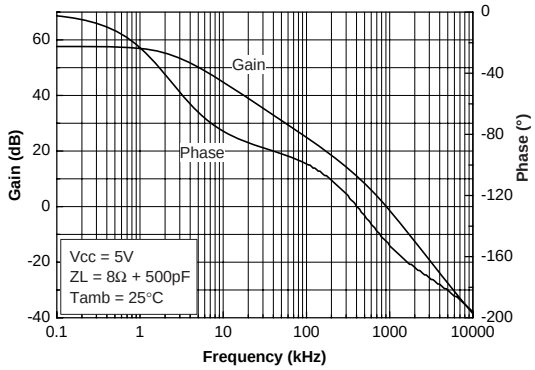


Figure 16. Open loop gain vs. frequency

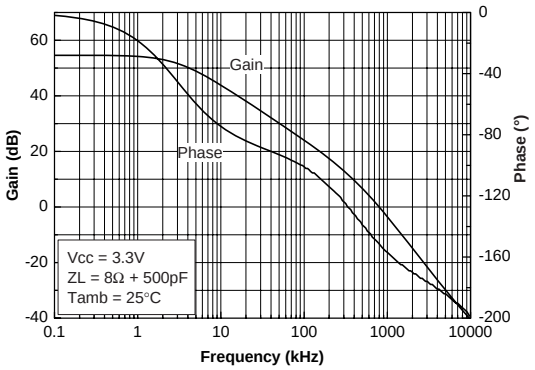


Figure 17. Open loop gain vs. frequency

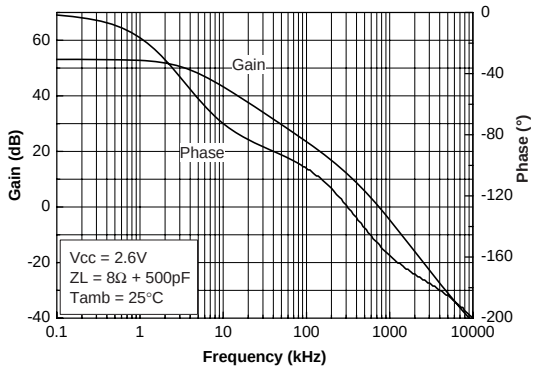


Figure 18. Closed loop gain vs. frequency

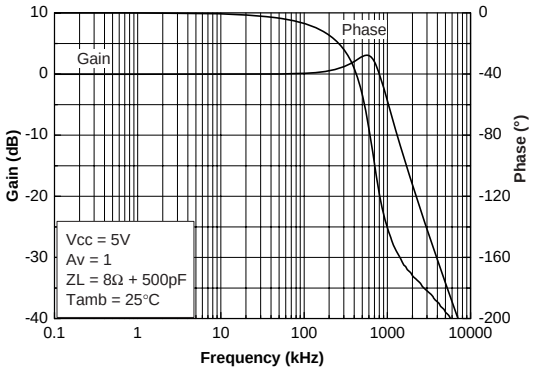


Figure 19. Closed loop gain vs. frequency

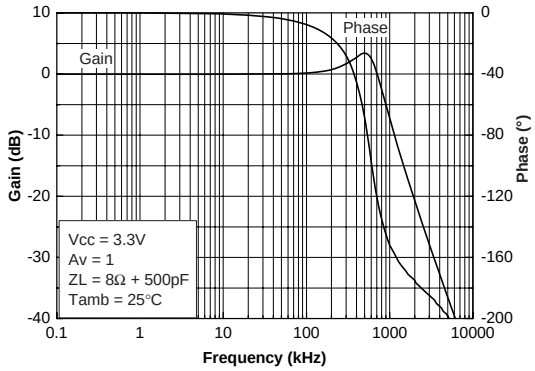


Figure 20. Closed loop gain vs. frequency

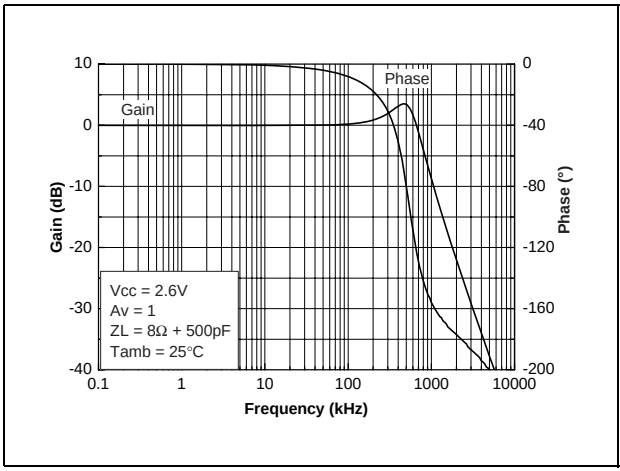


Figure 21. PSRR vs. frequency

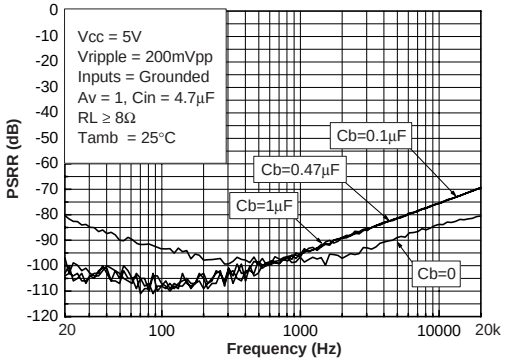


Figure 22. PSRR vs. frequency

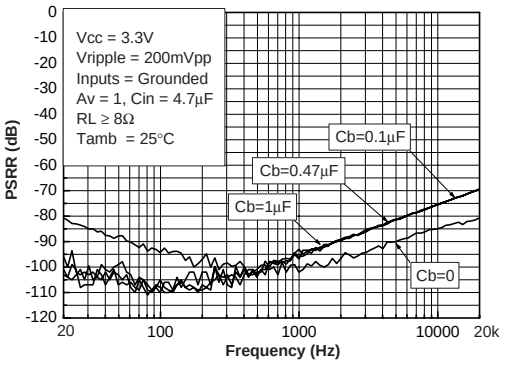


Figure 23. PSRR vs. frequency

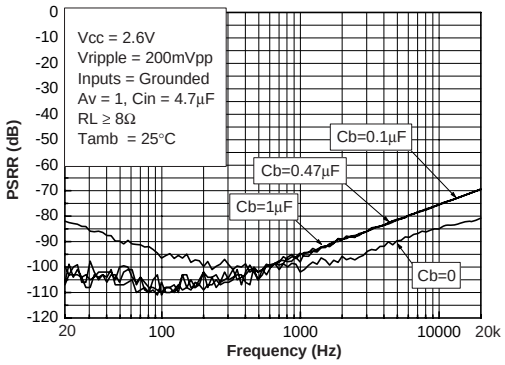


Figure 24. PSRR vs. frequency

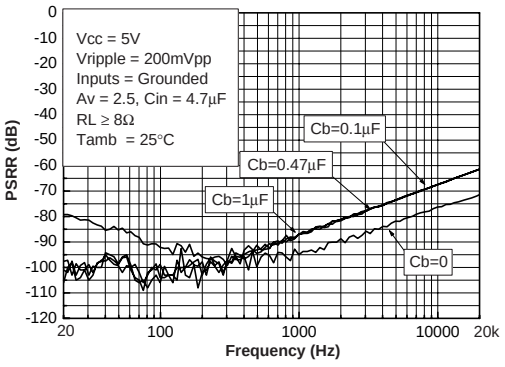


Figure 25. PSRR vs. frequency

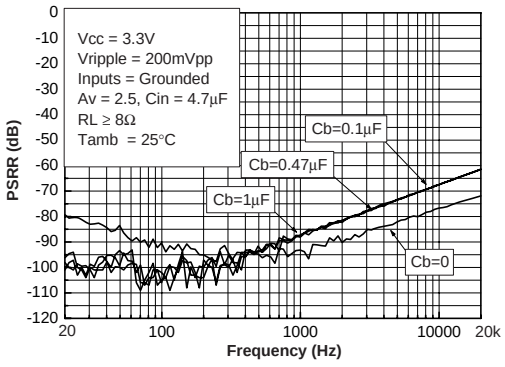


Figure 26. PSRR vs. frequency

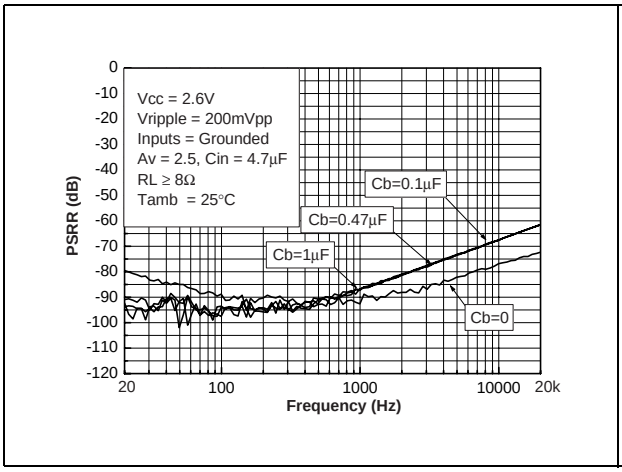


Figure 27. PSRR vs. frequency

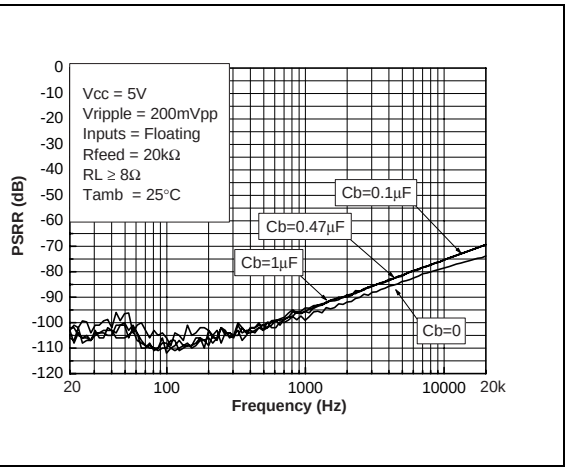


Figure 28. PSRR vs. frequency

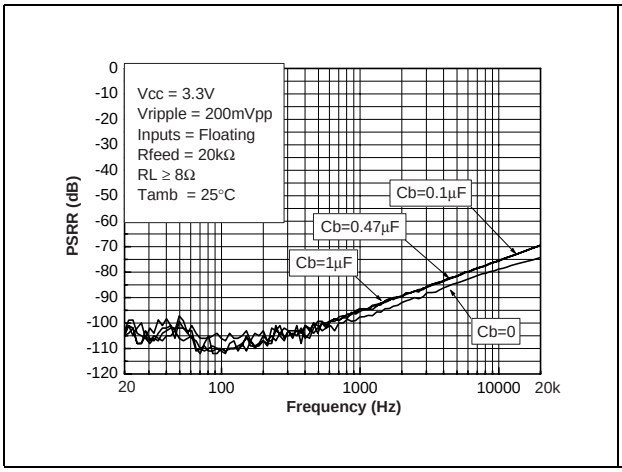


Figure 29. PSRR vs. frequency

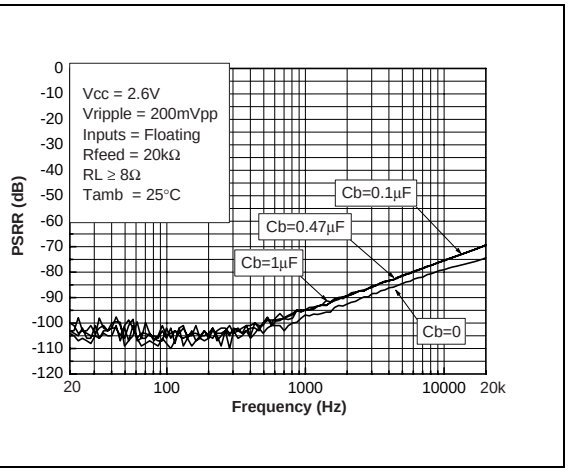


Figure 30. PSRR vs. common mode input voltage

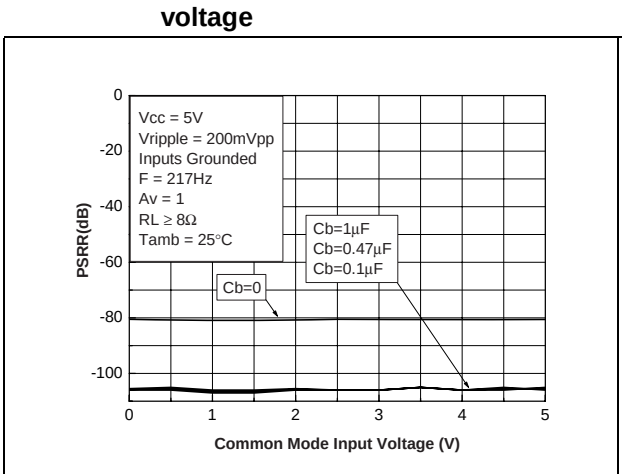


Figure 31. PSRR vs. common mode input voltage

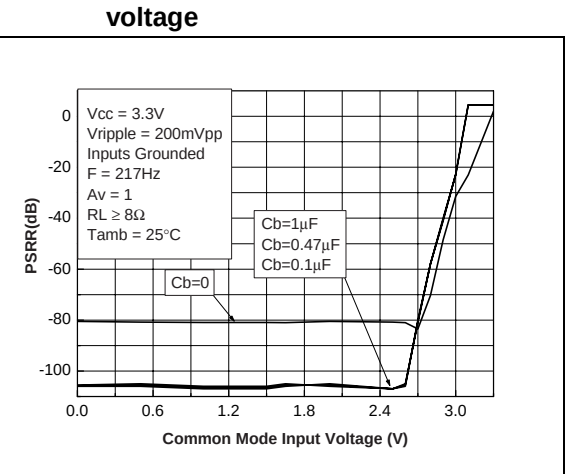


Figure 32. PSRR vs. common mode input voltage

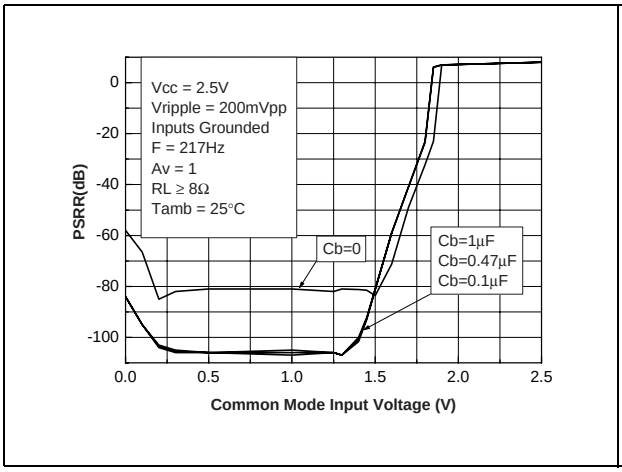


Figure 33. CMRR vs. frequency

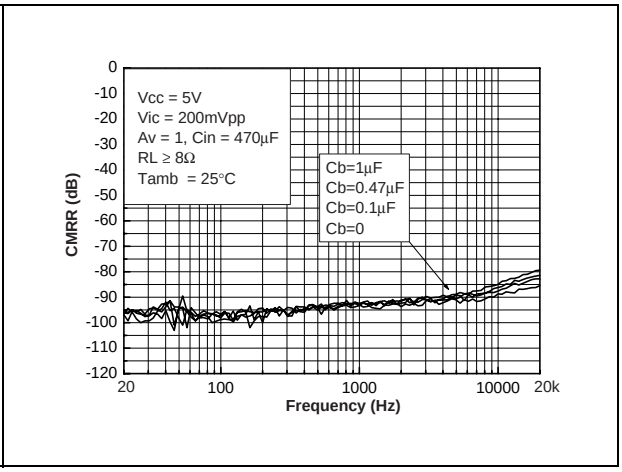


Figure 34. CMRR vs. frequency

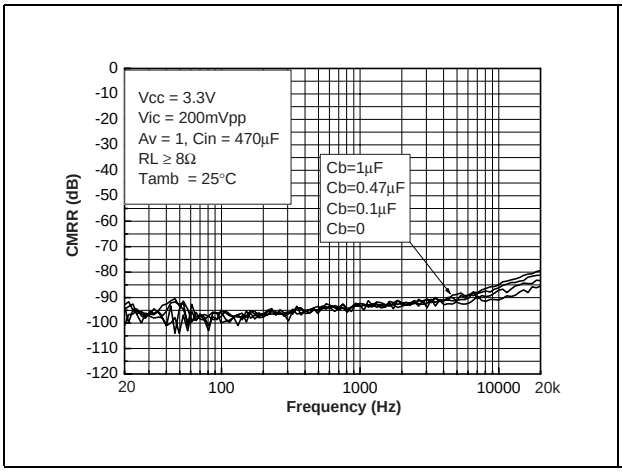


Figure 35. CMRR vs. frequency

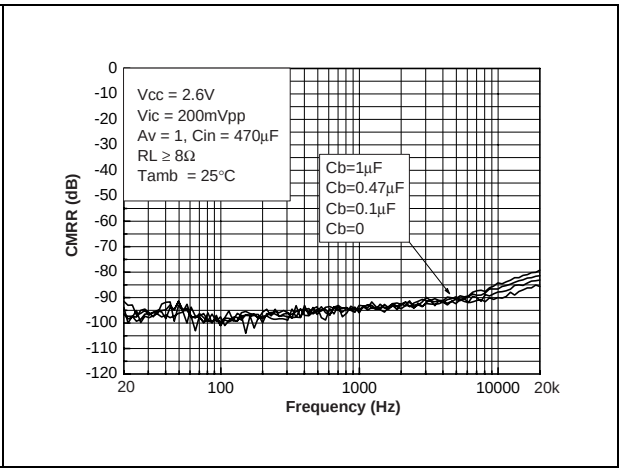


Figure 36. CMRR vs. frequency

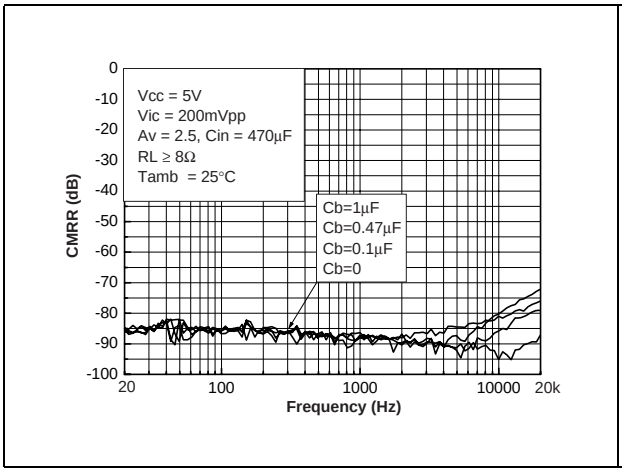


Figure 37. CMRR vs. frequency

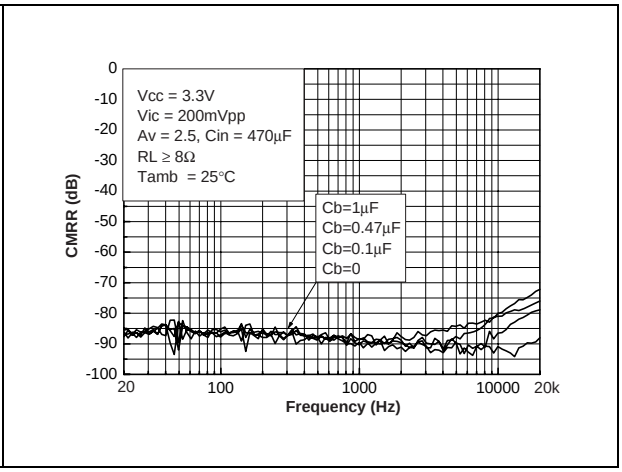


Figure 38. CMRR vs. frequency

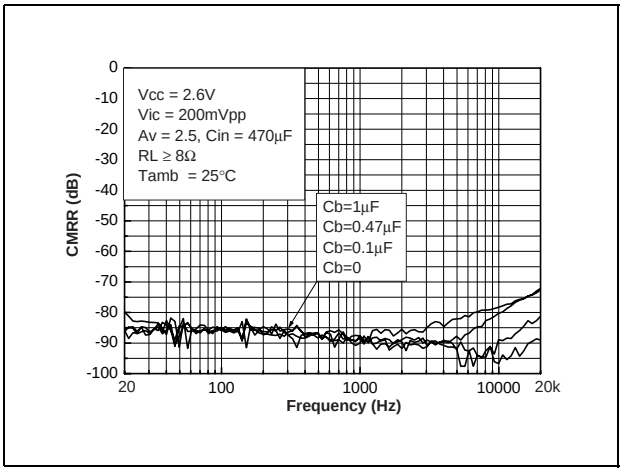


Figure 39. CMRR vs. common mode input voltage

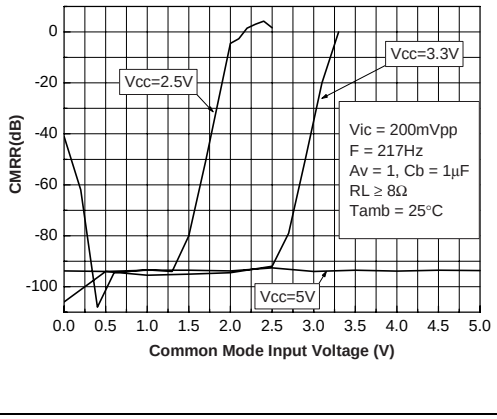


Figure 40. CMRR vs. common mode input voltage

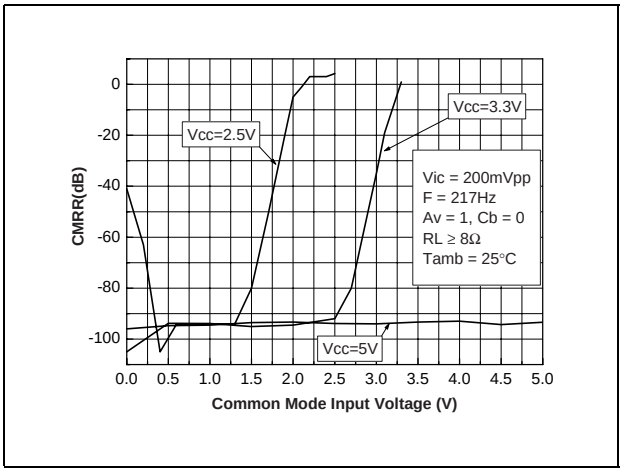


Figure 41. THD+N vs. output power

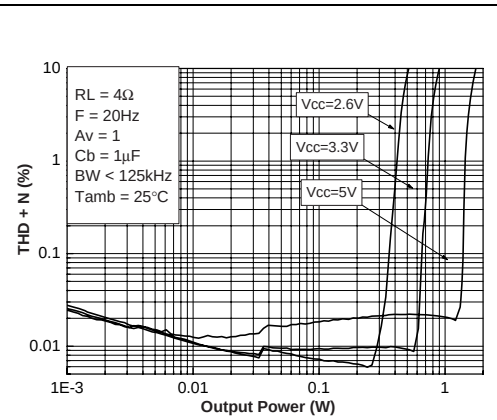


Figure 42. THD+N vs. output power

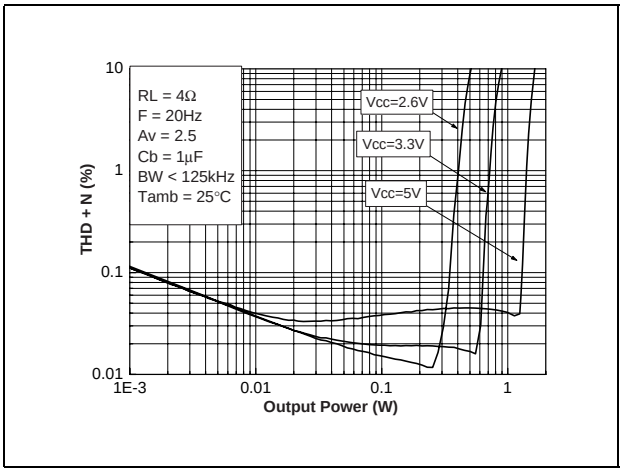


Figure 43. THD+N vs. output power

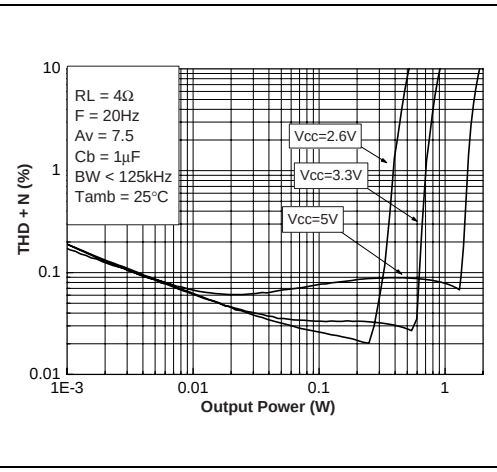


Figure 44. THD+N vs. output power

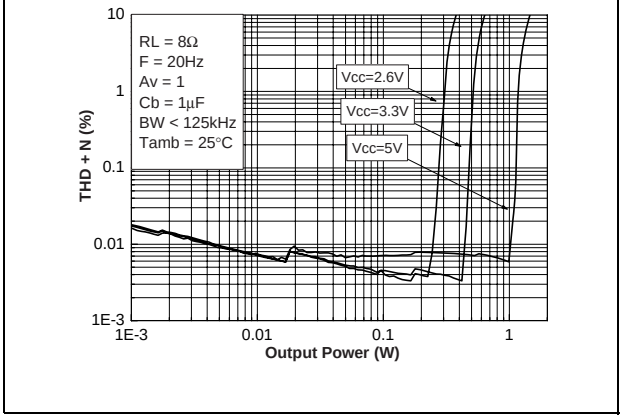


Figure 45. THD+N vs. output power

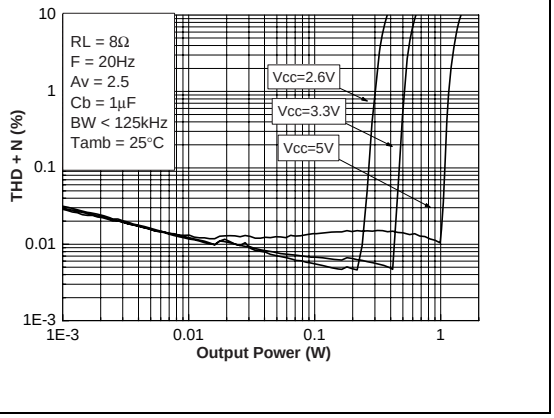


Figure 46. THD+N vs. output power

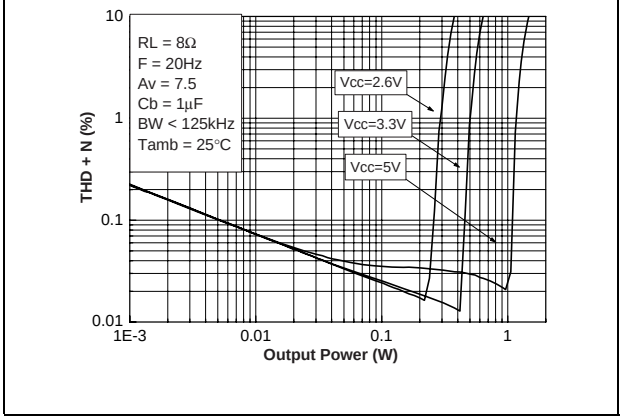


Figure 47. THD+N vs. output power

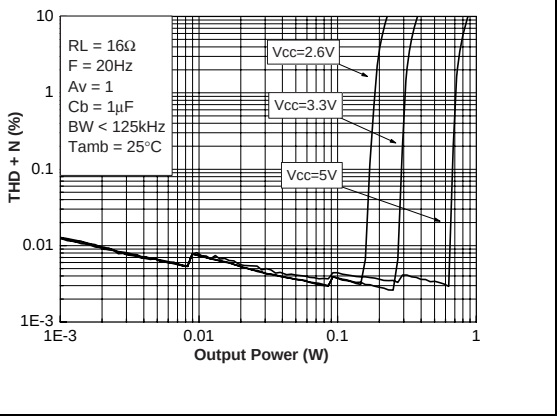


Figure 48. THD+N vs. output power

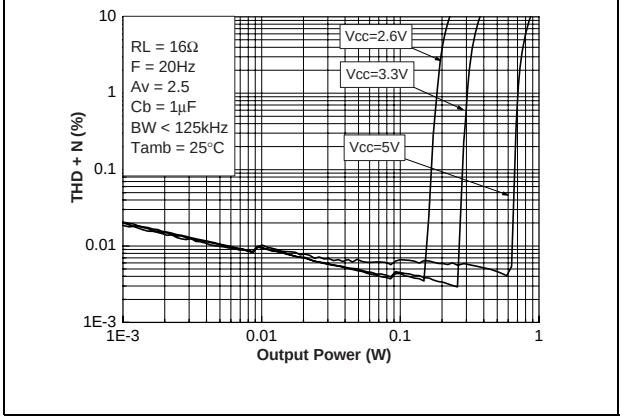


Figure 49. THD+N vs. output power

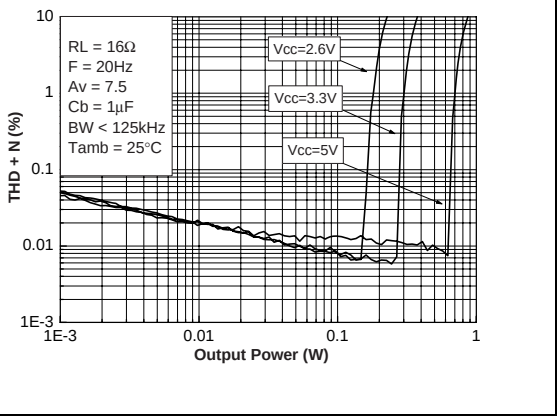


Figure 50. THD+N vs. output power

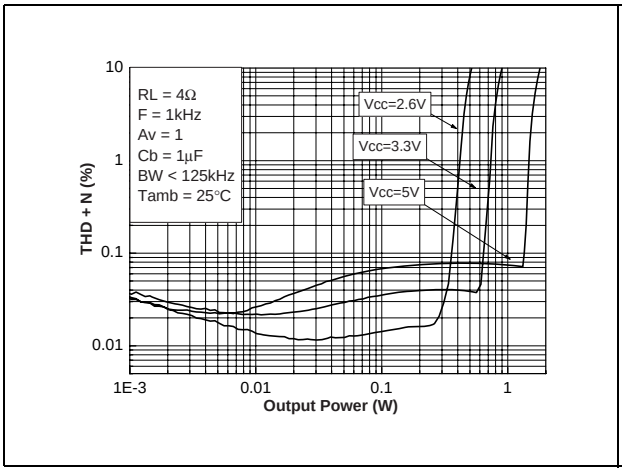


Figure 51. THD+N vs. output power

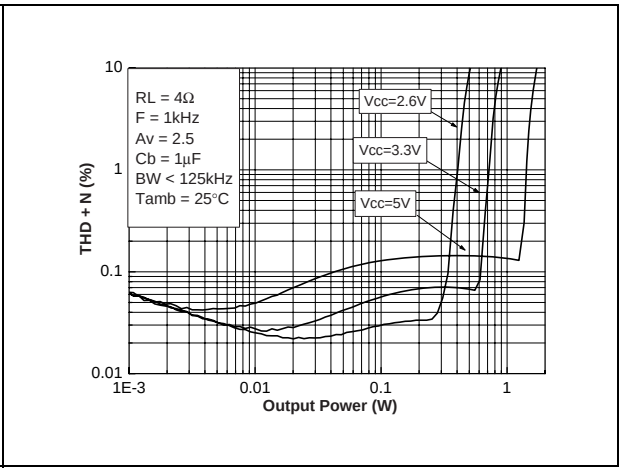


Figure 52. THD+N vs. output power

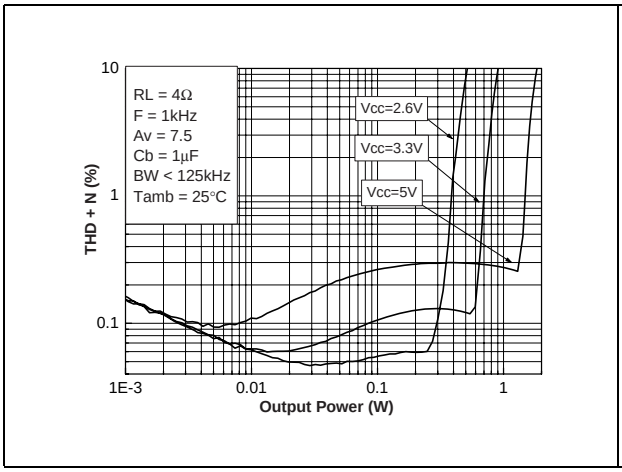


Figure 53. THD+N vs. output power

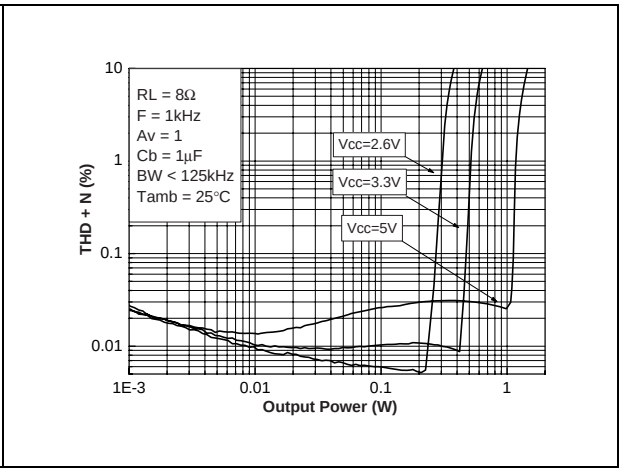


Figure 54. THD+N vs. output power

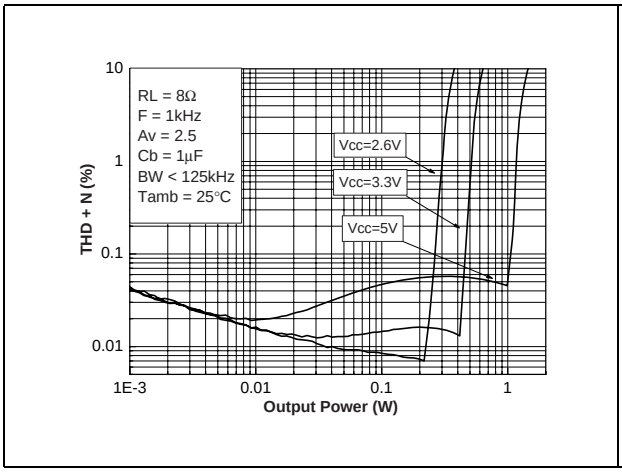


Figure 55. THD+N vs. output power

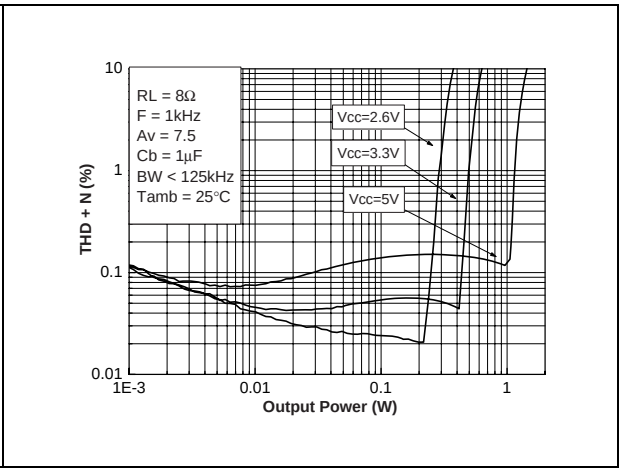


Figure 56. THD+N vs. output power

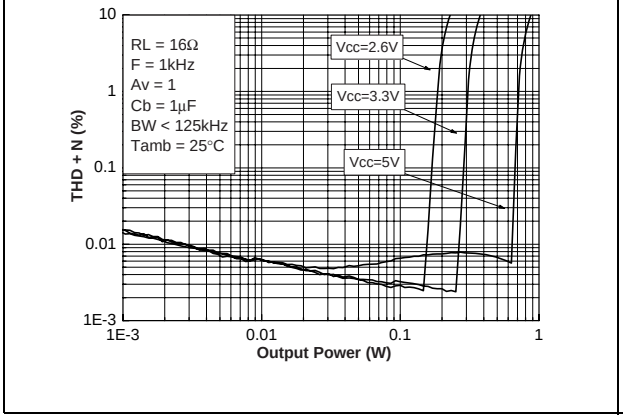


Figure 57. THD+N vs. output power

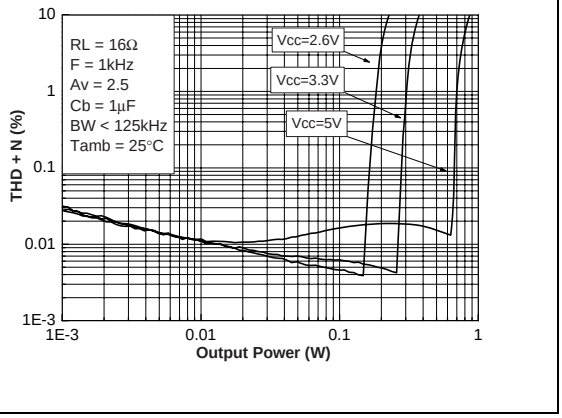


Figure 58. THD+N vs. output power

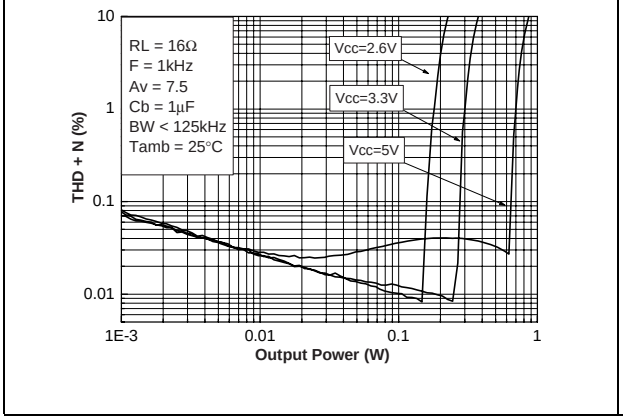


Figure 59. THD+N vs. output power

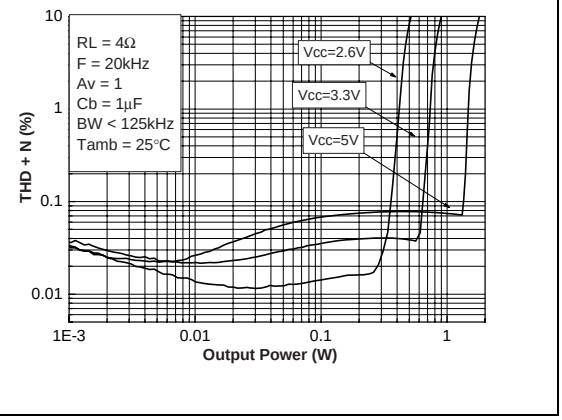


Figure 60. THD+N vs. output power

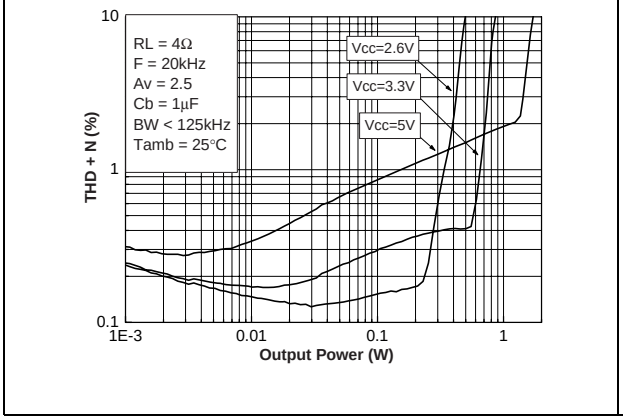


Figure 61. THD+N vs. output power

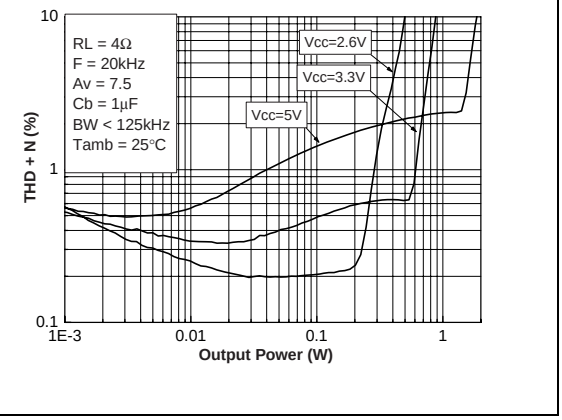


Figure 62. THD+N vs. output power

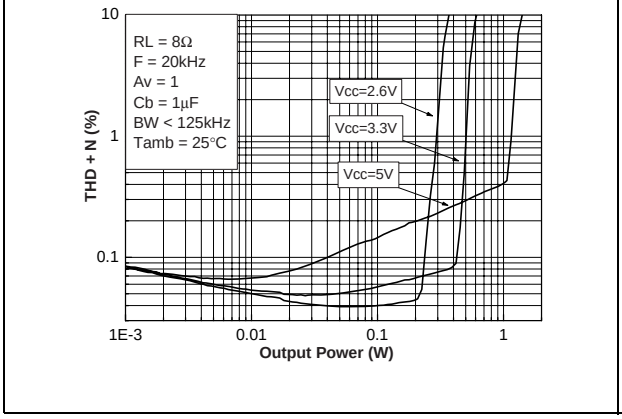


Figure 63. THD+N vs. output power

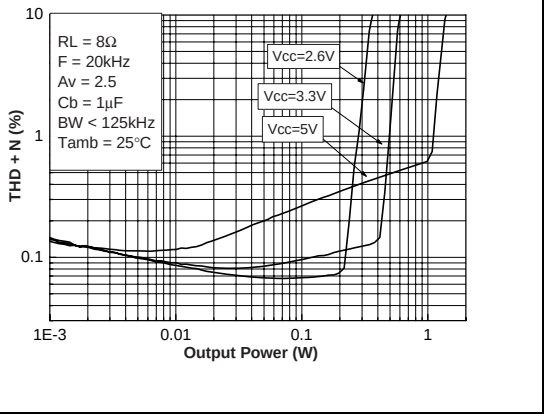


Figure 64. THD+N vs. output power

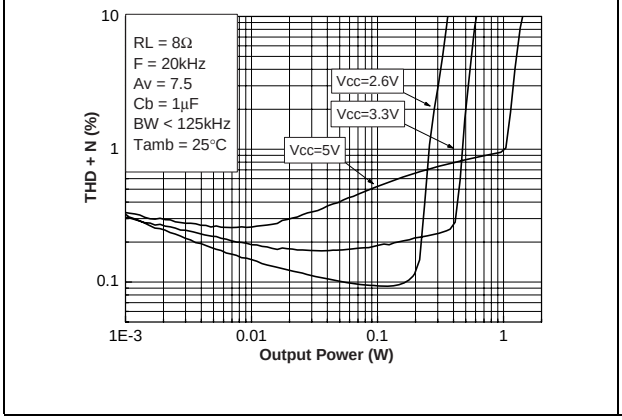


Figure 65. THD+N vs. output power

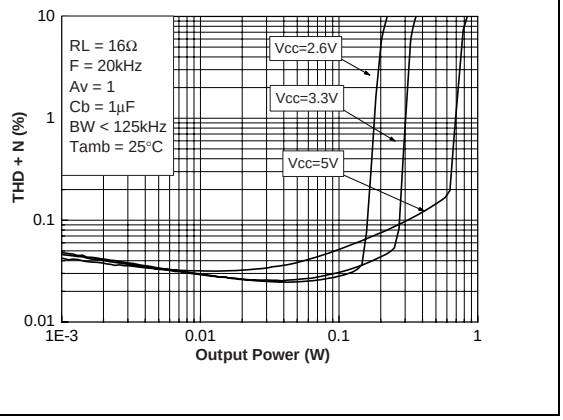


Figure 66. THD+N vs. output power

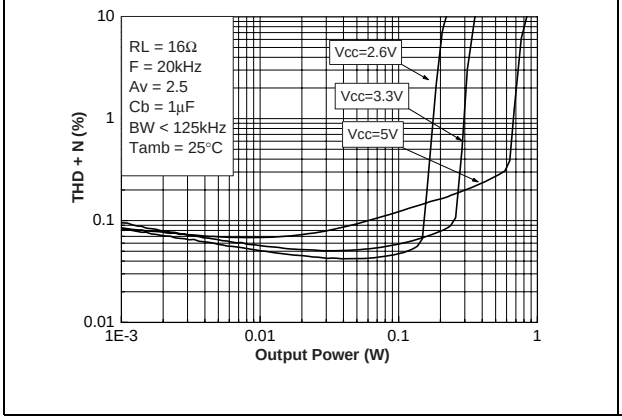


Figure 67. THD+N vs. output power

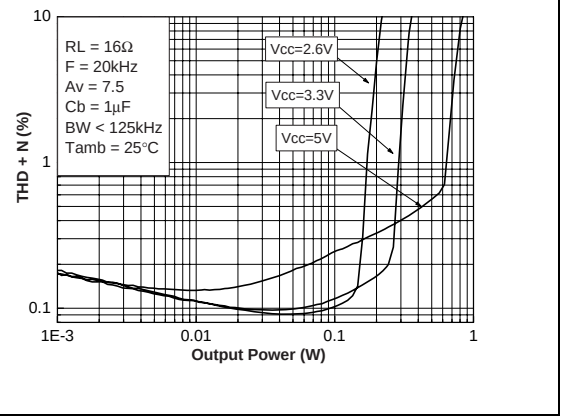


Figure 68. THD+N vs. frequency

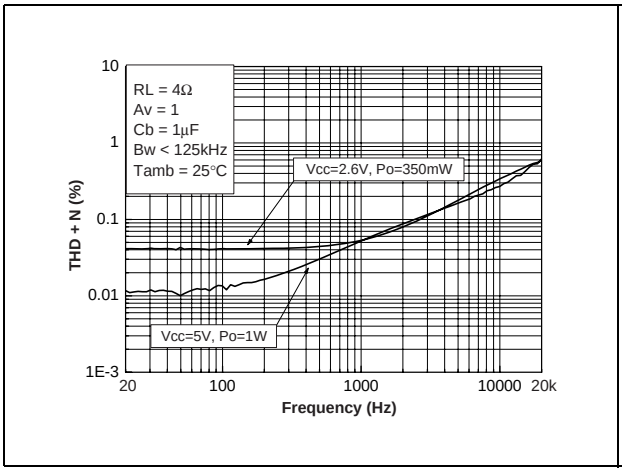


Figure 69. THD+N vs. frequency

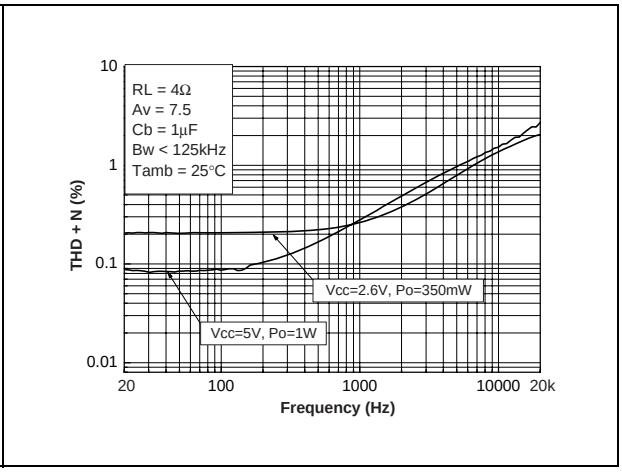


Figure 70. THD+N vs. frequency

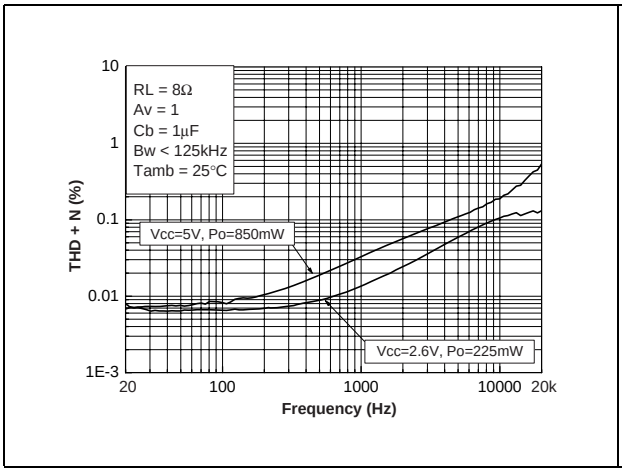


Figure 71. THD+N vs. frequency

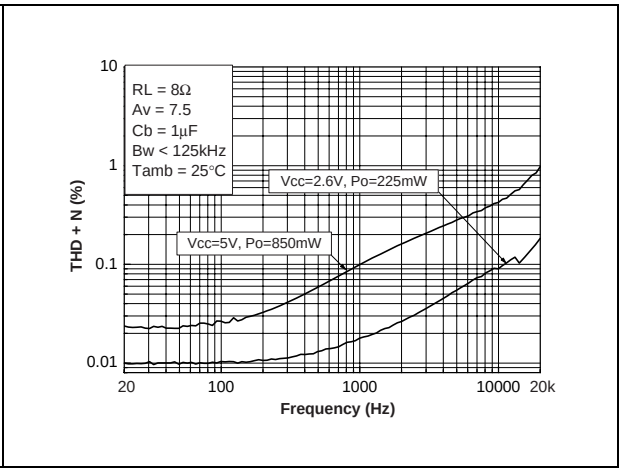


Figure 72. THD+N vs. frequency

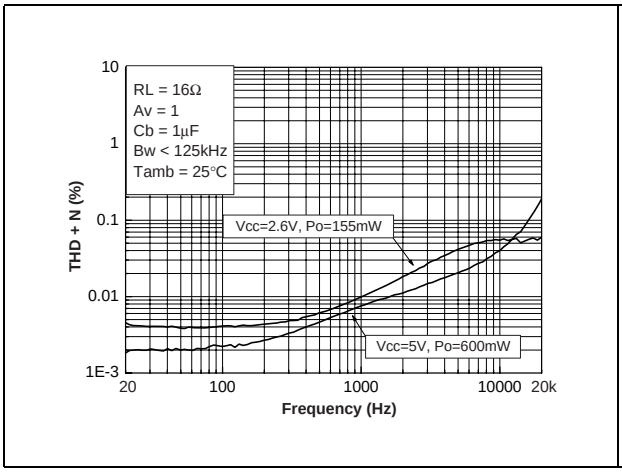


Figure 73. THD+N vs. frequency

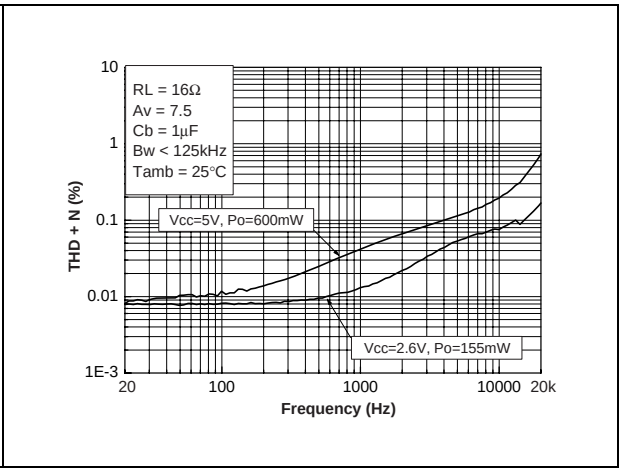


Figure 74. THD+N vs. output power

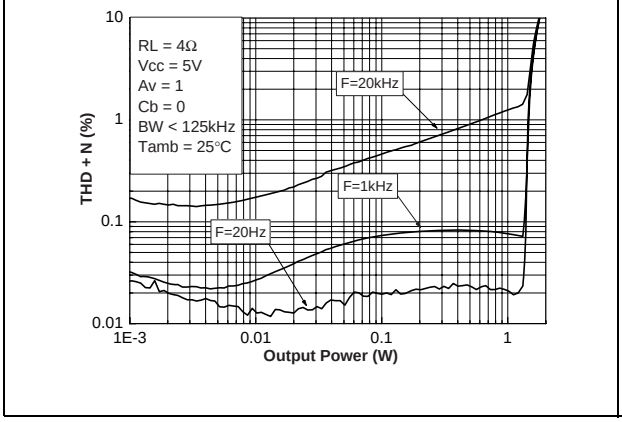


Figure 75. THD+N vs. output power

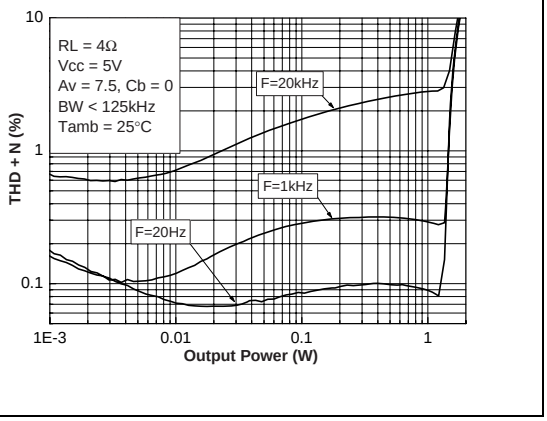


Figure 76. THD+N vs. output power

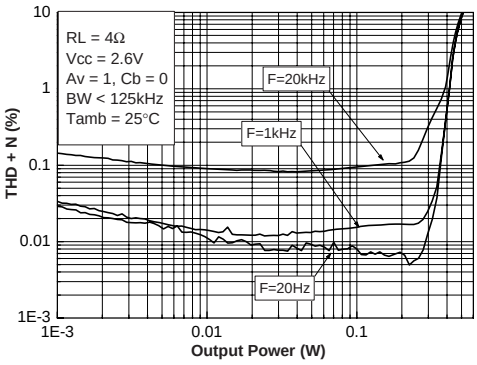


Figure 77. THD+N vs. output power

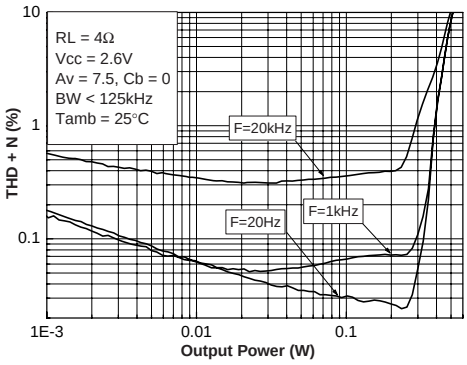


Figure 78. THD+N vs. output power

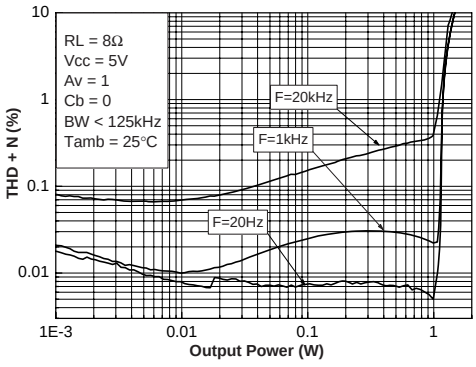


Figure 79. THD+N vs. output power

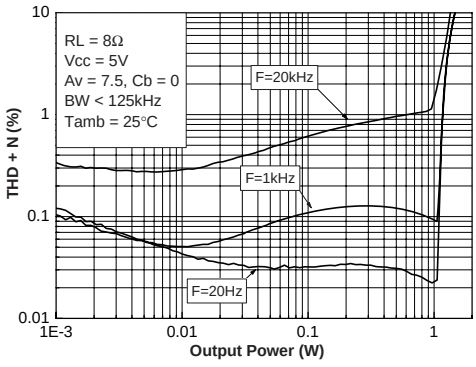


Figure 80. THD+N vs. output power

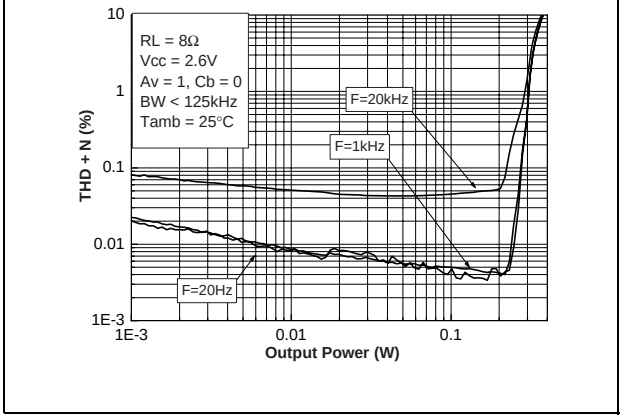


Figure 81. THD+N vs. output power

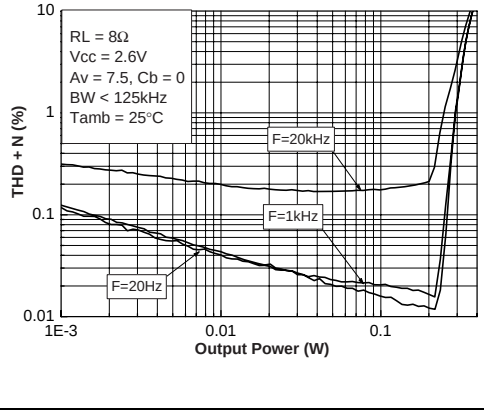


Figure 82. THD+N vs. output power

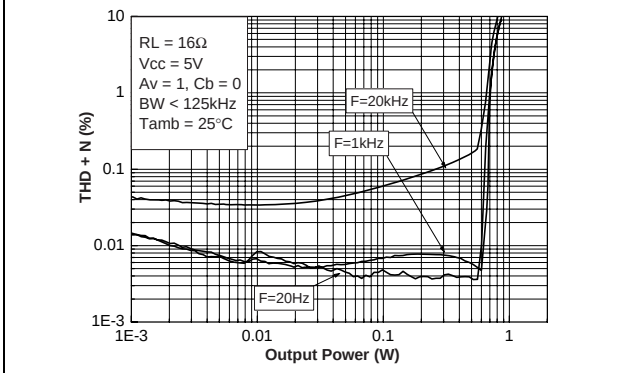


Figure 83. THD+N vs. output power

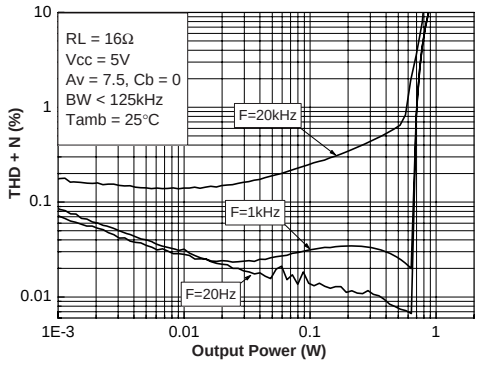


Figure 84. THD+N vs. output power

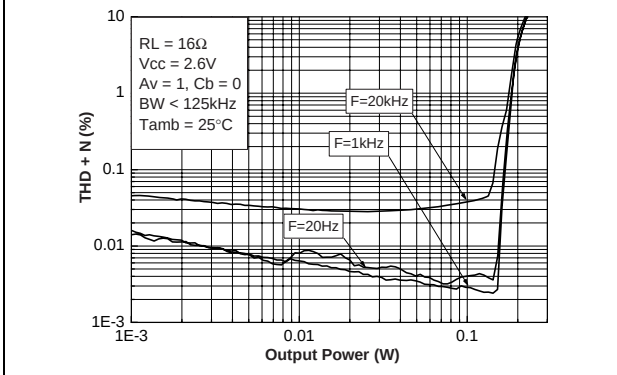


Figure 85. THD+N vs. output power

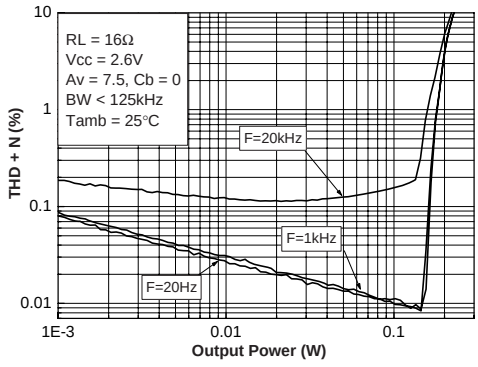


Figure 86. SNR vs. power supply voltage with unweighted filter

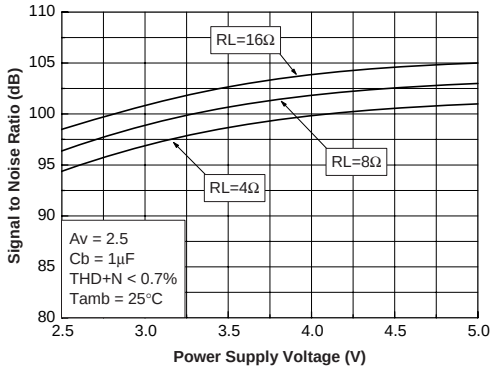


Figure 87. SNR vs. power supply voltage with A-weighted filter

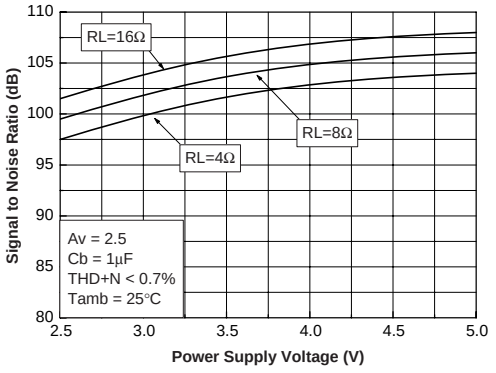
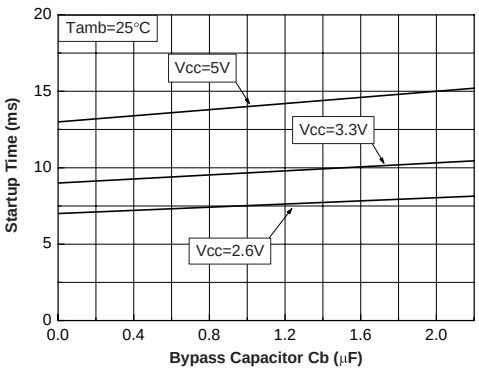


Figure 88. Startup time vs. bypass capacitor



4 Application information

4.1 Differential configuration principle

The TS4994 is a monolithic full-differential input/output power amplifier. The TS4994 also includes a common mode feedback loop that controls the output bias value to average it at $V_{CC}/2$ for any DC common mode input voltage. This allows the device to always have a maximum output voltage swing, and by consequence, maximize the output power. Moreover, as the load is connected differentially, compared to a single-ended topology, the output is four times higher for the same power supply voltage.

The **advantages** of a full-differential amplifier are:

- Very high PSRR (power supply rejection ratio).
- High common mode noise rejection.
- Virtually zero pop without additional circuitry, giving a faster start-up time compared with conventional single-ended input amplifiers.
- Easier interfacing with differential output audio DAC.
- No input coupling capacitors required due to common mode feedback loop.
- In theory, the filtering of the internal bias by an external bypass capacitor is not necessary. But, to reach maximum performance in all tolerance situations, it is better to keep this option.

The main **disadvantage** is:

- As the differential function is directly linked to the mismatch between external resistors, paying particular attention to this mismatch is mandatory in order to get the best performance from the amplifier.

4.2 Gain in typical application schematic

A typical differential application is shown in *Figure 1 on page 3*.

In the flat region of the frequency-response curve (no C_{in} effect), the differential gain is expressed by the relation:

$$A_{V_{diff}} = \frac{V_{O+} - V_O}{Diff_{input+} - Diff_{input-}} = \frac{R_{feed}}{R_{in}}$$

where $R_{in} = R_{in1} = R_{in2}$ and $R_{feed} = R_{feed1} = R_{feed2}$.

Note: For the rest of this section, Av_{diff} will be called A_V to simplify the expression.

4.3 Common mode feedback loop limitations

As explained previously, the common mode feedback loop allows the output DC bias voltage to be averaged at $V_{CC}/2$ for any DC common mode bias input voltage.

However, due to V_{ICM} limitation of the input stage (see *Table 3 on page 5*), the common mode feedback loop can play its role only within a defined range. This range depends upon

the values of V_{CC}, R_{in} and R_{feed} (A_V). To have a good estimation of the V_{ICM} value, use the following formula:

$$V_{ICM} = \frac{V_{CC} \times R_{in} + 2 \times V_{ic} \times R_{feed}}{2 \times (R_{in} + R_{feed})} \quad (V)$$

with

$$V_{ic} = \frac{Diff_{input+} + Diff_{input-}}{2} \quad (V)$$

The result of the calculation must be in the range:

$$0.6V \leq V_{ICM} \leq V_{CC} - 0.9V$$

If the result of the V_{ICM} calculation is not in this range, an input coupling capacitor must be used.

Example: With V_{CC}=2.5V, R_{in} = R_{feed} = 20k and V_{ic} = 2V, we find V_{ICM} = 1.63V. This is higher than 2.5V - 0.9V = 1.6V, so input coupling capacitors are required. Alternatively, you can change the V_{ic} value.

4.4 Low and high frequency response

In the low frequency region, C_{in} starts to have an effect. C_{in} forms, with R_{in}, a high-pass filter with a -3dB cut-off frequency. F_{CL} is in Hz.

$$F_{CL} = \frac{1}{2 \times \pi \times R_{in} \times C_{in}} \quad (Hz)$$

In the high-frequency region, you can limit the bandwidth by adding a capacitor (C_{feed}) in parallel with R_{feed}. It forms a low-pass filter with a -3dB cut-off frequency. F_{CH} is in Hz.

$$F_{CH} = \frac{1}{2 \times \pi \times R_{feed} \times C_{feed}} \quad (Hz)$$

While these bandwidth limitations are in theory attractive, in practice, because of low performance in terms of capacitor precision (and by consequence in terms of mismatching), they deteriorate the values of PSRR and CMRR.

The influence of mismatching on PSRR and CMRR performance is discussed in more detail in the following sections.

Example: A typical application with input coupling and feedback capacitor with F_{CL} = 50Hz and F_{CH} = 8kHz. We assume that the mismatching between $R_{in1,2}$ and $C_{feed1,2}$ can be neglected. If we sweep the frequency from DC to 20kHz we observe the following with respect to the PSRR value:

- From DC to 200Hz, the C_{in} impedance decreases from infinite to a finite value and the C_{feed} impedance is high enough to be neglected. Due to the tolerance of $C_{in1,2}$, we

must introduce a mismatch factor (R_{in1} x C_{in} ≠ R_{in2} x C_{in2}) that will decrease the PSRR performance.

- From 200Hz to 5kHz, the C_{in} impedance is low enough to be neglected when compared with $R_{in,}$ and the C_{feed} impedance is high enough to be neglected as well. In this range, we can reach the PSRR performance of the TS4994 itself.
- From 5kHz to 20kHz, the C_{in} impedance is low to be neglected when compared to $R_{in,}$ and the C_{feed} impedance decreases to a finite value. Due to tolerance of $C_{feed1,2}$, we introduce a mismatching factor (R_{feed1} x C_{feed1} ≠ R_{feed2} x C_{feed2}) that will decrease the PSRR performance.

4.5 Calculating the influence of mismatching on PSRR performance

For calculating PSRR performance, we consider that C_{in} and C_{feed} have no influence. We use the same kind of resistor (same tolerance) and ΔR is the tolerance value in %.

The following PSRR equation is valid for frequencies ranging from DC to about 1kHz.

The PSRR equation is (ΔR in %):

$$PSRR \leq 20 \times Log\left[\frac{\Delta R \times 100}{(10000 - \Delta R^2)}\right] \quad (dB)$$

This equation doesn't include the additional performance provided by bypass capacitor filtering. If a bypass capacitor is added, it acts, together with the internal high output impedance bias, as a low-pass filter, and the result is a quite important PSRR improvement with a relatively small bypass capacitor.

The complete PSRR equation (ΔR in %, C_b in microFarad and F in Hz) is:

$$PSRR \leq 20 \times \log\left[\frac{\Delta R \times 100}{(1000 - \Delta R^2) \times \sqrt{1 + F^2 \times C_b{}^2 \times 22.2}}\right] (dB)$$

Example: With ΔR = 0.1% and C_b = 0, the minimum PSRR is -60dB. With a 100nF bypass capacitor, at 100Hz the new PSRR would be -93dB.

This example is a worst case scenario, where each resistor has extreme tolerance. It illustrates the fact that with only a small bypass capacitor, the TS4994 provides high PSRR performance.

Note also that this is a theoretical formula. Because the TS4994 has self-generated noise, you should consider that the highest practical PSRR reachable is about -110dB. It is therefore unreasonable to target a -120dB PSRR.

The three following graphs show PSRR versus frequency and versus bypass capacitor C_b in worst-case conditions (ΔR = 0.1%).

Figure 89. PSRR vs. frequency (worst case conditions)

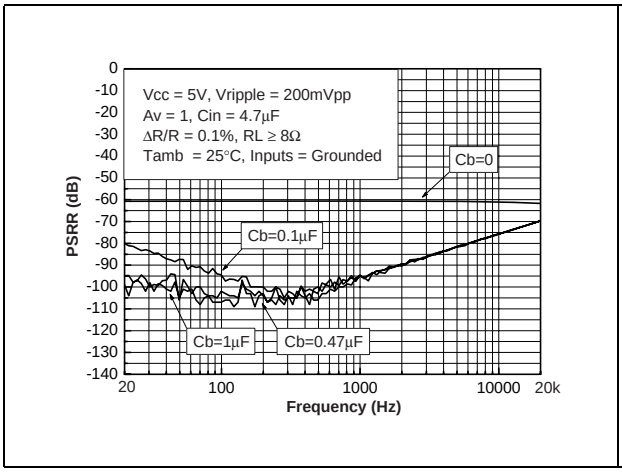


Figure 90. PSRR vs. frequency (worst case conditions)

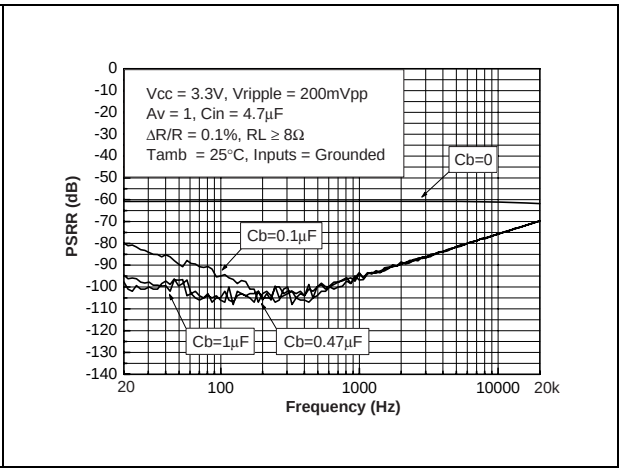
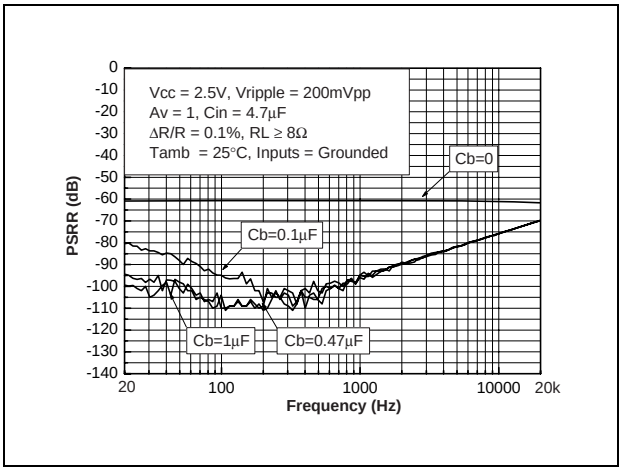


Figure 91. PSRR vs. frequency (worst case conditions)



The two following graphs show typical applications of the TS4994 with a random selection of four ⊿R/R values with a 0.1% tolerance.

Figure 92. PSRR vs. frequency with random choice condition

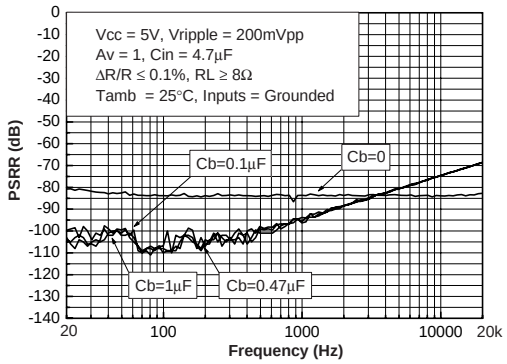
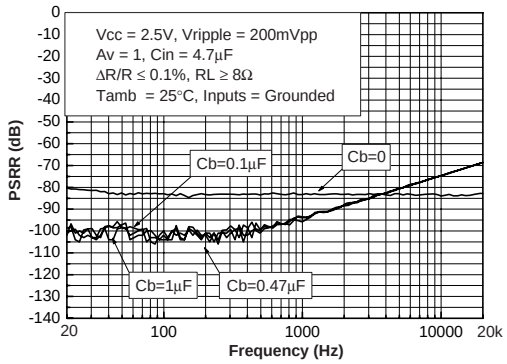


Figure 93. PSRR vs. frequency with random choice condition



4.6 CMRR performance

For calculating CMRR performance, we consider that C_{in} and C_{feed} have no influence. C_b has no influence in the calculation of the CMRR.

We use the same kind of resistor (same tolerance) and ΔR is the tolerance value in %.

The following CMRR equation is valid for frequencies ranging from DC to about 1kHz.

The CMRR equation is (ΔR in %):

$$CMRR \leq 20 \times Log\left[\frac{\Delta R \times 200}{(10000 - \Delta R^2)}\right] \quad (dB)$$

Example: With ΔR = 1%, the minimum CMRR is -34dB.

This example is a worst case scenario where each resistor has extreme tolerance. Ut illustrates the fact that for CMRR, good matching is essential.

As with the PSRR, due to self-generated noise, the TS4994 CMRR limitation is about -110dB.

Figure 94 and *Figure 95* show CMRR versus frequency and versus bypass capacitor C_b in worst-case conditions (ΔR=0.1%).

Figure 94. CMRR vs. frequency (worst case conditions)

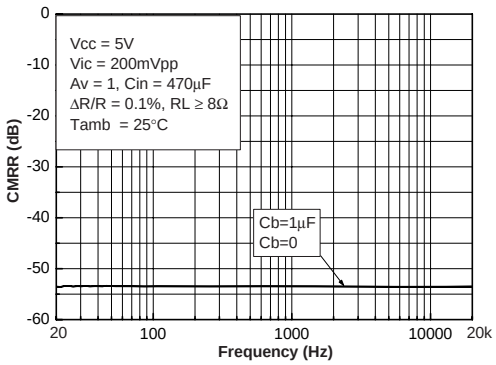


Figure 95. CMRR vs. frequency (worst case conditions)

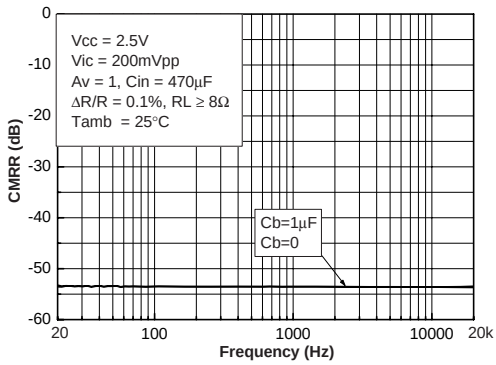


Figure 96 and *Figure 97* show CMRR versus frequency for a typical application with a random selection of four ⊿R/R values with a 0.1% tolerance.

Figure 96. CMRR vs. frequency with random selection condition

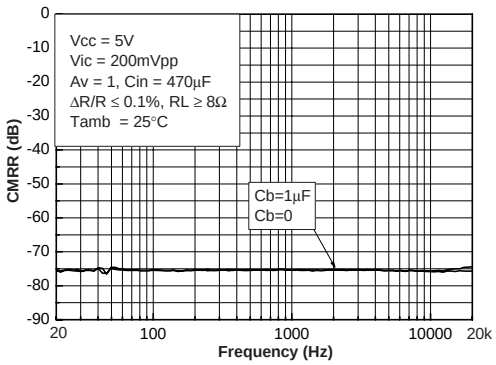
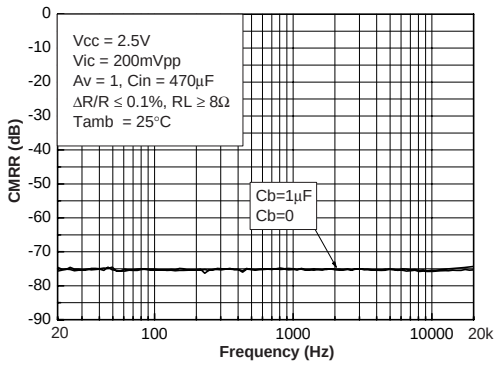


Figure 97. CMRR vs. frequency with random selection condition



4.7 Power dissipation and efficiency

Assumptions:

- Load voltage and current are sinusoidal (V_{out} and I_{out})
- Supply voltage is a pure DC source (V_{CC})

The output voltage is:

$$V_{out} = V_{peak} \sin\omega t \text{ (V)}$$

and

$$I_{out} = \frac{V_{out}}{R_L} \text{ (A)}$$

and

$$P_{out} = \frac{V_{peak}^2}{2R_L} \text{ (W)}$$

Therefore, the average current delivered by the supply voltage is:

Equation 1

$$I_{CC\ AVG} = 2\frac{V_{peak}}{\pi R_L} \text{ (A)}$$

The power delivered by the supply voltage is:

$$P_{supply} = V_{CC} \cdot I_{CC_{AVG}} \quad \text{(W)}$$

Therefore, the **power dissipated by each amplifier** is:

$$P_{diss} = P_{supply} - P_{out} \quad \text{(W)}$$

Equation 2

$$P_{diss} = \frac{2\sqrt{2}V_{CC}}{\pi\sqrt{R_L}}\sqrt{P_{out}} - P_{out}$$

and the maximum value is obtained when:

$$\frac{\partial P_{diss}}{\partial P_{out}} = 0$$

and its value is:

Equation 3

$$Pdiss\,max = \frac{2Vcc^2}{\pi^2 R_L} \text{ (W)}$$

Note: This maximum value is only dependent on the power supply voltage and load values.

The **efficiency** is the ratio between the output power and the power supply:

Equation 4

$$\eta = \frac{P_{out}}{P_{supply}} = \frac{\pi V_{peak}}{4V_{CC}}$$

The maximum theoretical value is reached when $V_{peak} = V_{CC}$, so:

$$\eta = \frac{\pi}{4} = 78.5\%$$

The maximum die temperature allowable for the TS4994 is 125°C. However, in case of overheating, a thermal shutdown set to 150°C, puts the TS4994 in standby until the temperature of the die is reduced by about 5°C.

To calculate the maximum ambient temperature T_{amb} allowable, you need to know:

- The value of the power supply voltage, V_{CC}
- The value of the load resistor, R_L
- The R_{thja} value for the package type

Example: V_{CC} = 5V, R_L = 8Ω, $R_{thja\text{-}flipchip}$ = 100°C/W (100mm² copper heatsink)

Using the power dissipation formula given above in *Equation 3* this gives a result of:

$P_{dissmax}$ = 633mW

T_{amb} is calculated as follows:

Equation 5

$$T_{amb} = 125°C - R_{TJHA} \times P_{dissmax}$$

Therefore, the maximum allowable value for T_{amb} is:

T_{amb} = 125-80x0.633=62°C

4.8 Decoupling of the circuit

Two capacitors are needed to correctly bypass the TS4994. A power supply bypass capacitor C_s and a bias voltage bypass capacitor C_b.

C_s has particular influence on the THD+N in the high frequency region (above 7kHz) and an indirect influence on power supply disturbances. With a value for C_s of 1µF, you can expect similar THD+N performance to that shown in the datasheet.

In the high frequency region, if C_s is lower than 1µF, it increases THD+N, and disturbances on the power supply rail are less filtered.

On the other hand, if C_s is higher than 1µF, the disturbances on the power supply rail are more filtered.

C_b has an influence on THD+N at lower frequencies, but its function is critical to the final result of PSRR (with input grounded and in the lower frequency region).

4.9 Wake-up time: t_{WU}

When the standby is released to put the device ON, the bypass capacitor C_b is not charged immediately. As C_b is directly linked to the bias of the amplifier, the bias will not work properly until the C_b voltage is correct. The time to reach this voltage is called the wake-up time or t_{WU} and is specified in *Table 3 on page 5*, with C_b=1µF. During the wake-up time, the TS4994 gain is close to zero. After the wake-up time, the gain is released and set to its nominal value.

If C_b has a value other than 1µF, refer to the graph in *Figure 88 on page 22* to establish the wake-up time.

4.10 Shutdown time

When the standby command is set, the time required to put the two output stages in high impedance and the internal circuitry in shutdown mode is a few microseconds.

Note: In shutdown mode, the Bypass pin and Vin+, Vin- pins are short-circuited to ground by internal switches. This allows a quick discharge of the C_b and C_{in} capacitors.

4.11 Pop performance

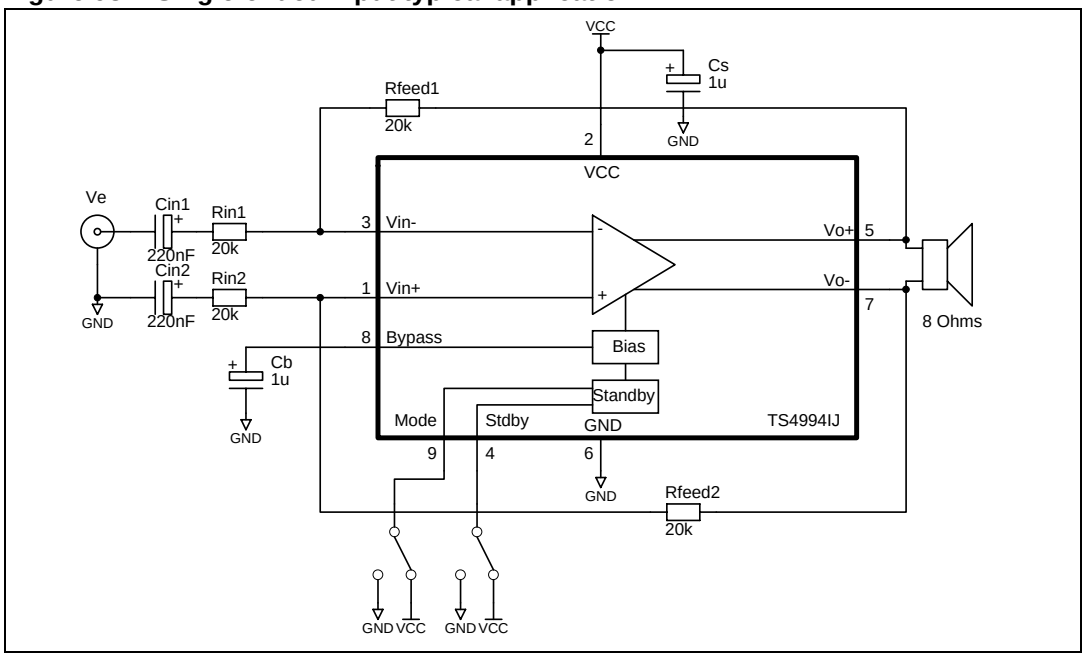
Due to its fully differential structure, the pop performance of the TS4994 is close to perfect. However, due to mismatching between internal resistors R_{in}, R_{feed}, and external input capacitors C_{in}, some noise might remain at startup. To eliminate the effect of mismatched components, the TS4994 includes pop reduction circuitry. With this circuitry, the TS4994 is close to zero pop for all possible common applications.

In addition, when the TS4994 is in standby mode, due to the high impedance output stage in this configuration, no pop is heard.

4.12 Single-ended input configuration

It is possible to use the TS4994 in a single-ended input configuration. However, input coupling capacitors are needed in this configuration. The schematic in *Figure 98* shows an example of this configuration.

Figure 98. Single-ended input typical application



The component calculations remain the same, except for the gain. In single-ended input configuration, the formula is:

$$Av_{SE} = \frac{V_{O+} - V_{O-}}{Ve} = \frac{R_{feed}}{R_{in}}$$

5 Package information

In order to meet environmental requirements, STMicroelectronics offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an STMicroelectronics trademark. ECOPACK specifications are available at: www.st.com.

Flip-chip package (9 bumps)

Dimensions in millimeters unless otherwise indicated.

Figure 99. Pinout (top view)

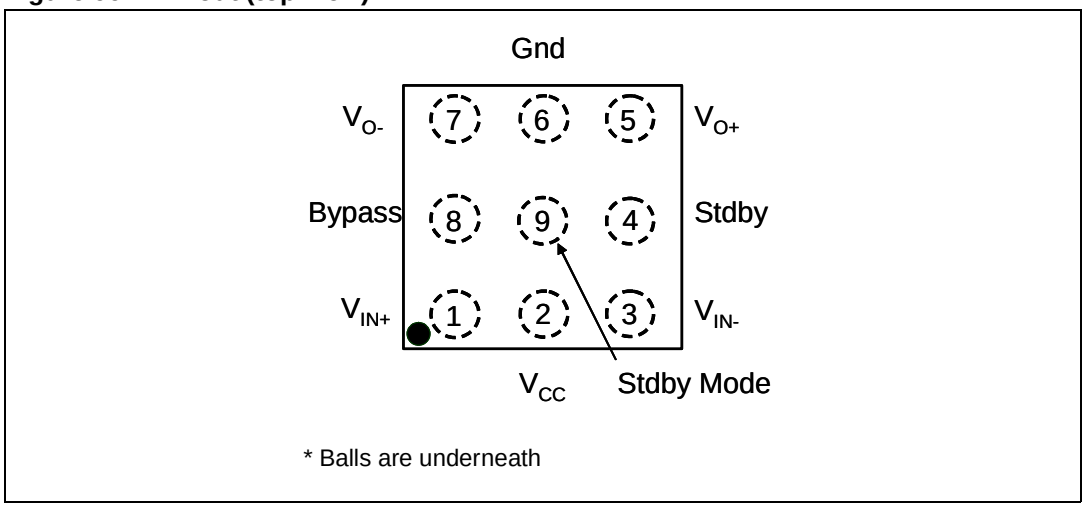


Figure 100. Marking (top view)

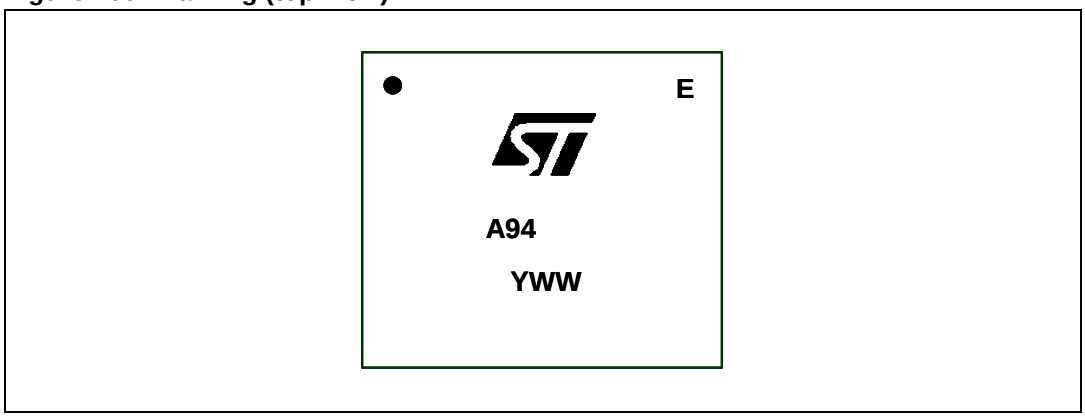
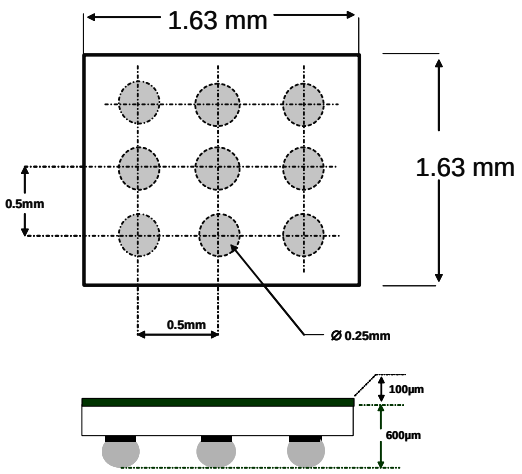
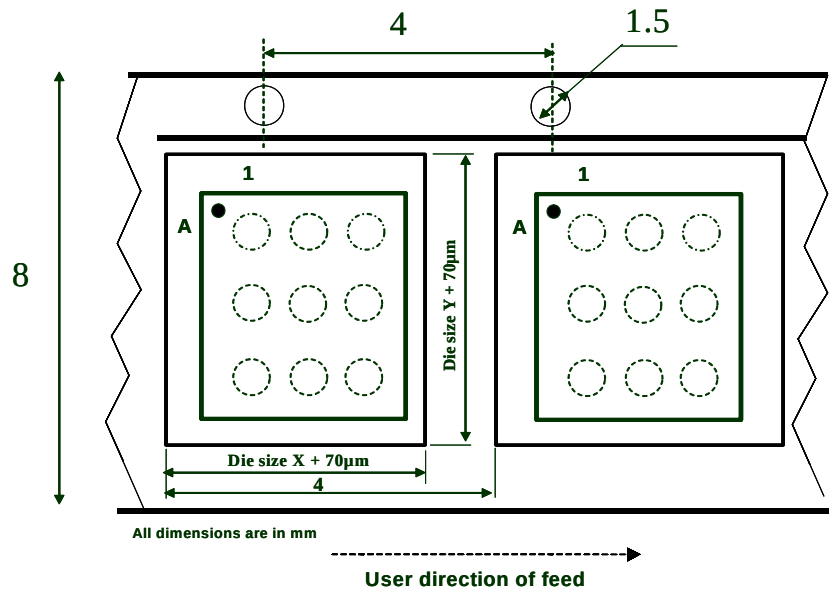


Figure 101. Dimensions



- Die size: **1.63mm x 1.63mm** ± 30µm
- Die height (including bumps): **600µm**
- Bumps diameter: **315µm** ±50µm
- Bump diameter before reflow: **300µm** ±10µm
- Bump height: **250µm** ±40µm
- Back coating height: **40µm** ±10µm
- Die height: **350µm** ±20µm
- Pitch: **500µm** ±50µm
- Coplanarity: **60µm max**

Figure 102. Tape & reel dimensions



6 Revision history

Table 6. Document revision history

Date	Revision	Changes
17-Mar-2005	1	Initial release.
12-Dec-2006	2	Template update.

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