

Product Features

- Featuring **QiK Chip™** Technology
- From order to ship in 2 weeks
- Superior Jitter Performance (less than 0.25 ps RMS, 12 kHz - 20 MHz)
- SAW replacement - better performance
- Frequencies from 150 MHz to 1.4 GHz



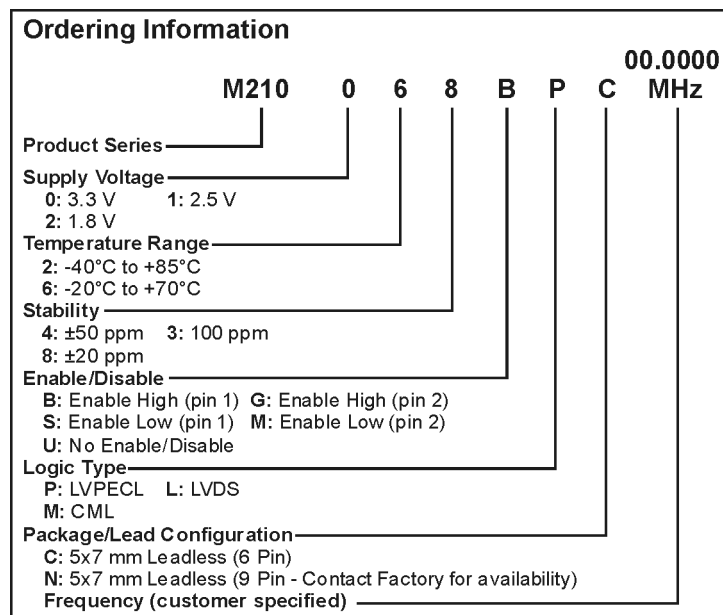
Product Description

The 210x series of oscillators are 5x7 mm oscillators designed with the QiK Chip™ technology. The QiK Chip™ technology was specifically designed for crystal based oscillators to provide low jitter performance (as low as 0.25 ps RMS) and a wide range of frequency support (150.00 MHz to 1.4 GHz) and provides a breakthrough in lean manufacturing enabling product to be provided in less than 2 weeks. The M210x provides design engineers with the stability needed in their advanced applications and supports the need for parts to be supplied quickly so that the rest of their circuit design can be solidified.

Product Applications

- Telecommunications such as SONET / SDH / DWDM / FEC / SERDES / OC-3 thru OC-192
- 1-2-4-10 Gigabit Fibre Channel
- Wireless Base Stations / WLAN / Gigabit Ethernet
- Avionic Flight Controls
- Military Communications
- Clock and Data Recovery
- SD/HD Video
- FPGA/ASIC Clock Generation
- Test and Measurement Equipment

Product Ordering Information



M2100Sxxx, M2101Sxxx, M2102Sxxx & M2103Sxxx -
Contact factory for datasheets.

Performance Characteristics

PARAMETER	Symbol	Min.	Typ.	Max.	Units	Condition/Notes	
Frequency Range	F	150		1400	MHz	See Note 1	
Operating Temperature	T _A	(See ordering information)					
Storage Temperature	T _S	-55		+125	°C		
Frequency Stability	ΔF/F	(See ordering information)					See Note 2
Aging 1st Year		-3		+3	ppm		
Thereafter (per year)		-1		+1	ppm		
Supply Voltage	V _{cc}	1.71 2.375 3.135	1.8 2.5 3.3	1.89 2.625 3.465	V V V	LVDS/CML	
Input Current	I _{cc}			125	mA	LVPECL/LVDS/CML	
Load		50 Ohms to (V _{cc} -2) V _{dc} 100 Ohm differential load				See Note 3 LVPECL Waveform LVDS/CML Waveform	
Symmetry (Duty Cycle)		45		55	%	LVPECL – V _{dd} -1.3 V LVDS – 1.25 V	
Output Skew			20 15 20		ps ps ps	LVPECL CML LVDS	
Differential Voltage	V _{od}	250	350	450	mV	LVDS	
	V _{od}	0.7	.095	1.20	V _{pp}	CML	
Common Mode Output Voltage	V _{cm}		1.2		V	LVDS	
Logic “1” Level	V _{oh}	V _{cc} -1.02			V	LVPECL	
Logic “0” Level	V _{ol}			V _{cc} -1.63	V	LVPECL	
Rise/Fall Time	T _r /T _f		0.23	0.50	ns	@ 20/80% LVPECL	
Enable Function		80% V _{cc} min or N/C: Output active 0.5V max: Output disables to high-Z				Output Option B or G	
		0.5V max or N/C: Output active 80% V _{cc} min: Output disables to high-Z				Output Option S or M	
Start up Time				10	ms		
Phase Jitter @ 622.08 MHz	φ _J		0.25		ps RMS	Integrated 12 kHz – 20 MHz	
Phase Noise			-60 -97 -107 -116 -121 -134 -146 -148			@ 622.08 MHz dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz	
Mechanical Shock	Per MIL-STD-202, Method 213, Condition C (100 g's, 6 mS duration, ½ sinewave)						
Vibration	Per MIL-STD-202, Method 201 & 204 (10 g's from 10-2000 Hz)						
Hermeticity	Per MIL-STD-202, Method 112, (1x10 ⁻⁸ atm. cc/s of Helium)						
Thermal Cycle	Per MIL-STD-883, Method 1010, Condition B (-55°C to +125°C, 15 min. dwell, 10 cycles)						
Solderability	Per EIAJ-STD-002						
Max Soldering Conditions	See solder profile, Figure 1						

Note 1: Contact factory for standard frequency availability over 945 MHz

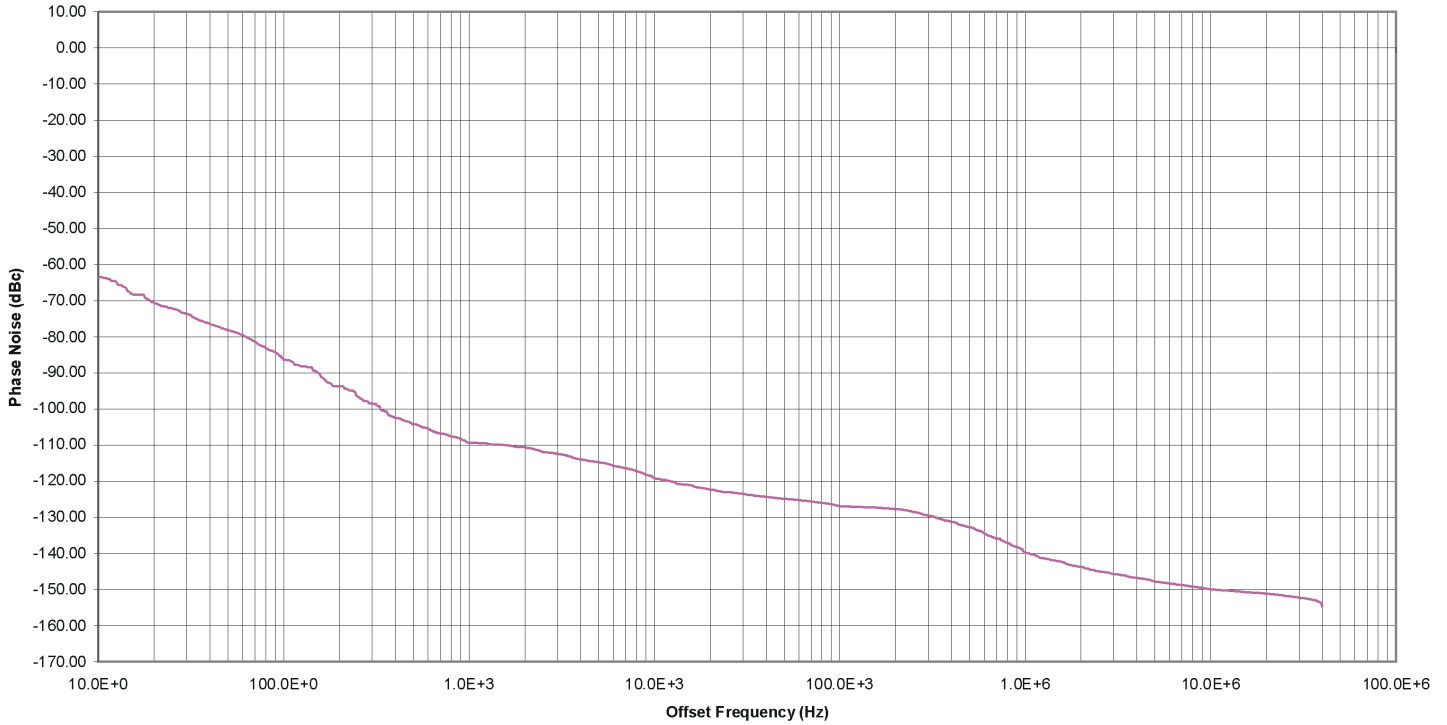
Note 2: Stability is inclusive of initial tolerance, deviation over temperature, shock, vibration, supply voltage, and aging for one year at 50°C mean ambient temperature.

Note 3: See Load Circuit Diagram in this Datasheet. Consult factory with nonstandard output load requirements.

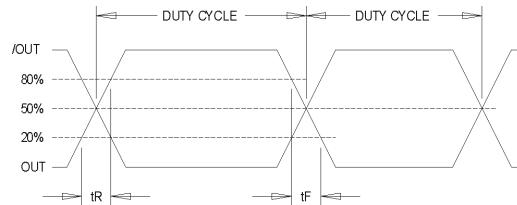
Phase Noise Plot

M210X Phase Noise Plot @ 622.08 MHz

Phase Noise (dBc/Hz) 622.08MHz



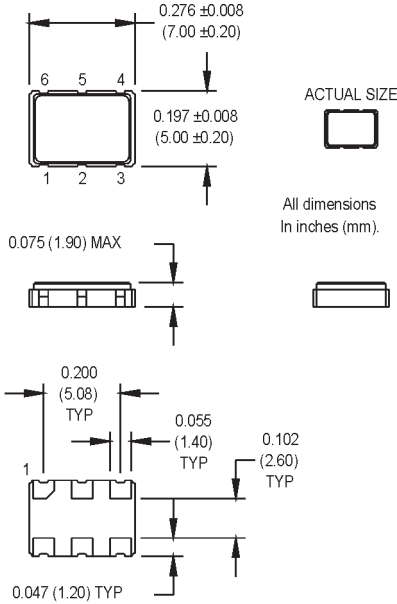
Output Waveform



Output Waveform: LVDS/CML/PECL

Product Dimension & Pinout Information

6 Pad Standard Option

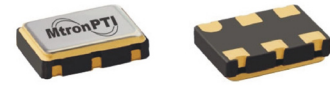


PIN 1 ENABLE

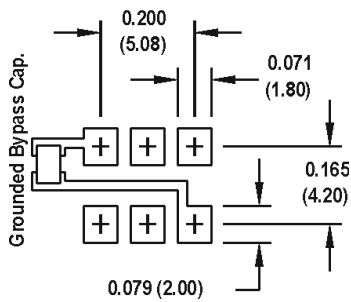
- Pad1: Enable/Disable
- Pad2: N/C
- Pad3: Ground
- Pad4: Output Q (LVPECL, LVDS, CML)
- Pad5: Output Q (LVPECL, LVDS, CML)
- Pad6: Vcc

PIN 2 ENABLE

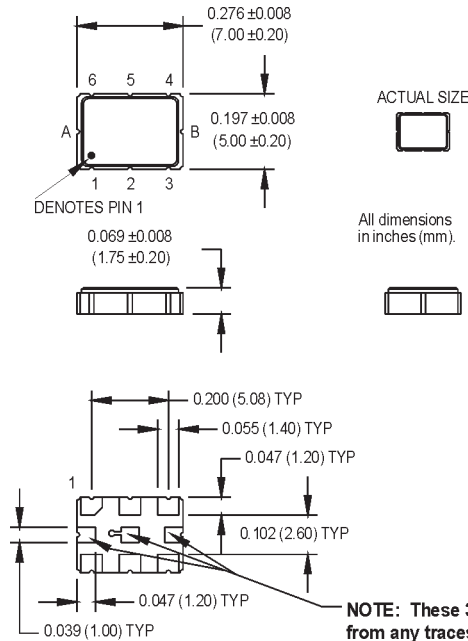
- Pad1: N/C
- Pad2: Enable/Disable
- Pad3: Ground
- Pad4: Output Q (LVPECL, LVDS, CML)
- Pad5: Output Q (LVPECL, LVDS, CML)
- Pad6: Vcc



SUGGESTED SOLDER PAD LAYOUT



9 Pad Option



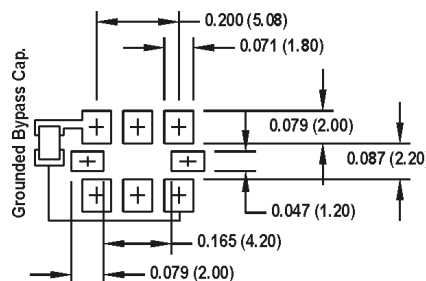
PIN 1 ENABLE

- Pad1: Enable/Disable
- Pad2: N/C
- Pad3: Ground
- Pad4: Output Q (LVPECL, LVDS, CML)
- Pad5: Output Q (LVPECL, LVDS, CML)
- Pad6: Vcc
- PadA: Do not connect!
- PadB: Do not connect!
- PadC: Do not connect!

PIN 2 ENABLE

- Pad1: N/C
- Pad2: Enable/Disable
- Pad3: Ground
- Pad4: Output Q (LVPECL, LVDS, CML)
- Pad5: Output Q (LVPECL, LVDS, CML)
- Pad6: Vcc
- PadA: Do not connect!
- PadB: Do not connect!
- PadC: Do not connect!

SUGGESTED SOLDER PAD LAYOUT



Handling Information

Although protection circuitry has been designed into the M210x oscillator, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. MtronPTI utilizes a human-body model (HBM) and a charged-device model (CDM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used to define the mode. Although no industry-wide standard has been adopted for the CDM, a standard HBM (resistance = 1500 Ω, capacitance = 100 pF) is widely used and therefore can be used for comparison purposes. The HBM ESD threshold presented here was obtained using these circuit parameters.

Model	ESD Threshold, Minimum	Unit
Human Body	1500*	V
Charged Device	1500*	V

* MIL-STD-883D, Method 3015, Class 1



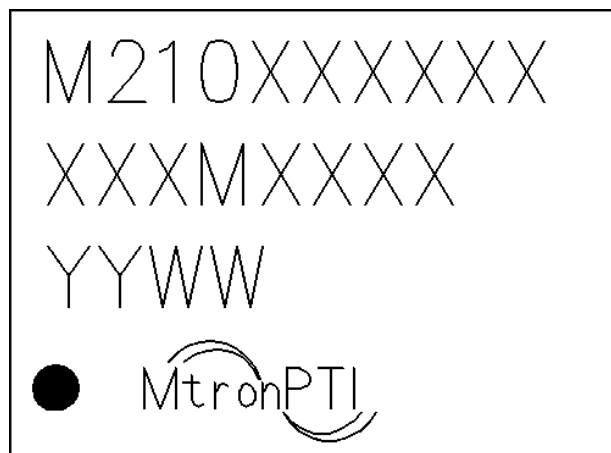
ATTENTION
Static Sensitive
Devices
Handle only at
Static Safe Work
Stations

Quality Parameters

Environmental Specifications/Qualification Testing Performed on the M210 Clock Oscillator		
Test	Test Method	Test Condition
Electrical Characteristics	Internal Specification	Per Specification
Frequency vs. Temperature	Internal Specification	Per Specification
Mechanical Shock	MIL-STD-202, Method 213, C	100 g's
Vibration	MIL-STD-202, Method 201-204	10 g's from 10-2000 Hz
Thermal Cycle	MIL-STD-883, Method 1010, B	-55 Deg. C to +125 Deg. C, 15 minute Dwell, 10 cycles
Aging	Internal Specification	168 Hours at 105 Degrees C
Gross Leak	MIL-STD-202, Method 112	30 Second Immersion
Fine Leak	MIL-STD-202, Method 112	Must meet 1x10 ⁻⁵
Solderability	MIL-STD-883, Method 2003	8 Hour Steam Age – Must Exhibit 95% coverage
Resistance to Solvents	MIL-STD-883, Method 2015	Three 1 minute soaks
Terminal Pull	MIL-STD-883, Method 2004, A	2 Pounds
Lead Bend	MIL-STD-883, Method 2004, B1	1 Bending Cycle
Physical Dimensions	MIL-STD-883, Method 2016	Per Specification
Internal Visual	Internal Specification	Per Internal Specification

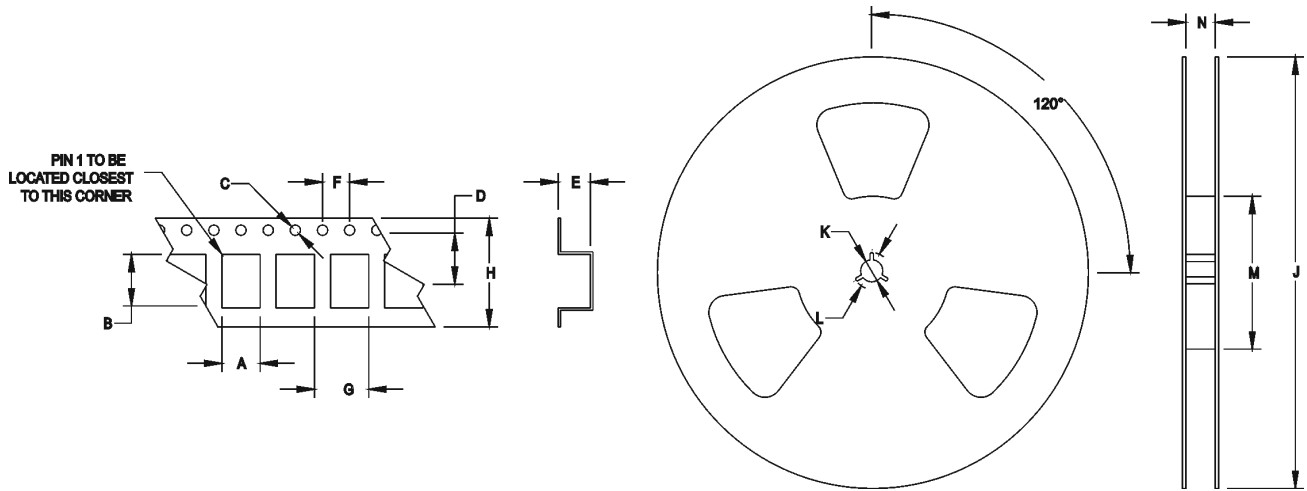
Part Marking Guide

- Line 1: Model Number
- Line 2: Frequency
- Line 3: Date Code
- Line 4: Pin 1 Indicator / MtronPTI



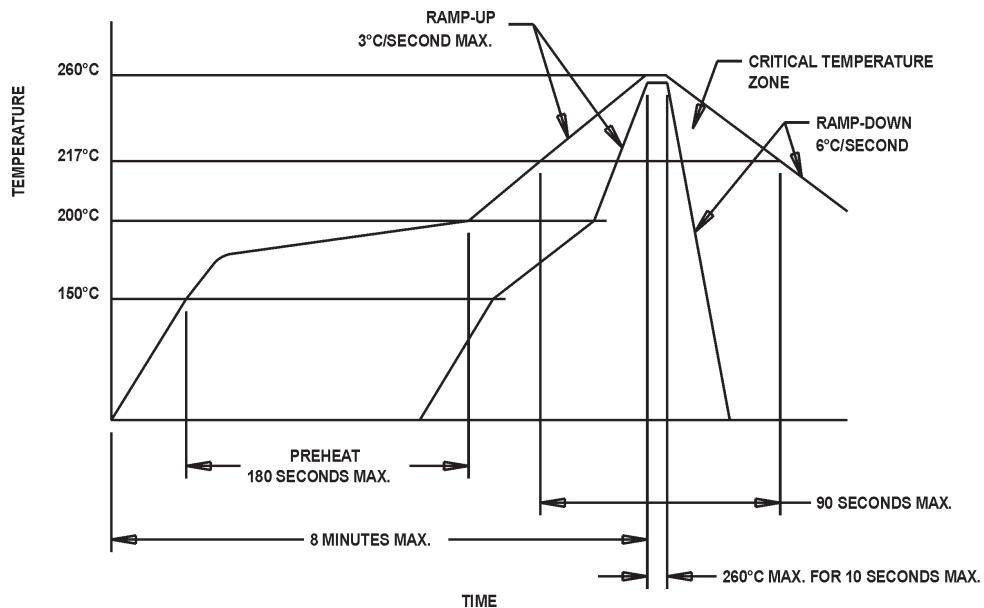
Tape & Reel Specifications

(all measurements are in mm)	A	B	C	D	E	F	G	H	I	J	K	L
M210x	6.51	9.29	1.5	7.5	2.8	4	8/12	16	180-330	13	21	60-100



Standard Tape and Reel: 1000 parts per reel

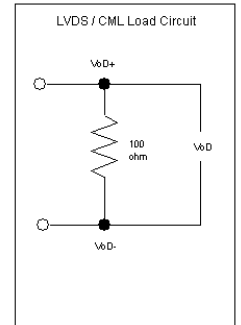
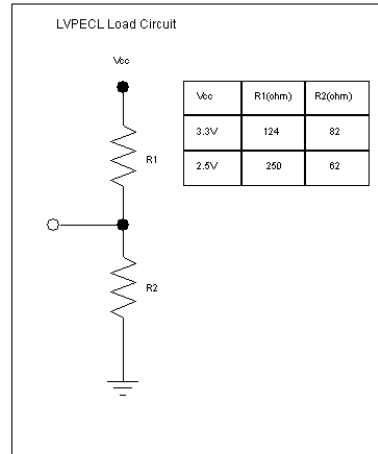
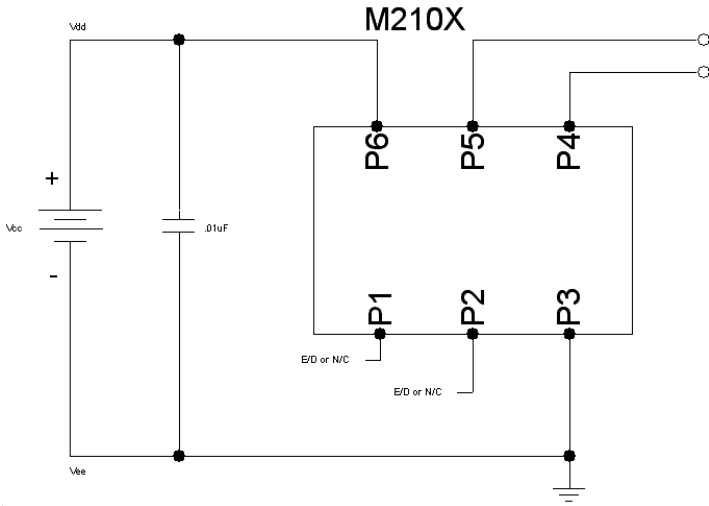
Maximum Soldering Conditions



Solder Conditions

Note: Exceeding these limits may damage the device.

Typical Test Circuit & Load Circuit Diagrams



Product Revision Table

Date	Revision	PCN Number	Details of Revision
7/20/07	A	10118	IC Revision to improve phase noise and electrical performance

For custom products or additional specifications contact our sales team at
800.762.8800 (toll free) or 605.665.9321

For more information on this product visit the MtronPTI website at
www.mtronpti.com