Edge819
Octal, 18V Pin Electronics Driver

TEST AND MEASUREMENT PRODUCTS

Description

The Edge819 is an octal pin electronics driver fabricated in a wide voltage CMOS process. It is designed specifically for Test During Burn In (TDBI) applications, where cost, functional density, and power are all at a premium.

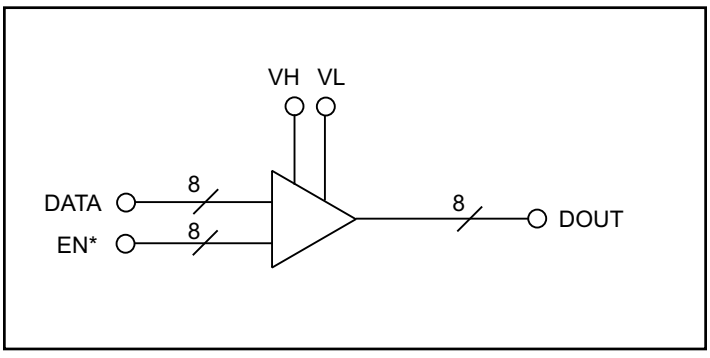
The Edge819 incorporates eight channels of programmable drivers into one 14 mm X 20 mm 100 pin MQFP package. Each channel has per pin driver levels, data, and high impedance control.

The Edge819 uses "Flex In" digital inputs and, therefore, can mate directly with any digital technology.

The Edge819 is pin and functionally compatible with the Edge818, except the Edge819 does not have any comparators.

The 18V driver output range allows the Edge819 to interface directly with TTL, ECL, CMOS (3.3V and 5V), LVCMOS, and custom level circuitry, as well as the high voltage (Super Voltage) level required for many special test modes for Flash Devices.

Functional Block Diagram



Features

- 18V I/O Range
- 50 MHz Operation
- Per Pin Flexibility
- Flex In Digital Inputs
- Small footprint (100 pin MQFP)

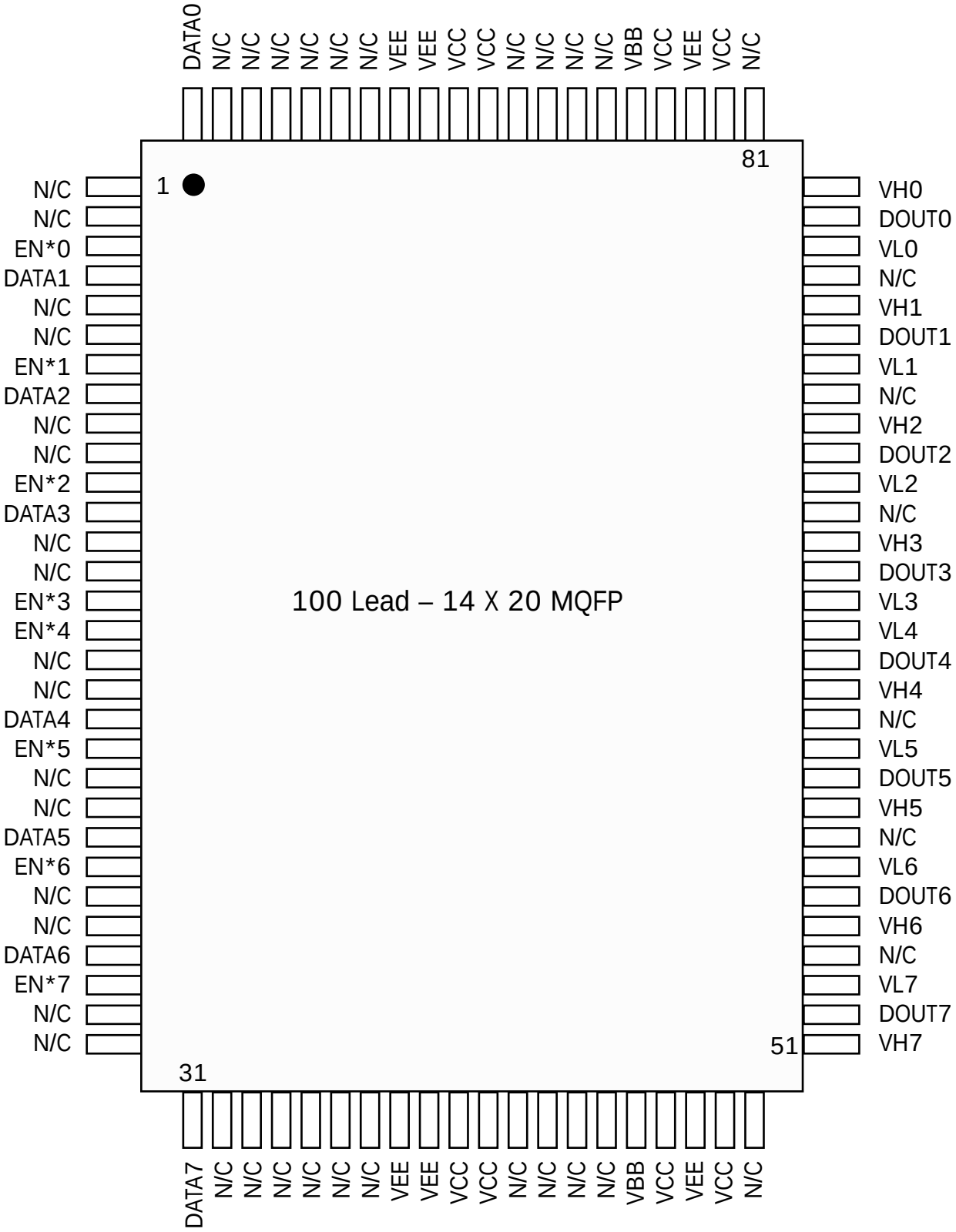
Applications

- Burn In ATE
- Low Cost ATE
- Instrumentation

PIN Description

Pin Name	Pin #	Description
DATA (0:7)	100, 4, 8, 12, 19, 23, 27, 31	Digital inputs which determine the high/low state of the driver when it is enabled.
EN* (0:7)	3, 7, 11, 15, 16, 20, 24, 28	Digital inputs which enable/disable the driver.
N/C	1, 5, 9, 13, 18, 22, 26, 30, 2, 6, 10, 14, 17, 21, 25, 29	No connect.
DOUT (0:7)	79, 75, 71, 67, 64, 60, 56, 52	Driver outputs.
N/C	81, 77, 73, 69, 62, 58, 54, 50	No connect.
VH (0:7)	80, 76, 72, 68, 63, 59, 55, 51	Unbuffered analog inputs that set the driver "high" voltage level.
VL (0:7)	78, 74, 70, 66, 65, 61, 57, 53	Unbuffered analog inputs that set the driver "low" voltage level.
N/C	97, 95, 89, 87, 44, 42, 36, 34	No connect.
N/C	96, 94, 88, 86, 45, 43, 37, 35	No connect.
VBB	46, 85	Analog input voltage that sets the threshold for the digital inputs.
N/C	33, 98	No connect.
N/C	32, 99	No connect.
VCC	40, 41, 47, 49, 82, 84, 90, 91	Positive power supply.
VEE	38, 39, 48, 83, 92, 93	Negative power supply.

PIN Description *(continued)*



Driver Description

The Edge819 supports programmable high and low levels and tristate per channel. There are no shared lines between any drivers. The EN* and DATA signals are wide voltage high impedance analog inputs capable of receiving digital signals over a wide common mode range. VBB is the high impedance analog input which sets the threshold for EN* and DATA.

EN*, DATA	Status
> VBB	"1"
< VBB	"0"

With EN* high, the driver goes into a high impedance state. With EN* low, DATA high forces the driver into a high state, and DATA low forces the driver into a low state.

EN*	DATA	DOUT
1	X	HiZ
0	1	VH
0	0	VL

Driver High and Low

VH and VL define the logical "1" and "0" levels of the driver, and can be adjusted anywhere over the range determined by VCC and VEE. There are no restrictions between VH and VL, other than they must remain within the power supply levels.

$$VEE \leq VH \leq VCC$$
$$VEE \leq VL \leq VCC$$

Driver Output Protection

In a functional testing environment, where a resistor is added in series with the driver output to create a 50Ω driver, the Edge819 can withstand a short to any legal voltage for an indefinite amount of time.

In a low impedance application, with no additional output resistance, the system should be designed to check for a short circuit prior to connecting the driver, and tristate the driver if a short is detected.

Application Information

Power Supply Decoupling

VCC and VEE should be decoupled to GND with a .1 µF chip capacitor in parallel with a .001 µF chip capacitor. A VCC and VEE plane, or at least a solid power bus, is recommended for optimal performance.

VH and VL Decoupling

As the VH and VL inputs are unbuffered and supply the driver output current, which can be quite large during edge transitions, decoupling capacitors for these inputs are recommended in proportion to the amount of output current requirements.

For applications where VH and VL are shared over multiple channels, a solid power plane to distribute these levels is preferred.

VBB

The two VBB pins are connected together on-chip. Therefore, only one VBB needs to be connected to for proper 819 operation.

The two pins may be used to daisy chain a VBB signal across a PC Board without having to route the actual signal underneath the 819.

Power Supplies

The Edge819 has several power supply requirements to protect the part in power supply fault situations, as well as during power up and power down sequences.

The following power supply requirements must be satisifed at all times:

$$VEE \leq \text{All I/O Pins} \leq VCC \text{ at all times}$$

The power sequence below can be used as a guideline when operating the Edge819:

Power-On Sequencing	*Power-Off Sequencing*
1. VCC (Substrate)	1. I/O Pins
2. VEE	2. VEE
3. I/O Pins	3. VCC

The three diode configuration shown in Figure 1 should be used on a once-per-board basis.

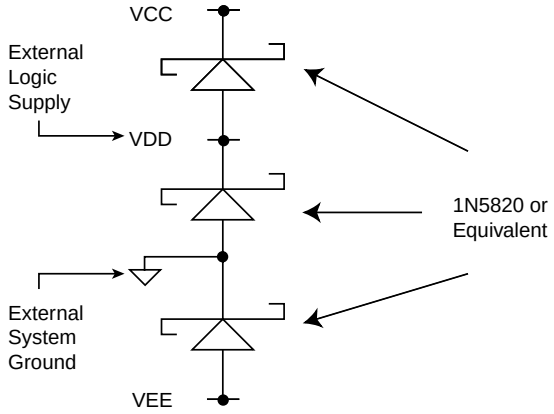
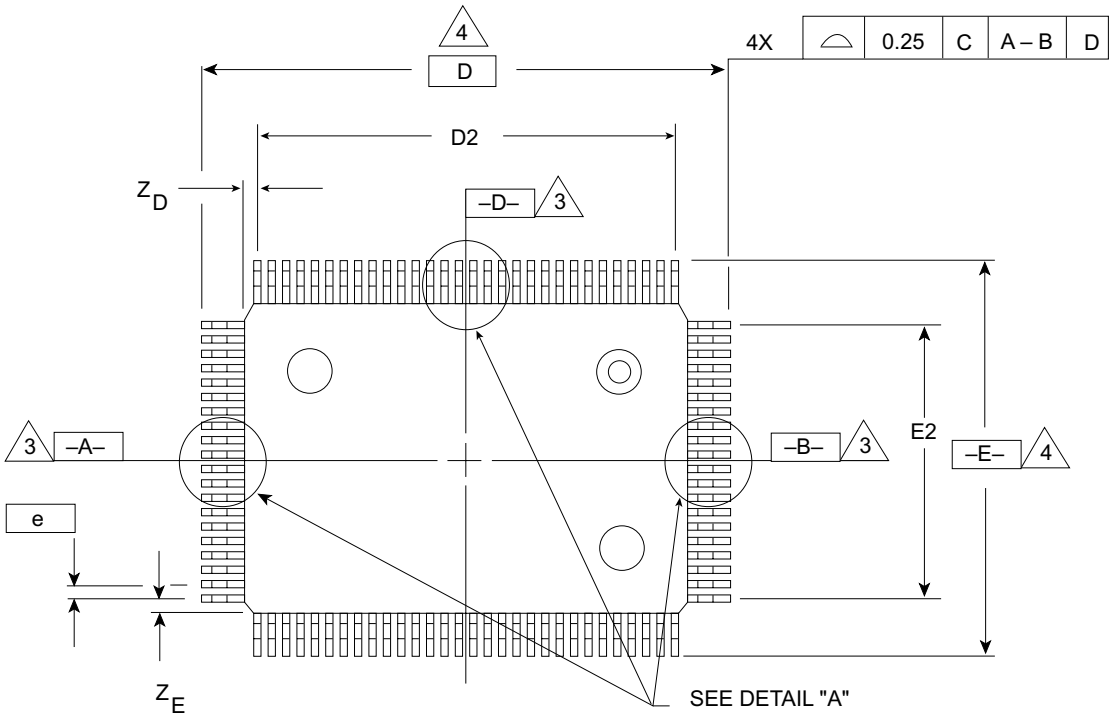


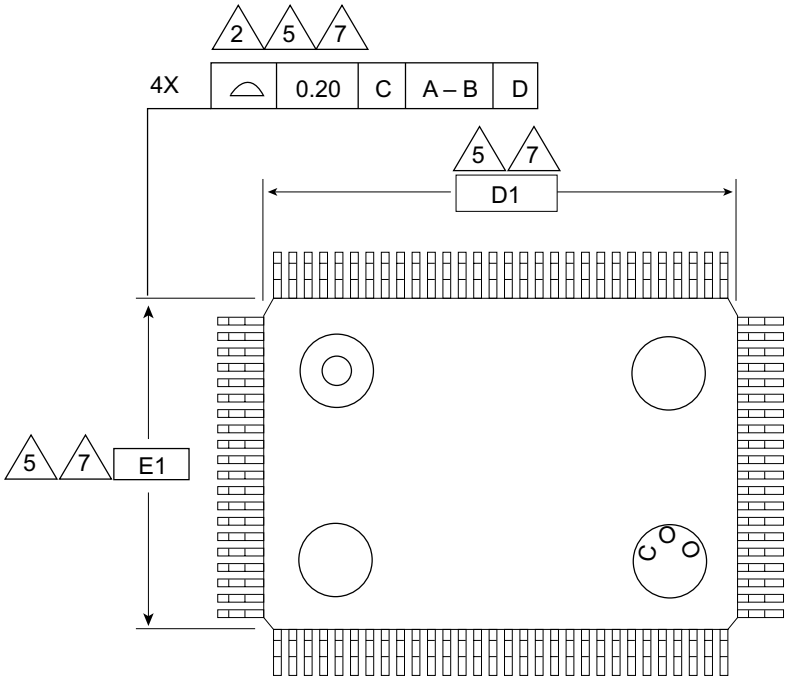
Figure 1.
Power Supply Protection Scheme

Warning: It is extremely important that the voltage on any device pin does not exceed the range of VEE –0.5V to VCC +0.5V at any time, either during power up, normal operation, or during power down. Failure to adhere to this requirement could result in latchup of the device, which could be destructive if the system power supplies are capable of supplying large amounts of current. Even if the device is not immediately destroyed, the cumulative damage caused by the stress of repeated latchup may affect device reliability.

100-Pin MQFP
14 mm x 20 mm

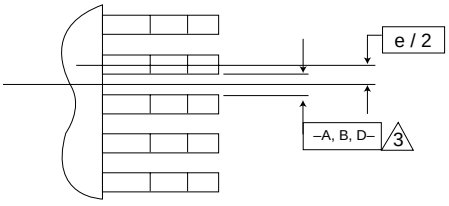


TOP VIEW

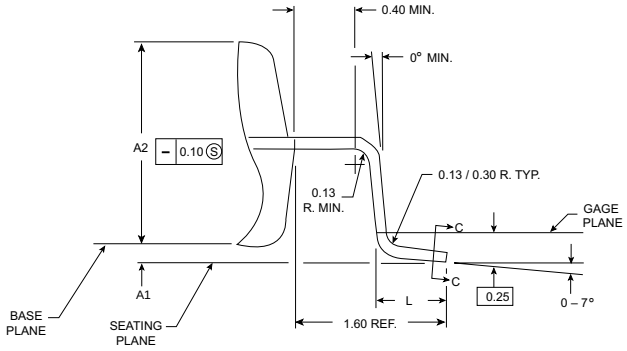


BOTTOM VIEW

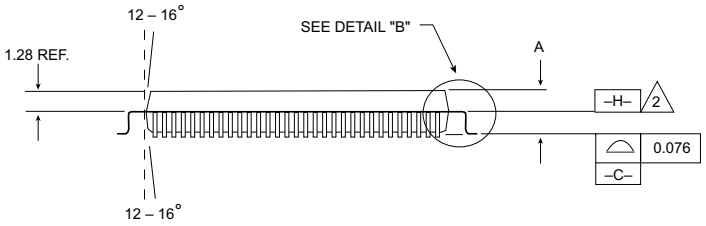
Package Information *(continued)*

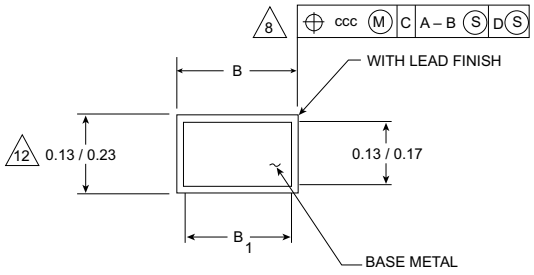


DETAIL "A"



DETAIL "B"





SECTION C–C

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5-1982.
2. Datum plane -H- located at mold parting line and coincident with lead, where lead exits plastic body at bottom of parting line.
3. Datums A-B and -D- to be determined where centerline between leads exits plastic body at datum plane -H-.
4. To be determined at seating plane -C-.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable mold protrusion is 0.254 mm per side. Dimensions D1 and E1 do include mold mismatch and are determined at datum plane -H-.
6. "N" is the total # of terminals.
7. Package top dimensions are smaller than bottom dimensions and top of package will not overhang bottom of package.
8. Dimension B does not include dambar protrusion. Allowable dambar protrusion shall be 0.08 mm total in excess of the dimension at maximum material condition. Dambar cannot be located on the lowerradius or the foot.
9. All dimensions are in millimeters.
10. Maximum allowable die thickness to be assembled in this package family is 0.635 millimeters.
11. This drawing conforms to JEDEC registered outlines MS-108 and MS-022.
12. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.

Variations
(all dimensions in millimeters)

Symbol	Min	Nom	Max	Note	Comments
A		3.04	3.40		Height above PCB
A1	0.25	0.33			Gap above PCB
A2	2.57	2.71	2.87		Body Thickness
D		23.20 BSC		4	
D1		20.00 BSC		5	Body Dimension
D2		18.85 REF			
ZD		0.58 REF			
E		17.20		4	
E1		14.00 BSC		5	Body Dimension
E2		12.35 REF			
ZE		0.83 REF			
L	0.73	0.88	1.03		
N		100		6	Pin Count
e		0.65 BSC			Lead Pitch
B	0.22		0.38	8	Pad Dimension
B1	0.22	0.30	0.33		Pad Dimension
ccc		0.13			
ND		30			Side Pin Count
NE		20			Side Pin Count

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Total Analog Supply	VCC - VEE	+10		+18	V
Ambient Operating Temperature	TA			70	°C
Junction Temperature	TJ			+125	°C
Thermal Resistance of Package (Junction to Still Air)	θ_{JA}		32.2		°C/W
Thermal Resistance of Package (Junction to Case)	θ_{JC}		12.4		°C/W

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Total Power Supply	VCC – VEE	–0.5	19.0	V
Digital Input Voltages	DATA, EN*	VEE – .5	VCC + .5	V
Analog Input Voltages	VH, VL, VBB	VEE – .5	VCC + .5	V
Analog Output Voltages	DOUT	VEE – .5	VCC + .5	V
Ambient Operating Temperature	TA	–50	+125	°C
Storage Temperature	TS	–65	+150	°C
Junction Temperature	TJ		+150	°C
Soldering Temperature (5 seconds, .25" from the pin)	TSOL		+260	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these, or any other conditions beyond those listed, is not implied. Exposure to absolute maximum conditions for extended periods may affect device reliability.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Driver					
High Voltage	VH	VEE		VCC	V
Low Voltage	VL	VEE		VCC	V
Output Swing	VH – VL	VEE		VCC	V
HiZ Leakage Current	Ileak	–2.0	0	+2.0	nA
Output Impedance	Rout	9.0	12	15	Ω
DC Output Current (Note 1)	Iout DC	–125		+125	mA
AC Output Current (Note 2)	Iout AC	–400		+400	mA
Digital Inputs					
Input High Voltage	EN*, DATA - VBB	1.0			V
Input Low Voltage	VBB – EN*, DATA	1.0			V
Input Current	Iin	–100	0	+100	nA
Common Mode Range	DATA, EN*	VEE		VCC	V
Power Supplies					
Positive Supply Current (Note 3)	ICC	36	57	78	mA
Negative Supply Current (Note 3)	IEE	36	57	78	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions". VCC = +15V, VEE = –3V.

Note 1: DC output current is specified per individual driver.
Note 2: Surge current capability for durations of < 2 seconds.
Note 3: VCC = +15V, VEE = –3V.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Driver					
DATA to DOUT (Notes 2, 4)	Tpd	9.5	14.5	19.5	ns
EN* to DOUT (Active to HiZ) (Note 1)	Tpd	10	20	30	ns
EN* to DOUT (HiZ to Active)	Tpd	11	16	21	ns
Rise/Fall Times (Note 2)					
1V Swing (20% - 80%)	Tr/Tf		3.0		ns
3V Swing (10% - 90%)	Tr/Tf		3.5		ns
5V Swing (10% - 90%)	Tr/Tf		4.0		ns
10V Swing (10% - 90%)	Tr/Tf		4.5		ns
15V Swing (10% - 90%)	Tr/Tf		5.0		ns
Maximum Operating Frequency (Note 3)	Fmax	50			MHz
Minimum Pulse Width			8	11	ns

Test conditions (unless otherwise specified): "Recommended Operating Conditions". VCC = +15V, VEE = –3V.

Note 1: Load = 10 mA and measured when a 1V change at the output is detected. (VH = 3V, VL = 0V, VFLOAT = 1.5V, tested at 1V and 2V.)

Note 2: Into 18 cm of 50 Ω transmission line terminate with 1 KΩ and 5 pF, with proper series termination resistor. Guaranteed by characterization. This parameter is not tested in production.

Note 3: This parameter is production tested at 40 MHz.

Note 4: From VBB threshold of DATA to 50% level of DOUT.

Ordering Information

Model Number	Package
E819AHF	100 lead MQFP 14 mm x 20 mm Body Size w/Internal Heat Spreader
EVM819AHF	Edge819 Evaluation Board

Contact Information

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