

H5N5005PL

Silicon N Channel MOS FET High Speed Power Switching

REJ03G0419-0300

Rev.3.00

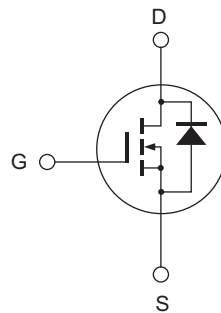
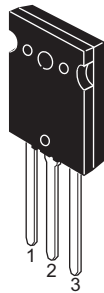
May 25, 2006

Features

- Low on-resistance: $R_{DS(on)} = 0.070 \Omega$ typ.
- Low leakage current: $I_{DSS} = 10 \mu A$ max (at $V_{DS} = 500 V$)
- High speed switching: $t_f = 300 ns$ typ (at $V_{GS} = 10 V$, $I_D = 30 A$, $R_L = 8.33 \Omega$)
- Low gate charge: $Q_g = 300 nC$ typ (at $V_{DD} = 400 V$, $V_{GS} = 10 V$, $I_D = 60 A$)
- Avalanche ratings
- Built-in fast recovery diode: $t_{rr} = 220 ns$ typ

Outline

RENESAS Package code: PRSS0004ZF-A
(Package name: TO-3PL)



1. Gate
2. Drain (Flange)
3. Source

Absolute Maximum Ratings

($T_a = 25^\circ C$)

Item	Symbol	Ratings	Unit
Drain to Source voltage	V_{DSS}	500	V
Gate to Source voltage	V_{GSS}	± 30	V
Drain current	I_D	60	A
Drain peak current	$I_{D(pulse)}$ ^{Note1}	240	A
Body-Drain diode reverse Drain current	I_{DR}	60	A
Body-Drain diode reverse Drain peak current	$I_{DR(pulse)}$ ^{Note1}	240	A
Avalanche current	I_{AP} ^{Note3}	30	A
Channel dissipation	P_{ch} ^{Note2}	270	W
Channel to case thermal impedance	θ_{ch-c}	0.463	$^\circ C/W$
Channel temperature	T_{ch}	150	$^\circ C$
Storage temperature	T_{stg}	-55 to +150	$^\circ C$

Notes: 1. $PW \leq 10 \mu s$, duty cycle $\leq 1\%$

2. Value at $T_c = 25^\circ C$

3. $ST_{ch} = 25^\circ C$, $T_{ch} \leq 150^\circ C$

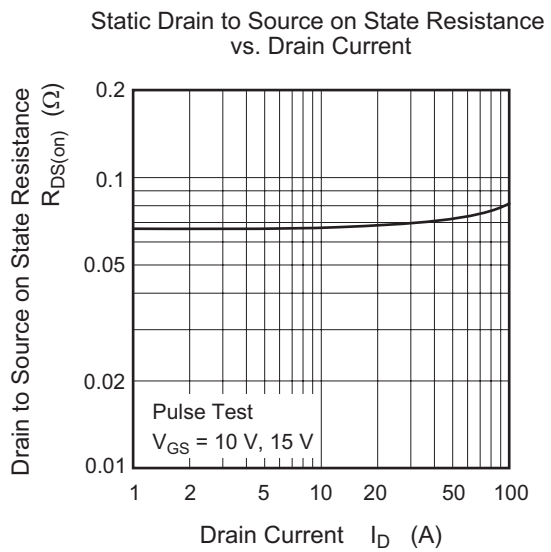
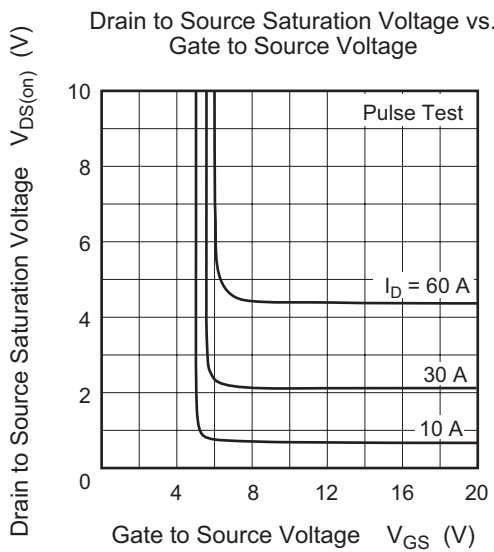
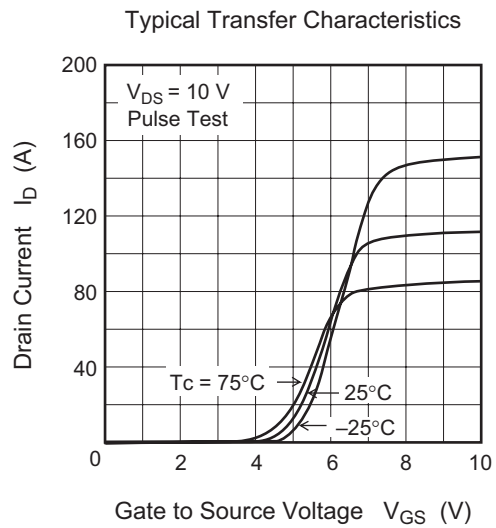
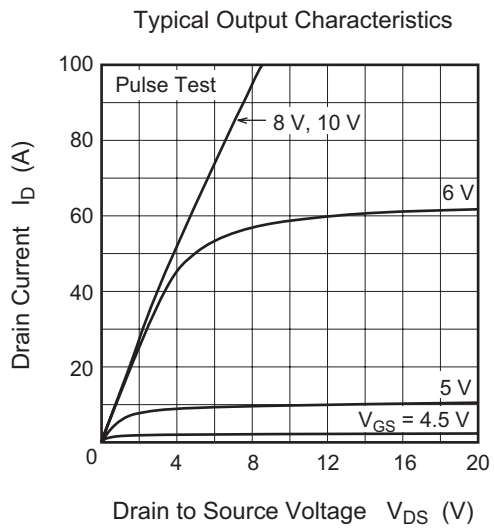
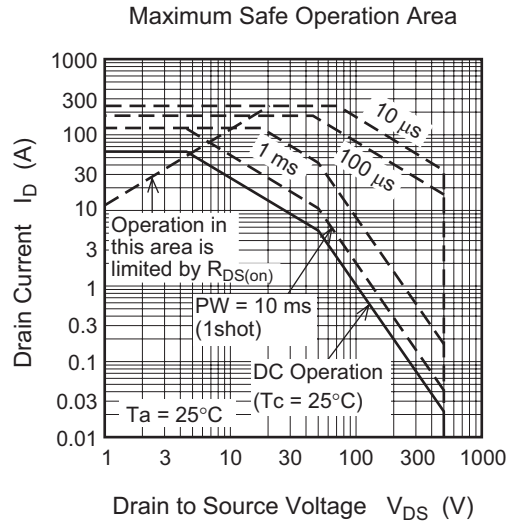
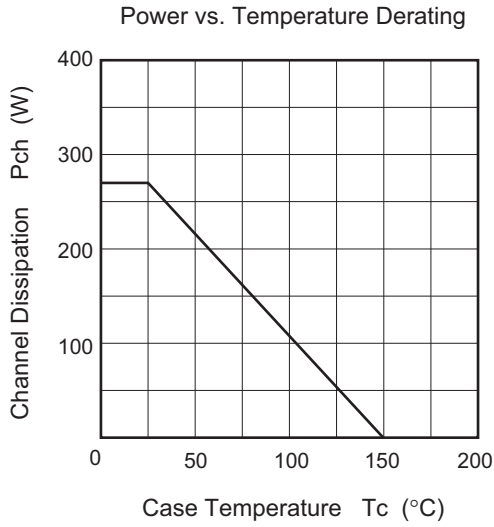
Electrical Characteristics

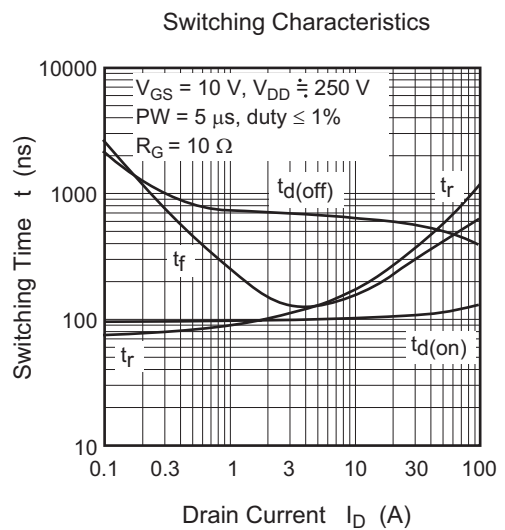
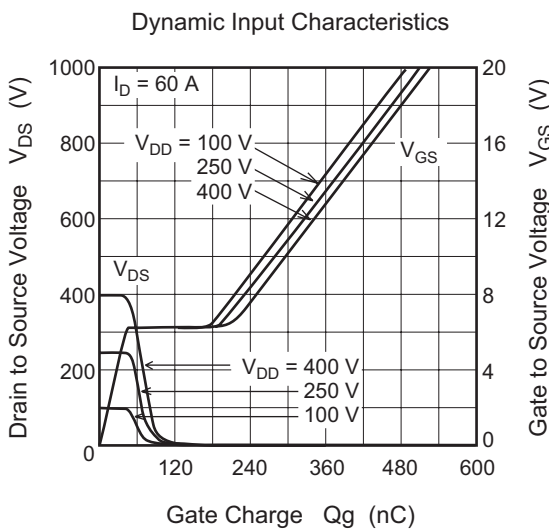
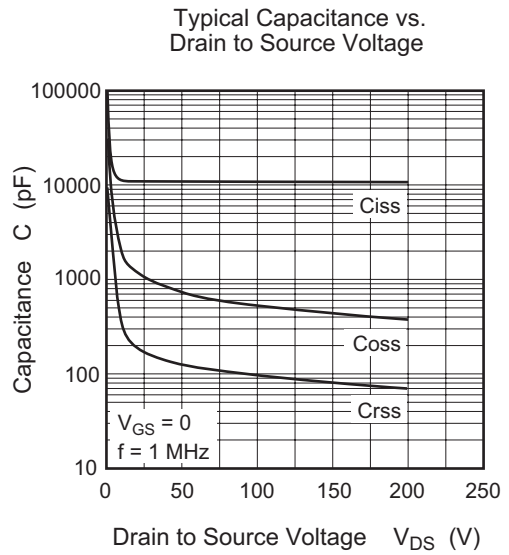
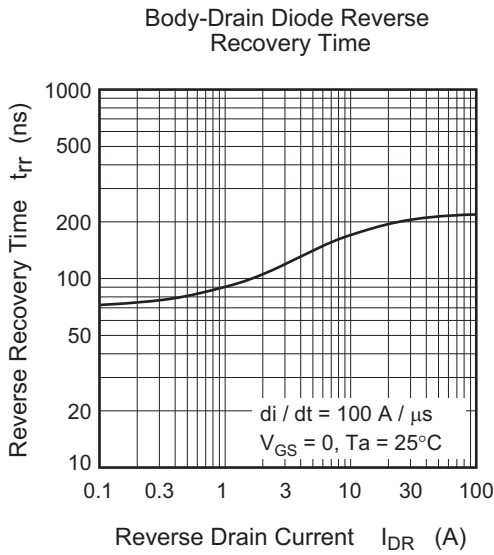
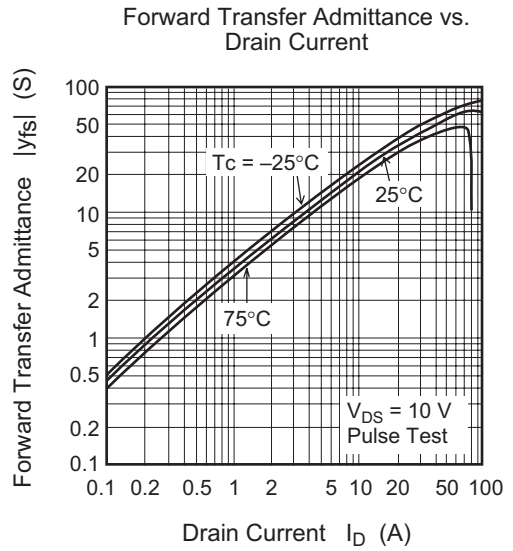
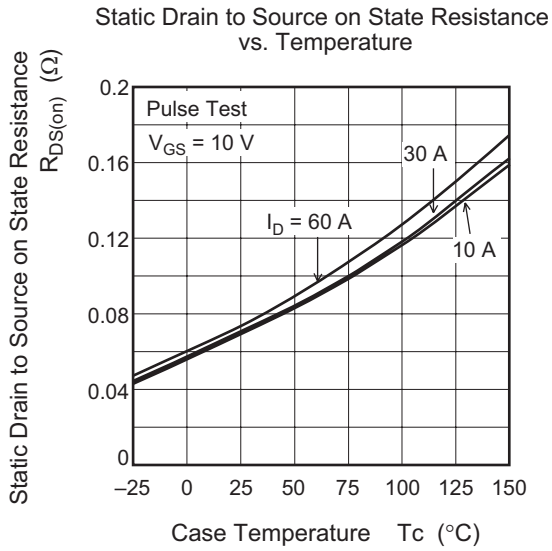
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to Source breakdown voltage	$V_{(BR)DSS}$	500	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Zero Gate voltage Drain current	I_{DSS}	—	—	10	μA	$V_{DS} = 500 \text{ V}$, $V_{GS} = 0$
Gate to Source leak current	I_{GSS}	—	—	± 0.1	μA	$V_{GS} = \pm 30 \text{ V}$, $V_{DS} = 0$
Gate to Source cutoff voltage	$V_{GS(off)}$	2.0	—	4.0	V	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$
Forward transfer admittance	$ y_{fs} $	25	42	—	S	$I_D = 30 \text{ A}$, $V_{DS} = 10 \text{ V}$ ^{Note4}
Static Drain to Source on state resistance	$R_{DS(on)}$	—	0.070	0.085	Ω	$I_D = 30 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note4}
Input capacitance	C_{iss}	—	10550	—	pF	$V_{DS} = 25 \text{ V}$
Output capacitance	C_{oss}	—	1060	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	180	—	pF	$f = 1 \text{ MHz}$
Turn-on delay time	$t_{d(on)}$	—	115	—	ns	$I_D = 30 \text{ A}$
Rise time	t_r	—	380	—	ns	$V_{GS} = 10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	560	—	ns	$R_L = 8.33 \Omega$
Fall time	t_f	—	300	—	ns	$R_g = 10 \Omega$
Total Gate charge	Q_g	—	300	—	nC	$V_{DD} = 400 \text{ V}$
Gate to Source charge	Q_{gs}	—	40	—	nC	$V_{GS} = 10 \text{ V}$
Gate to Drain charge	Q_{gd}	—	155	—	nC	$I_D = 60 \text{ A}$
Body-Drain diode forward voltage	V_{DF}	—	1.0	1.5	V	$I_F = 60 \text{ A}$, $V_{GS} = 0$ ^{Note4}
Body-Drain diode reverse recovery time	t_{rr}	—	220	—	ns	$I_F = 60 \text{ A}$, $V_{GS} = 0$ $di_F/dt = 100 \text{ A}/\mu\text{s}$
Body-Drain diode reverse recovery charge	Q_{rr}	—	2.0	—	μC	

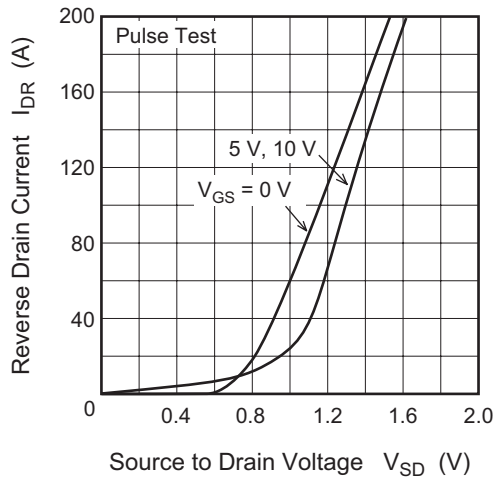
Note: 4. Pulse test

Main Characteristics

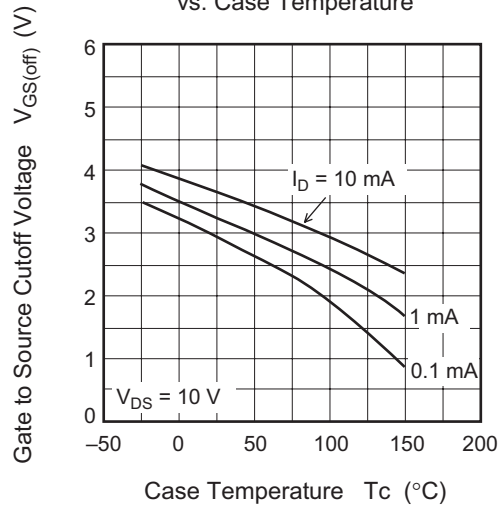




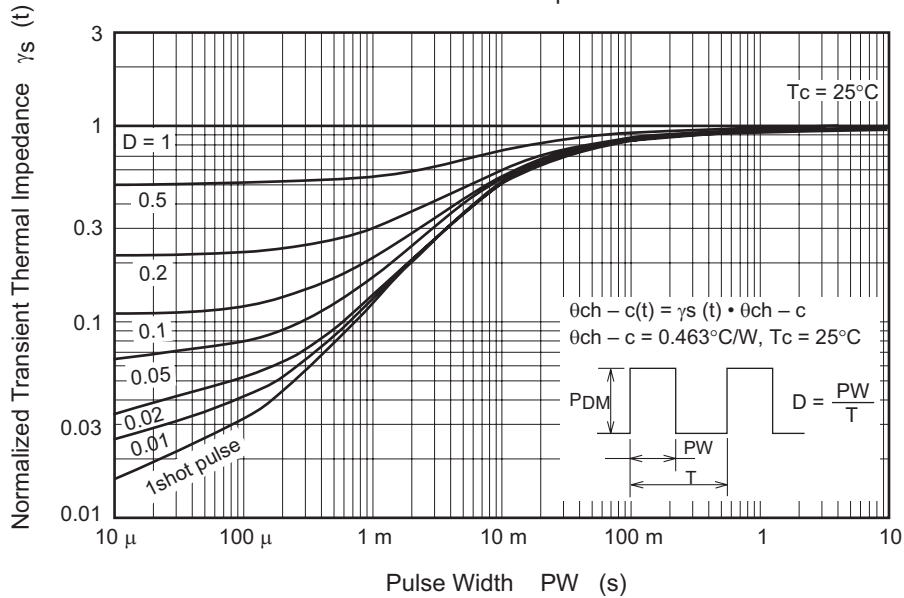
Reverse Drain Current vs. Source to Drain Voltage



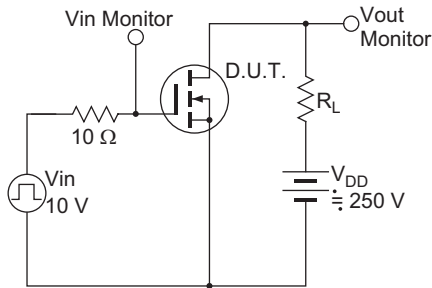
Gate to Source Cutoff Voltage vs. Case Temperature



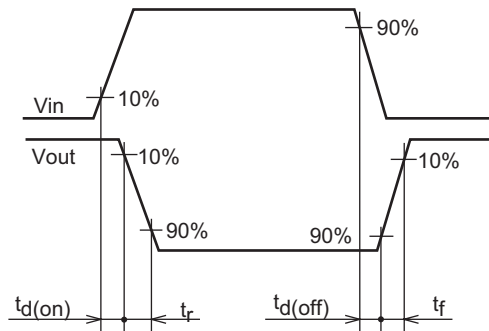
Normalized Transient Thermal Impedance vs. Pulse Width



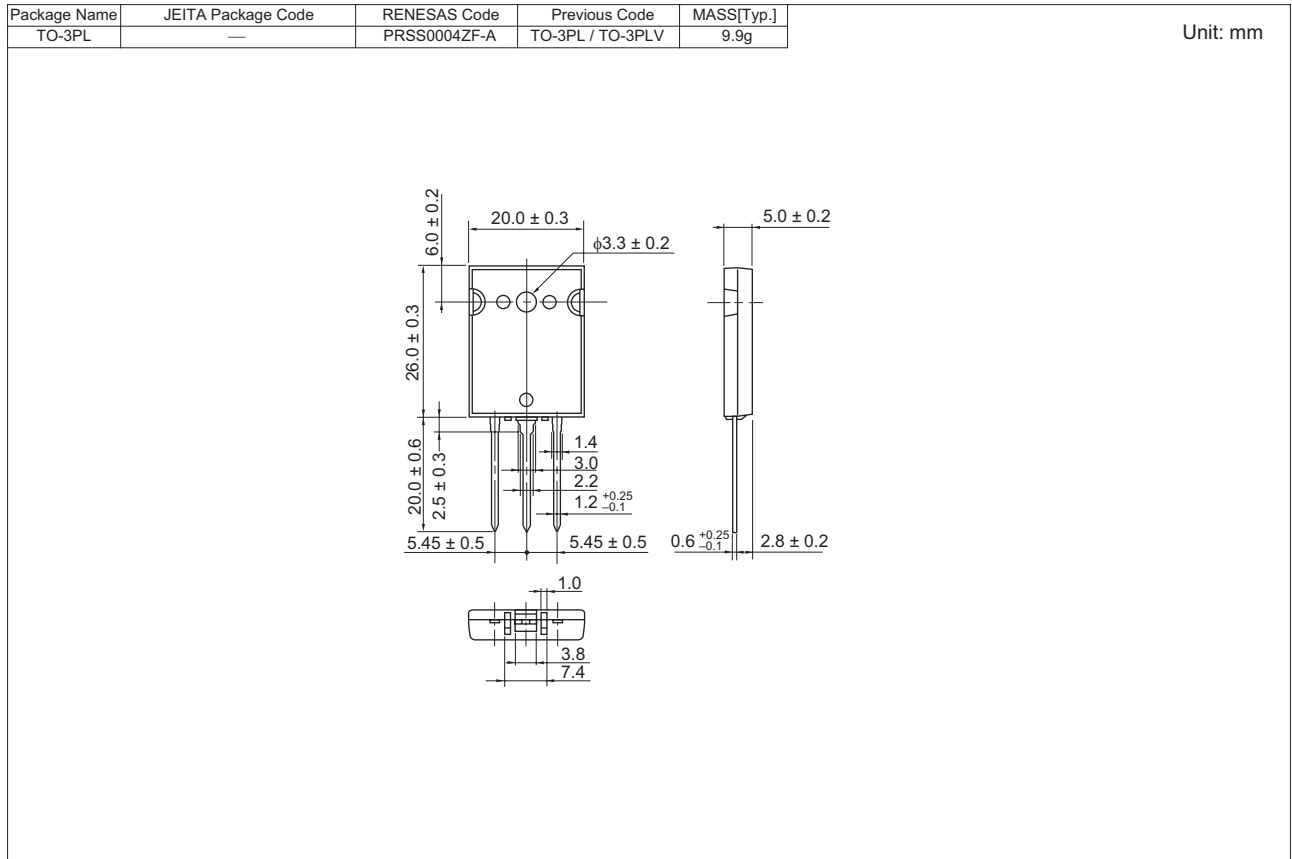
Switching Time Test Circuit



Waveform



Package Dimensions



Ordering Information

Part Name	Quantity	Shipping Container
H5N5005PL	100 pcs	Plastic case

Note: For some grades, production may be terminated. Please contact the Renesas sales office to check the state of production before ordering the product.

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Renesas Technology America, Inc.

450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology (Shanghai) Co., Ltd.

Unit 204, 205, AZIACenter, No.1233 Lujiazui Ring Rd, Pudong District, Shanghai, China 200120
Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7898

Renesas Technology Hong Kong Ltd.

7th Floor, North Tower, World Finance Centre, Harbour City, 1 Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2730-6071

Renesas Technology Taiwan Co., Ltd.

10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology Singapore Pte. Ltd.

1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd.

Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

Renesas Technology Malaysia Sdn. Bhd

Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510