MOS Field Effect Transistor
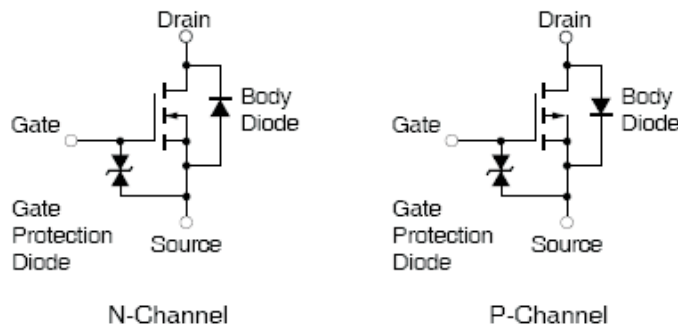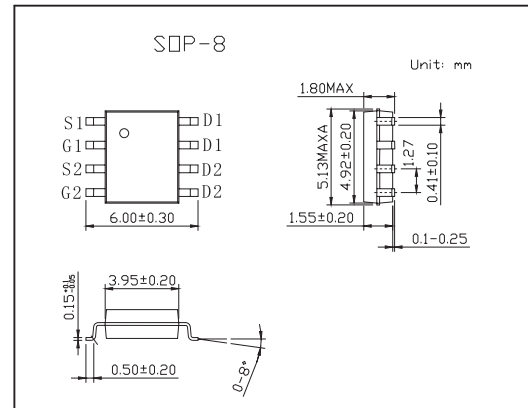
KPA1790

■ Features

● Dual chip type

● Low on-state resistance

N-channel $R_{DS(on)1}$ = 0.12 Ω TYP. (V_{GS} = 10 V, I_D = 0.5 A)

$R_{DS(on)2}$ = 1.19 Ω TYP. (V_{GS} = 4 V, I_D = 0.5 A)

● P-channel $R_{DS(on)1}$ = 0.45 Ω TYP. (V_{GS} = -10 V, I_D = -0.35 A)

$R_{DS(on)2}$ = 0.74 Ω TYP. (V_{GS} = -4 V, I_D = -0.35 A)

● Low input capacitance

N-channel C_{iss} = 180 pF TYP.

P-channel C_{iss} = 230 pF TYP.

● Built-in G-S protection diode

● Small and surface mount package

SOP-8

N-Channel   P-Channel

■ Absolute Maximum Ratings Ta = 25℃

Parameter	Symbol	N-Channel	P- Channel	Unit
Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	60	-60	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±20	±20	V
Drain Current (DC)	$I_{D(DC)}$	±1.0	±0.7	A
Drain Current (pulse) *1	$I_{D(pulse)}$	±4.0	±2.8	A
Total Power Dissipation (1 unit) *2	P_T	1.7		W
Total Power Dissipation (2 units) *2	P_T	2		W
Channel Temperature	T_{ch}	150		℃
Storage Temperature	T_{stg}	-55 to +150		℃
Single Avalanche Current *3	I_{AS}	0.5	-0.35	A
Single Avalanche Energy *3	E_{AS}	0.02	0.01	mJ

*1. PW ≤ 10 μs, Duty Cycle ≤ 1%

*2. Mounted on ceramic substrate of 2000 mm^2 X 2.25 mm

*3. Starting T_{ch} = 25℃, V_{DD} = 30 V, R_G = 25 Ω , V_{GS} = 20 → 0 V

KPA1790

■ Electrical Characteristics Ta = 25℃

Parameter	Symbol	Testconditons		Min	Typ	Max	Unit
Zero Gate Voltage Drain Current	I$_{DSS}$	V$_{DS}$ = 60 V, V$_{GS}$ = 0 V	N-Ch			10	μ A
		V$_{DS}$ = -60V, V$_{GS}$ = 0 V	P- Ch			-10	
Gate Leakage Current	I$_{GSS}$	V$_{GS}$ = ±16 V, V$_{DS}$ = 0 V	N-Ch			±10	μ A
		V$_{GS}$ = ±16 V, V$_{DS}$ = 0 V	P- Ch			±10	
Gate Cut-off Voltage	V$_{GS(off)}$	V$_{DS}$ = 10 V, I$_D$ = 1 mA	N-Ch	1.0	1.7	2.5	V
		V$_{DS}$ = -10 V, I$_D$ = -1 mA	P- Ch	-1.0	-1.7	-2.5	
Forward Transfer Admittance	| y$_{fs}$ |	V$_{DS}$ = 10 V, I$_D$ = 0.5 A	N-Ch	1.0	1.7		S
		V$_{DS}$ = -10 V, I$_D$ = -0.35A	P- Ch	5.0			
Drain to Source On-state Resistance	R$_{DS(on)1}$	V$_{GS}$ = 10 V, I$_D$ = 0.5 A	N-Ch		0.12	0.26	Ω
	R$_{DS(on)2}$	V$_{GS}$ = 4 V, I$_D$ = 0.5 A			0.19	0.34	Ω
	R$_{DS(on)1}$	V$_{GS}$ = -10 V, I$_D$ = -0.35 A	P- Ch		0.45	0.6	Ω
	R$_{DS(on)2}$	V$_{GS}$ = -4 V, I$_D$ = -0.35 A			0.74	1.1	Ω
Input Capacitance	C$_{iss}$	N-Channel	N-Ch		180		pF
		V$_{DS}$ = 10 V,V$_{GS}$ = 0 V,f = 1 MHz	P- Ch		230		
Output Capacitance	C$_{oss}$		N-Ch		100		pF
		P- Channel	P- Ch		100		
Reverse Transfer Capacitance	C$_{rss}$	V$_{DS}$ = -10 V,V$_{GS}$ = 0 V,f = 1 MHz	N-Ch		35		pF
			P- Ch		25		
Turn-on Delay Time	t$_{d(on)}$	N-Channel	N-Ch		1		ns
		V$_{DD}$ = 30 V, I$_D$ =0.5 A,V$_{GS}$ = 10 V	P- Ch		1.9		
Rise Time	t$_r$	R$_G$ = 10 Ω	N-Ch		1.4		ns
			P- Ch		1.7		
Turn-off Delay Time	t$_{d(off)}$	P- Channel	N-Ch		23		ns
		V$_{DD}$ = -30 V, I$_D$ = -0.35 A,V$_{GS}$ = -10 V	P- Ch		30		
Fall Time	t$_f$	R$_G$ = 10 Ω	N-Ch		17		ns
			P- Ch		15		
Total Gate Charge	Q$_G$	N-Channel	N-Ch		8		nC
		I$_D$ = 1.0 A,V$_{DD}$ = 48 V,V$_{GS}$ = 10 V	P- Ch		7.6		
Gate to Source Charge	Q$_{GS}$		N-Ch		1		nC
		P- Channel	P- Ch		1		
Gate to Drain Charge	Q$_{GD}$	I$_D$ = -0.7 A,V$_{DD}$ = -48 V,V$_{GS}$ = -10 V	N-Ch		3.5		nC
			P- Ch		2		
Body Diode Forward Voltage Note	V$_{F(S-D)}$	I$_F$ = 1.0 A, V$_{GS}$ = 0 V	N-Ch		0.75		V
		I$_F$ = 0.7 A, V$_{GS}$ = 0 V	P- Ch		0.85		
Reverse Recovery Time	t$_{rr}$	N-Channel	N-Ch		30		ns
		I$_F$ = 1.0A, V$_{GS}$ = 0 V,di/dt = 100 A/μ s	P- Ch		58		
Reverse Recovery Charge	Q$_{rr}$	P-Channel	N-Ch		33		nC
		I$_F$ = 0.7A, V$_{GS}$ = 0 V,di/dt = 100 A/μ s	P- Ch		130		