

Silicon PNP Power Transistors

2SB552

DESCRIPTION

- With TO-3 package
- Complement to type 2SD552

APPLICATIONS

- Power amplifier applications
- Power switching applications
- DC-DC converters

PINNING(see Fig.2)

PIN	DESCRIPTION
1	Base
2	Emitter
3	Collector

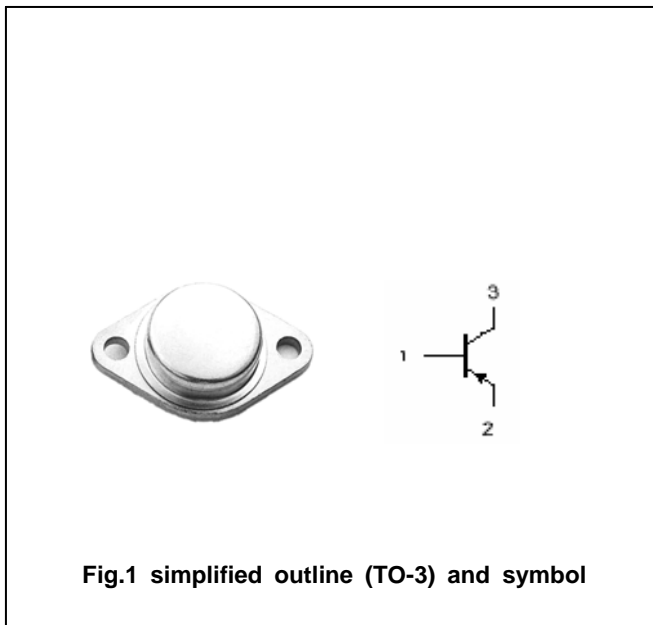


Fig.1 simplified outline (TO-3) and symbol

Absolute maximum ratings(Ta=°C)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V _{CBO}	Collector-base voltage	Open emitter	-220	V
V _{CEO}	Collector-emitter voltage	Open base	-180	V
V _{EBO}	Emitter-base voltage	Open collector	-5	V
I _C	Collector current		-15	A
I _B	Base current		-4	A
P _C	Collector power dissipation	T _C =25°C	150	W
T _j	Junction temperature		150	°C
T _{stg}	Storage temperature		-55~200	°C

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CHARACTERISTICS

T_j=25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V _{(BR)CEO}	Collector-emitter breakdown voltage	I _C =-25mA ; I _B =0	-180			V
V _{CEsat}	Collector-emitter saturation voltage	I _C =-10A; I _B =-1A			-2.0	V
V _{BEsat}	Base-emitter saturation voltage	I _C =-10A; I _B =-1A			-2.5	V
I _{CBO}	Collector cut-off current	V _{CB} =-220V; I _E =0			-0.1	mA
I _{EBO}	Emitter cut-off current	V _{EB} =-5V; I _C =0			-0.1	mA
h _{FE}	DC current gain	I _C =-5A ; V _{CE} =-5V	25		80	
C _{OB}	Output capacitance	I _E =0 ; V _{CB} =-10V; f=1.0MHz		300		pF
f _T	Transition frequency	I _C =-1A ; V _{CE} =-10V		3.5		MHz

PACKAGE OUTLINE

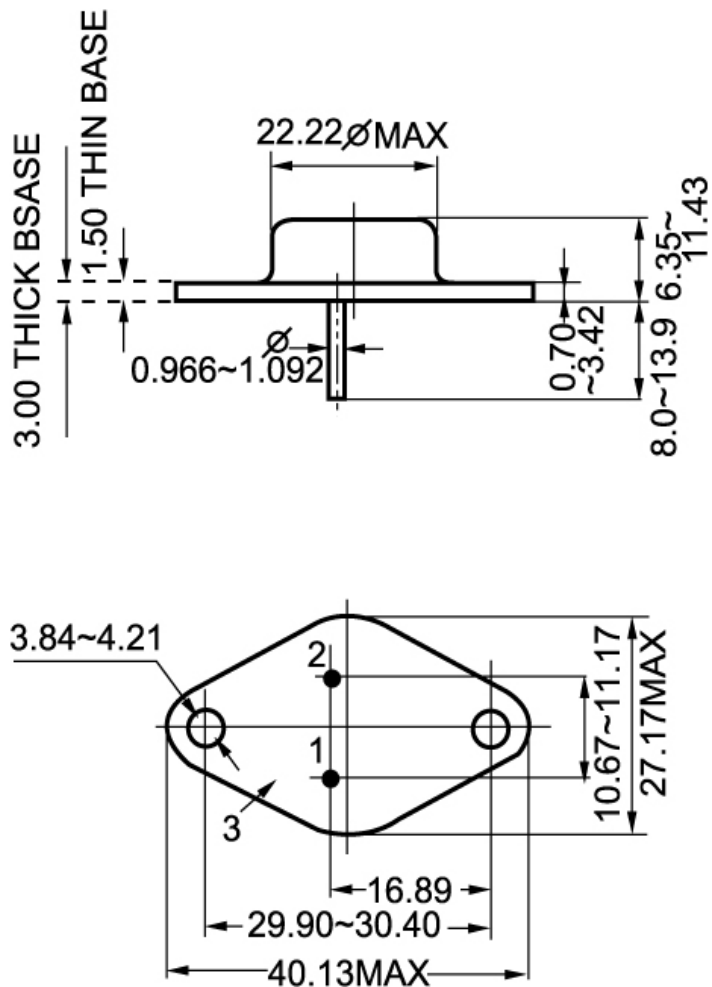


Fig.2 outline dimensions (unindicated tolerance: $\pm 0.1\text{mm}$)