

HD74SSTV16857A

1:1 14-bit SSTL_2 Registered Buffer

REJ03D0831-0100
(Previous: ADE-205-695)
Rev.1.00
Apr 07, 2006

Description

The HD74SSTV16857A is a 14-bit registered buffer designed for 2.3 V to 2.7 V V_{CC} operation and LVCMOS reset ($\overline{\text{RESET}}$) input / SSTL_2 data (D) inputs and CLK input.

Data flow from D to Q is controlled by differential clock pins (CLK, $\overline{\text{CLK}}$) and the $\overline{\text{RESET}}$. Data is triggered on the positive edge of the positive clock (CLK), and the negative clock ($\overline{\text{CLK}}$) must be used to maintain noise margins. When $\overline{\text{RESET}}$ is low, all registers are reset and all outputs are low.

To ensure defined outputs from the register before a stable clock has been supplied, $\overline{\text{RESET}}$ must be held in the low state during power up.

Features

- Supports LVCMOS reset ($\overline{\text{RESET}}$) input / SSTL_2 data (D) inputs and CLK input
- Differential SSTL_2 (Stub series terminated logic) CLK signal
- Flow through architecture optimizes PCB layout
- Ordering Information

Part Name	Package Type	Package Code (Previous code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74SSTV16857ATEL	TSSOP-48 pin	PTSP0048KA-A (TTP-48DBV)	T	EL (1,000 pcs / Reel)
HD74SSTV16857ANEL	TVSOP-48 pin	PTSP0048LA-A (TTP-48DEV)	N	EL (1,000 pcs / Reel)

Note: Please consult the sales office for the above package availability.

Function Table

Inputs				Output Q
$\overline{\text{RESET}}$	$\overline{\text{CLK}}$	CLK	D	
L	X	X	X	L
H	↓	↑	H	H
H	↓	↑	L	L
H	L or H	H or L	X	Q ₀ ^{*1}

H : High level

L : Low level

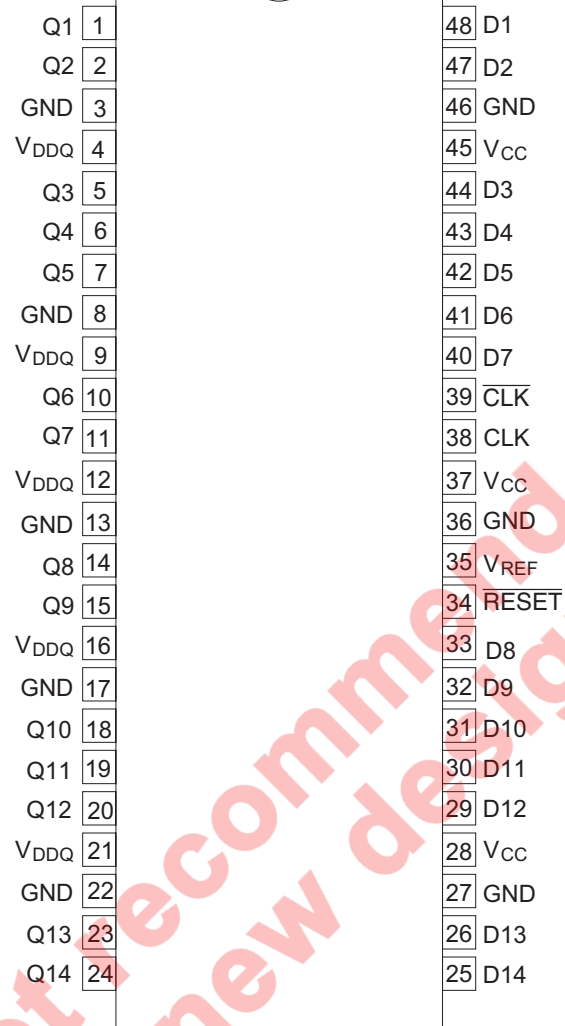
X : Immaterial

↑ : Low to high transition

↓ : High to low transition

Note: 1. Output level before the indicated steady state input conditions were established.

Pin Arrangement



(Top view)

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC} or V_{DDQ}	-0.5 to 3.6	V	
Input voltage ^{*1}	V_I	-0.5 to $V_{DDQ}+0.5$	V	
Output voltage ^{*1, 2}	V_O	-0.5 to $V_{DDQ}+0.5$	V	
Input clamp current	I_{IK}	±50	mA	$V_I < 0$ or $V_I > V_{CC}$
Output clamp current	I_{OK}	±50	mA	$V_O < 0$ or $V_O > V_{DDQ}$
Continuous output current	I_O	±50	mA	$V_O = 0$ to V_{DDQ}
V_{CC} , V_{DDQ} or GND current / pin	I_{CC} , I_{DDQ} or I_{GND}	±100	mA	
Maximum power dissipation at $T_a = 55^\circ\text{C}$ (in still air)	P_T	115	$^\circ\text{C} / \text{W}$	TSSOP
Storage temperature	T_{stg}	-65 to +150	$^\circ\text{C}$	

Notes: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

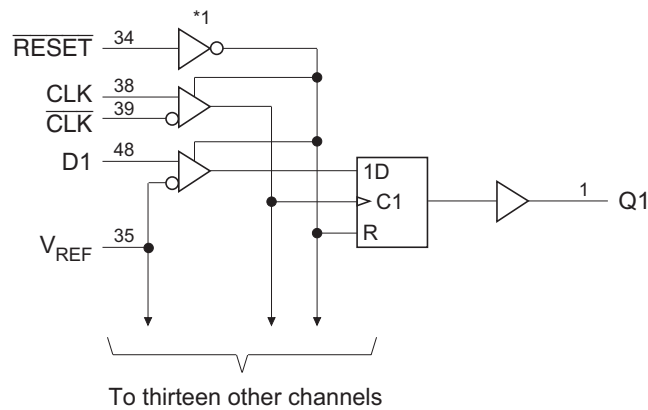
1. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
2. This current will flow only when the output is in the high state and $V_O > V_{DDQ}$.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit	Conditions
Supply voltage	V_{CC}	V_{DDQ}	2.5	2.7	V	
Output supply voltage	V_{DDQ}	2.3	2.5	2.7	V	
Reference voltage	V_{REF}	1.15	1.25	1.35	V	$V_{REF} = 0.5 \times V_{DDQ}$
Termination voltage	V_{TT}	$V_{REF}-40 \text{ mV}$	V_{REF}	$V_{REF}+40 \text{ mV}$	V	
Input voltage	V_I	0	—	V_{CC}	V	
AC high level input voltage	V_{IH}	$V_{REF}+310 \text{ mV}$	—	—	V	D
AC low level input voltage	V_{IL}	—	—	$V_{REF}-310 \text{ mV}$	V	D
DC high level input voltage	V_{IH}	$V_{REF}+150 \text{ mV}$	—	—	V	D
DC low level input voltage	V_{IL}	—	—	$V_{REF}-150 \text{ mV}$	V	D
High level input voltage	V_{IH}	1.7	—	$V_{DDQ}+0.3$	V	RESET
Low level input voltage	V_{IL}	-0.3	—	0.7	V	RESET
Differential input voltage	(Common mode range)	V_{CMR}	0.97	1.53	V	CLK, CLK
	(Minimum peak to peak input)	V_{PP}	360	—	mV	CLK, CLK
High level output current	I_{OH}	—	—	-20	mA	
Low level output current	I_{OL}	—	—	20	mA	
Operating temperature	T_a	0	—	70	$^\circ\text{C}$	

Note: The RESET input of the device must be held at V_{DDQ} or GND to ensure proper device operation. The differential inputs must not be floating, unless RESET is low.

Logic Diagram



Note: 1. $\overline{\text{RESET}}$ input gate is connected to V_{DDQ} .

Electrical Characteristics

Item	Symbol	V_{CC} (V)	Min	Typ	Max	Unit	Test Conditions
Input diode voltage	V_{IK}	2.3	—	—	-1.2	V	$I_{\text{IN}} = -18 \text{ mA}$
Output voltage	V_{OH}	2.3 to 2.7	$V_{\text{CC}} - 0.2$	—	—	V	$I_{\text{OH}} = -100 \mu\text{A}$
		2.3	1.95	—	V_{DDQ}		$I_{\text{OH}} = -16 \text{ mA}$
	V_{OL}	2.3 to 2.7	—	—	0.2		$I_{\text{OL}} = 100 \mu\text{A}$
		2.3	0	—	0.35		$I_{\text{OL}} = 16 \text{ mA}$
Input current (All inputs)	I_{IN}	2.7	—	—	± 5	μA	$V_{\text{IN}} = 2.7 \text{ V or } 0$
Quiescent supply current	I_{CC}^{*2}	2.7	—	25	45	mA	$V_{\text{IN}} = V_{\text{IH(AC)}} \text{ or } V_{\text{IL(AC)}}, I_{\text{O}} = 0$
Standby current	$I_{\text{CC}}(\text{stdy})$	2.7	—	—	10	μA	$\overline{\text{RESET}} = \text{GND}$
Dynamic operating clock only	I_{CCD}^{*2}	2.7	—	38	45	$\mu\text{A}/$ clock MHz	$\overline{\text{RESET}} = V_{\text{CC}},$ $V_{\text{I}} = V_{\text{IH(AC)}} \text{ or } V_{\text{IL(AC)}},$ CLK and $\overline{\text{CLK}}$ switching 50% duty cycle
Dynamic operating per each data input	I_{CCD}^{*2}	2.7	—	11	15	$\mu\text{A}/$ clock MHz/ data input	$\overline{\text{RESET}} = V_{\text{CC}},$ $V_{\text{I}} = V_{\text{IH(AC)}} \text{ or } V_{\text{IL(AC)}},$ CLK and $\overline{\text{CLK}}$ switching 50% duty cycle. One data input switching at half clock frequency, 50% duty cycle.
Output high ^{*3}	r_{OH}	2.3 to 2.7	7	—	20^{*4}	Ω	$I_{\text{OH}} = -20 \text{ mA}$
Output low ^{*3}	r_{OL}	2.3 to 2.7	7	—	20^{*4}	Ω	$I_{\text{OL}} = 20 \text{ mA}$
$ r_{\text{OH}} - r_{\text{OL}} $ each separate bit ^{*3}	$r_{\text{O}(\Delta)}$	2.5	—	—	4	Ω	$I_{\text{O}} = 20 \text{ mA}, T_{\text{a}} = 25^\circ\text{C}$
Input capacitance	Data inputs	C_{IN}^{*1}	2.5	—	3.5	pF	$V_{\text{I}} = V_{\text{REF}} \pm 310 \text{ mV}$
	CLK and $\overline{\text{CLK}}$		2.5	—	3.5		$V_{\text{CMR}} = 1.25 \text{ V}, V_{\text{PP}} = 360 \text{ mV}$
	$\overline{\text{RESET}}$		—	3.0	—		$V_{\text{I}} = V_{\text{CC}} \text{ or } \text{GND}$

Notes: 1. All typical values are at $V_{\text{CC}} = 2.5 \text{ V}, T_{\text{a}} = 25^\circ\text{C}$.

2. Total $I_{\text{CC}}(\text{max}) = I_{\text{CC}} + \{I_{\text{CCD}}(\text{clock}) \times f(\text{clock})\} + \{I_{\text{CCD}}(\text{Data}) \times 1/2f(\text{clock}) \times 14\}$

3. This is effective in the case that it did terminate by resistance.

4. See figure. 1, 2.

Switching Characteristics

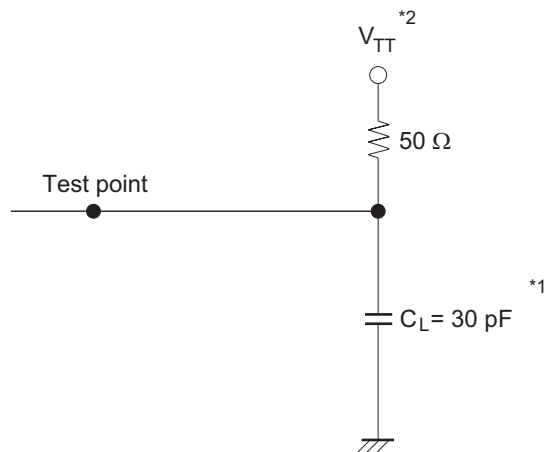
Item		Symbol	V _{CC} = 2.5 ± 0.2 V		Unit	Test Condition
			Min	Max		
Clock frequency ^{*1}		f _{clock}	—	200	MHz	
Setup time	Fast slew rate ^{*4, 6}	t _{su}	0.75	—	ns	Data before CLK↑, $\overline{\text{CLK}}$ ↓
	Slow slew rate ^{*5, 6}		0.9	—		
Hold time	Fast slew rate ^{*4, 6}	t _h	0.75	—	ns	Data after CLK↑, $\overline{\text{CLK}}$ ↓
	Slow slew rate ^{*5, 6}		0.9	—		
Differential inputs active time		t _{act}	22	—	ns	Data inputs must be low after $\overline{\text{RESET}}$ high.
Differential inputs inactive time		t _{inact}	22	—	ns	Data and clock inputs must be held at valid levels (not floating) after $\overline{\text{RESET}}$ low.
Pulse width Output slew ^{*3}		t _w	2.5	—	ns	CLK, $\overline{\text{CLK}}$ "H" or "L"
		t _{SL}	1	4	volt/ns	

(C_L = 30 pF, R_L = 50 Ω, V_{REF} = V_{TT} = V_{DDQ} × 0.5)

Item	Symbol	V _{CC} = 2.5±0.2 V			Unit	FROM (Input)	TO (Output)
		Min	Typ	Max			
Maximum clock frequency	f _{max}	200	—	—	MHz		
Propagation delay time ^{*2}	t _{PLH} , t _{PHL}	1.1	—	2.8	ns	CLK, $\overline{\text{CLK}}$	Q
	t _{PHL}	—	—	5.0		$\overline{\text{RESET}}$	Q

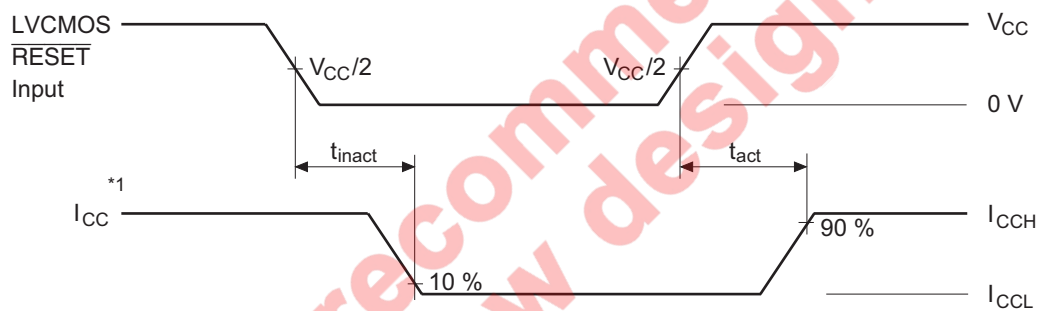
- Notes: 1. Although the clock is differential, all timing is relative to CLK going high and $\overline{\text{CLK}}$ going low.
2. This timing relationship is specified into test load (see waveforms – 3, 4) with all of the outputs switching.
3. Assumes into an equivalent, distributed load to the address net structure defined in the application information provided in this specification.
4. For data signal input slew rate ≥ 1 V/ns.
5. For data signal input slew rate ≥ 0.5 V/ns and < 1 V/ns.
6. CLK, $\overline{\text{CLK}}$ signals input slew rates are ≥ 1 V/ns.

Test Circuit

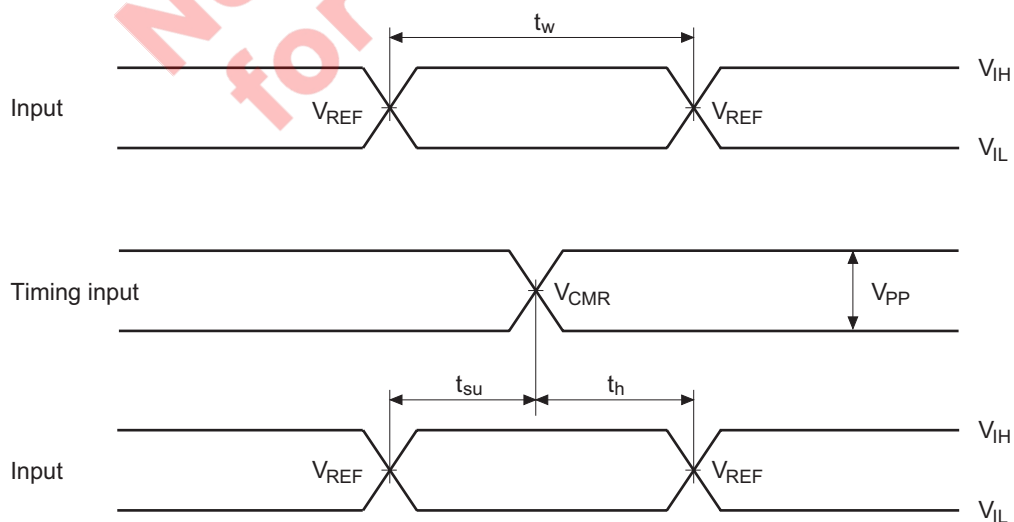


- Notes:
1. C_L includes probe and jig capacitance.
 2. $V_{TT} = V_{REF} = V_{DDQ} \times 0.5$

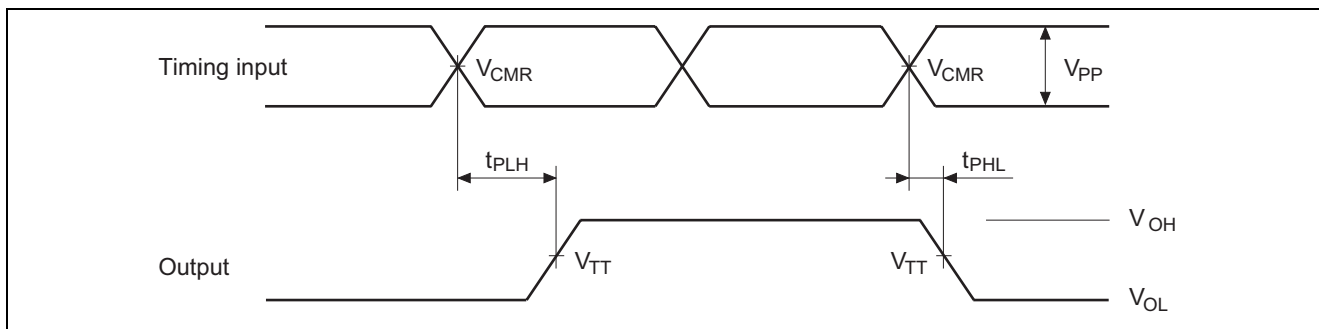
Waveforms – 1



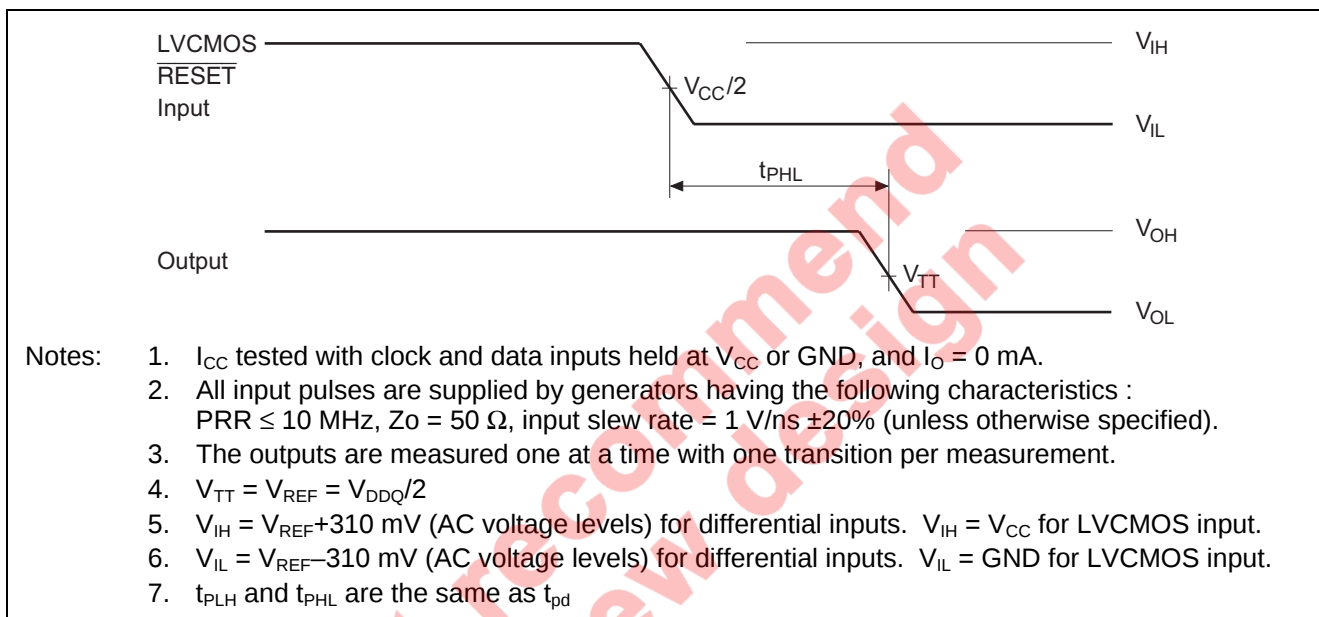
Waveforms – 2



Waveforms – 3



Waveforms – 4



Application Data

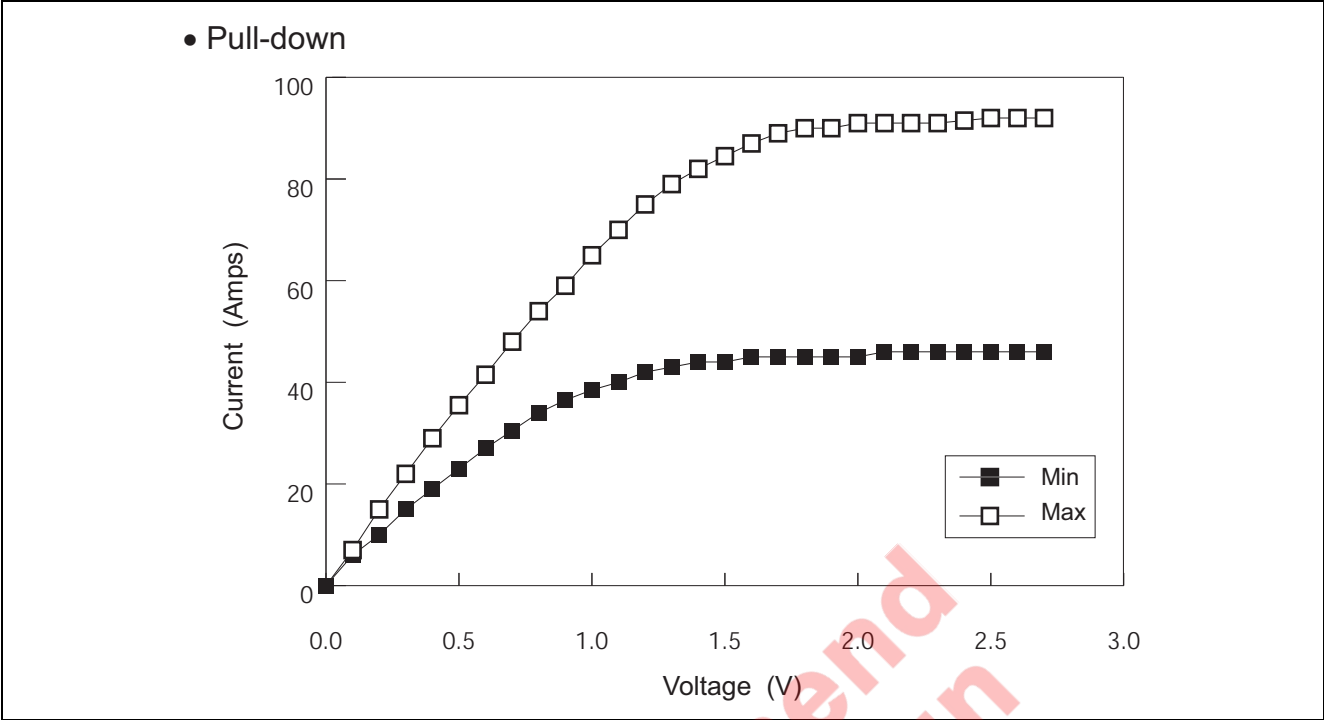


Figure 1

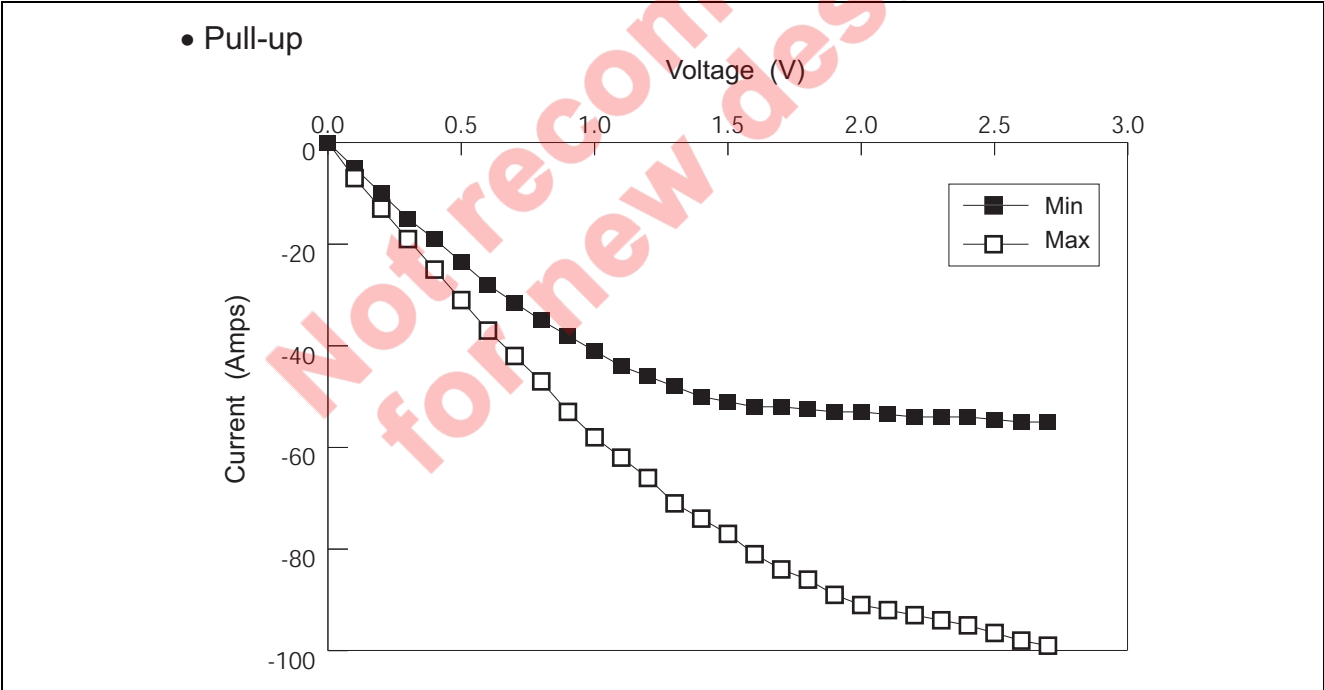
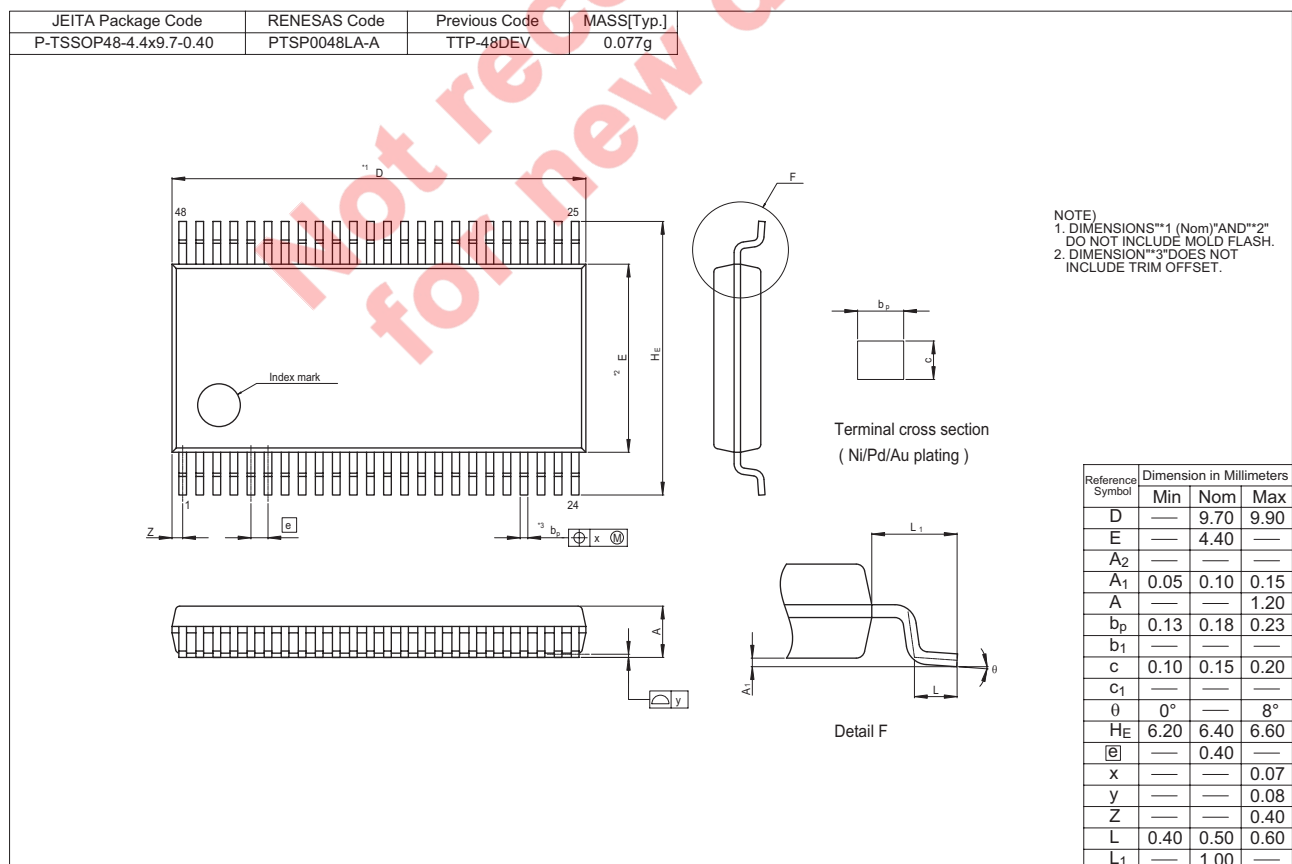
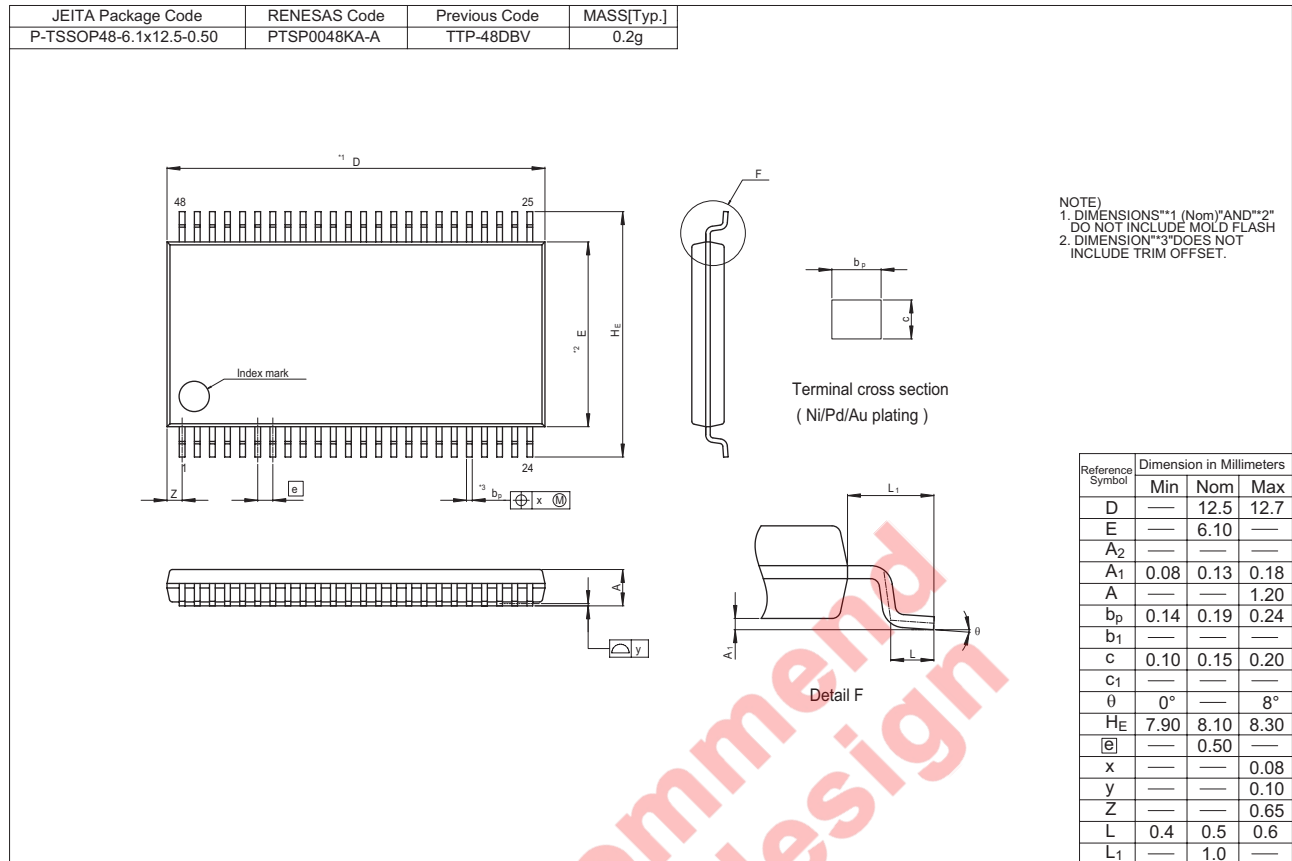


Figure 2

Curve Data

Voltage (V)	Pull-down		Pull-up	
	I (mA)	I (mA)	I (mA)	I (mA)
	Min	Max	Min	Max
0.0	0	0	0	0
0.1	6	7	-6	-7
0.2	11.5	15	-11.5	-13
0.3	16	22	-16	-19
0.4	20	29	-20	-25
0.5	23	35.5	-23.5	-31
0.6	27	41.5	-28	-37
0.7	30.5	48	-31.5	-42
0.8	34	54	-35	-47
0.9	36.5	59	-38	-53
1.0	38.5	65	-41	-58
1.1	40	70	-44	-62
1.2	42	75	-46	-66
1.3	43	79	-48	-71
1.4	44	82	-50	-74
1.5	44	84.5	-51	-77
1.6	45	87	-52	-81
1.7	45	89	-52	-84
1.8	45	90	-52.5	-86
1.9	45	90	-53	-89
2.0	45	91	-53	-91
2.1	46	91	-53.5	-92
2.2	46	91	-54	-93
2.3	46	91	-54	-94
2.4	46	91.5	-54	-95
2.5	46	92	-54.5	-96.5
2.6	46	92	-55	-98
2.7	46	92	-55	-99

Package Dimensions



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