

To all our customers

Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.

The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

8-BIT 8CH MULTIPLYING D-A CONVERTER WITH BUFFER AMPLIFIERS**DESCRIPTION**

The M62381FP is an integrated circuit semiconductor of CMOS structure with 8 channels of built-in 8-bit resolution multiplication type D-A converters.

The input data is a easy-to-use 3-wire serial transfer method and it is able to cascading serial use with Do terminal.

This device is capable of 4 quadrant multiplication because of built-in inverting type amplifier.

FEATURES

- Digital data transfer method
3-wire 12-bit serial data transfer method(DI,CLK,LD)
- High pressure proof(VDD±5V)
- Short setting time
- Built-in reset terminal,all the buffer amplifier outputs forces zero volts.

APPLICATION

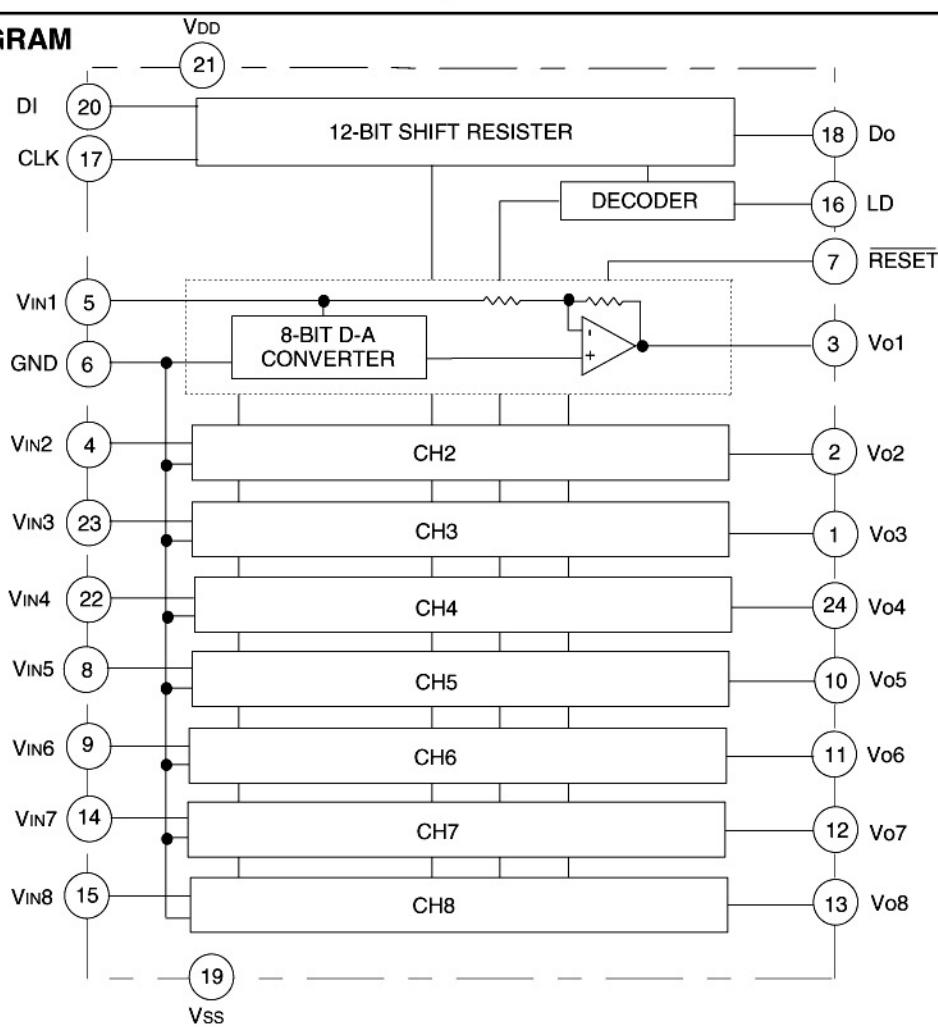
Signal gain control of DISPLAY-MONITOR or CTV.
Conversion from digital control data analog control data for form-use and industrial equipment.
Automatic adjustment by combination with EEPROM and micro-computer.
(replacement of conventional half-fixed resistor.)

PIN CONFIGURATION (TOP VIEW)

Vo3	1	○	24	Vo4
Vo2	2		23	VIN3
Vo1	3		22	VIN4
VIN2	4		21	VDD
VIN1	5		20	DI
GND	6		19	VSS
RESET	7		18	Do
VIN5	8		17	CLK
VIN6	9		16	LD
Vo5	10		15	VIN8
Vo6	11		14	VIN7
Vo7	12		13	Vo8

M62381FP

Outline 24P2V-A

BLOCK DIAGRAM

8-BIT 8CH MULTIPLYING D-A CONVERTER WITH BUFFER AMPLIFIERS**EXPLANATION OF TERMINALS**

Pin No.	Symbol	Function
(20)	DI	Serial data input terminal
(18)	DO	Serial data output terminal
(17)	CLK	Serial clock input terminal
(16)	LD	When LD terminal level is "H",latch circuit data is load
(3)	Vo1	
(2)	Vo2	
(1)	Vo3	8-bit resolution D-A converter output terminal
(24)	Vo4	
(10)	Vo5	
(11)	Vo6	
(12)	Vo7	
(13)	Vo8	
(21)	V _{DD}	Analog and digital common power supply terminal
(19)	V _{SS}	Analog negative power supply terminal
(6)	GND	GND terminal
(5)	V _{IN1}	
(4)	V _{IN2}	
(23)	V _{IN3}	
(22)	V _{IN4}	D-A converter reference input terminal
(8)	V _{IN5}	
(9)	V _{IN6}	
(14)	V _{IN7}	
(15)	V _{IN8}	
(7)	RESET	When RESET terminal level is "H",all D-A output terminal became "0V"

8-BIT 8CH MULTIPLYING D-A CONVERTER WITH BUFFER AMPLIFIERS**DIGITAL DATA FORMAT**LAST
LSBFIRST
MSB

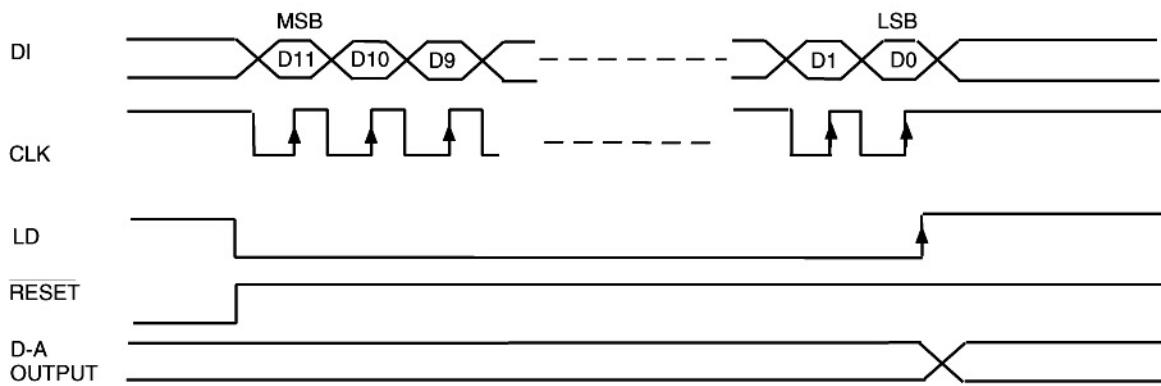
D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11
DAC DATA											DAC SELECT DATA

(1) DAC set up data

D7	D6	D5	D4	D3	D2	D1	D0	D-A output
0	0	0	0	0	0	0	0	-V _{IN}
0	0	0	0	0	0	0	1	(1/128-1) X V _{IN}
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
0	1	1	1	1	1	1	1	(127/128-1) X V _{IN}
1	0	0	0	0	0	0	0	(128/128-1) X V _{IN}
1	0	0	0	0	0	0	1	(129/128-1) X V _{IN}
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	1	1	0	(254/128-1) X V _{IN}
1	1	1	1	1	1	1	1	(255/128-1) X V _{IN}

(2) DAC select data

MSB	D11	D10	D9	D8	LSB	DAC selection
0	0	0	0	0	Don't care	
0	0	0	1	ch1 selection		
0	0	1	0	ch2 selection		
⋮	⋮	⋮	⋮	⋮	⋮	⋮
0	1	1	1	ch7 selection		
1	0	0	0	ch8 selection		
1	0	0	1	Don't care		
⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	Don't care	

TIMING CHART (MODEL)

8-BIT 8CH MULTIPLYING D-A CONVERTER WITH BUFFER AMPLIFIERS**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Conditions	Ratings	Unit
V _{DD}	Supply voltage		-0.3 to +6.0	V
V _{IN}	Digital input voltage		-0.3 to +6.0	V
V _{SS}	Analog negative supply voltage		-6.0 to +3.0	V
V _{IN}	Input voltage		V _{SS} +0.3 to V _{DD} -0.3	V
V _O	Output voltage		V _{SS} +0.3 to V _{DD} -0.3	V
T _{OPR}	Operating temperature		-20 to +85	°C
T _{STG}	Storage temperature		-40 to +125	°C

ELECTRICAL CHARACTERISTICS**Digital part**(V_{DD}=+5V, V_{SS}=-5V, V_{DD}≥V_{IN}≥V_{SS}, GND=0V, Ta=-20 to +85°C,unless otherwise noted)

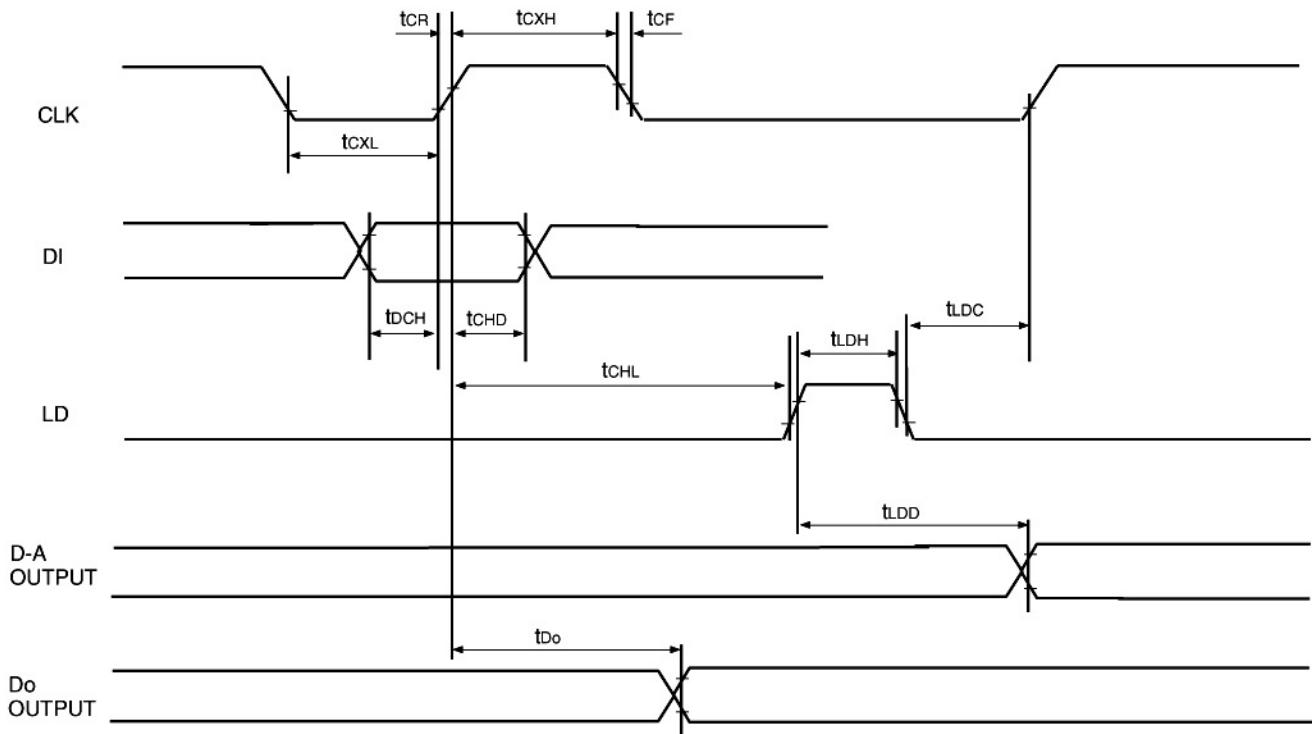
Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V _{DD}	Supply voltage		4.5	5.0	5.5	V
I _{ILK}	Input leak current	V _{IN} =0 to V _{CC}	-10		10	μA
V _{IL}	Input low voltage				0.2V _{DD}	V
V _{IH}	Input high voltage		0.8V _{DD}			V
V _{OL}	Output low voltage	I _{OL} =2.5mA			0.4	V
V _{OH}	Output high voltage	I _{OH} =-400μA	V _{DD} -0.4			V

Analog part(V_{DD}=+5V, V_{SS}=-5V, V_{DD}≥V_{IN}≥V_{SS}, GND=0V, Ta=-20 to +85°C,unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
I _{IN}	D-A converter reference input current		0.2	0.4	0.4	mA
V _{AO}	Buffer amplifier output voltage range	I _{AO} =±500μA	V _{A0ZERO} +0.15		V _{A0FULL} -0.15	V
		I _{AO} =±1mA	V _{A0ZERO} +0.3		V _{A0FULL} -0.3	
I _{AO}	Buffer amplifier output current range	V _{AO} =V _{A0ZERO} +0.3 to V _{A0FULL} -0.3	-1.0		1.0	mA
RES	Resolution		8			bit
DNL	Differential nonlinearity		-1.0		1.0	LSB
NL	Nonlinearity	V _{DD} -0.5≥V _{IN} ≥V _{SS} +0.5	-1.5		1.5	LSB
EG	Gain error		-3		3	%FS

AC CHARACTERISTICS

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t _{CXL}	Clock "L"pulse width		200			ns
t _{CXH}	Clock "H"pulse width		200			ns
t _{CR}	Clock rise time				200	ns
t _{CF}	Clock fall time				200	ns
t _{DCD}	Data set up time		30			ns
t _{CHD}	Data hold time		60			ns
t _{CHL}	LD set up time		200			ns
t _{LHD}	LD hold time		100			ns
t _{LDC}	LD "H" pulse width		100			ns
t _{DO}	Data output delay time	C _L =100pF	70		350	ns
t _{LDD}	D-A output setting time	Without load				ns

8-BIT 8CH MULTIPLYING D-A CONVERTER WITH BUFFER AMPLIFIERS**TIMING CHART****APPLICATION EXAMPLE**