

# M62382FP

## 5 V Type 12-bit 4ch Composite Multiplying D/A Converter

REJ03D0882-0300

Rev.3.00

Mar 25, 2008

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### Description

The M62382FP is a semiconductor integrated circuit of 5 V CMOS structure with 12-bit 4 channels of built-in multiplying D/A converters and 8-bit 8 channels of built-in multiplying D/A converters. 8-bit D/A converters, when used in combination with 12-bit D/A converters, can operate in a wider range. Parallel data input under the 2 modes (A, B) of channel assignment allows for easier usage.

### Features

- Built-in low power 12-bit 4 channels D/A converters
- 8-bit D/A converter with buffer making full swing between  $V_{CC}$  and GND.
- 2 modes (A, B) of channel assignment
- Zero level function

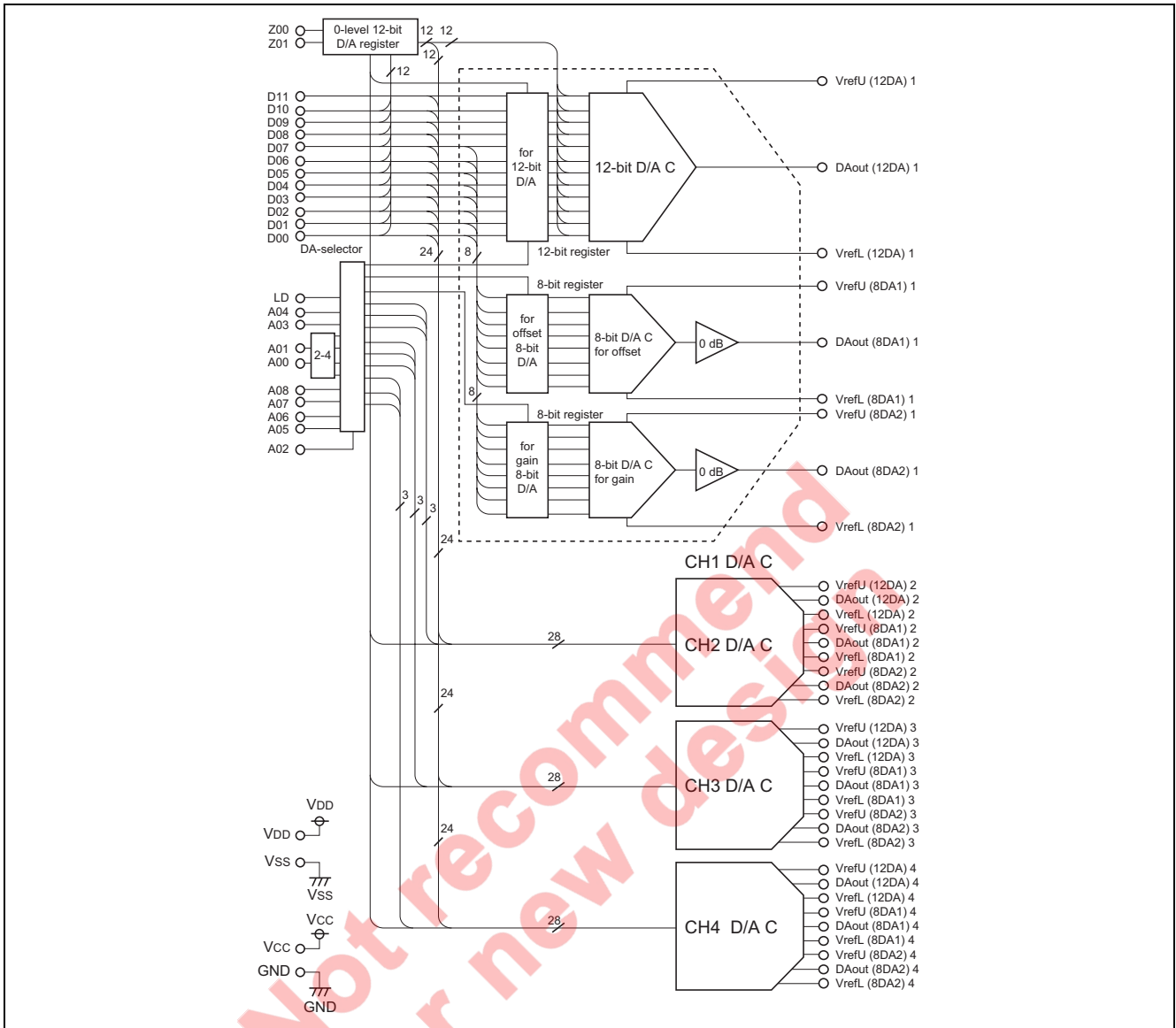
Built-in function of retaining arbitrary assigned data in 12-bit D/A converter. In normal use, output voltage can be switched to the voltage corresponding to the formerly assigned data by the setting of Z01, making it possible to calibrate the data (output voltage value).

### Application

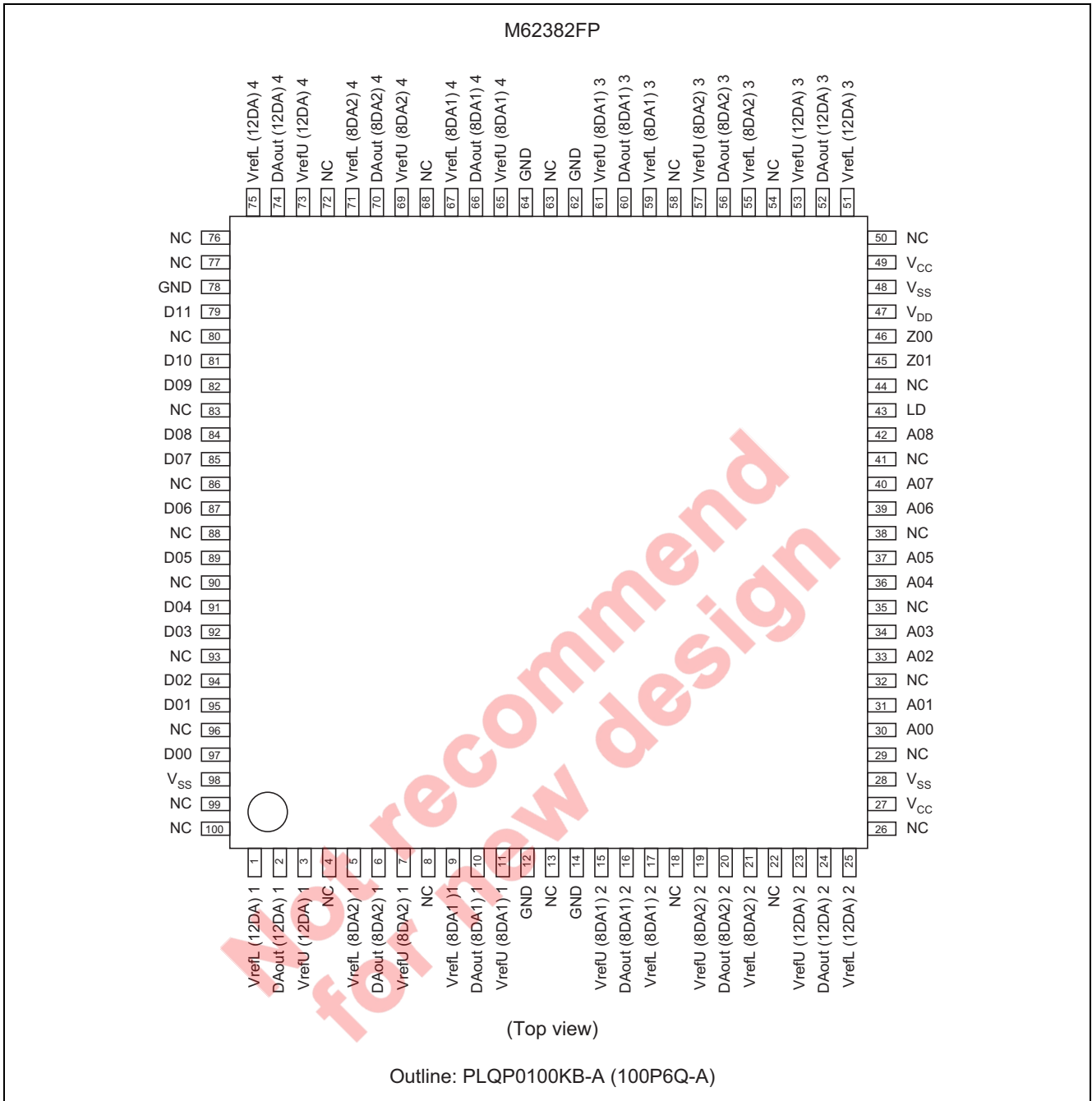
High precision measurement equipments such as memory testers, industrial measurement equipments, medical equipments, standard equipments in general

Not recommended  
for new design

Block Diagram



Pin Arrangement



## Pin Description

Pin No.	Pin Name	Function
1, 25, 51, 75	VrefL (12)	12-bit D/A converter lower reference voltage input terminal
2, 24, 52, 74	DAout (12)	12-bit D/A converter output terminal
3, 23, 53, 73	VrefU (12)	12-bit D/A converter upper reference voltage input terminal
5, 9, 17, 21, 55, 59, 67, 71	VrefL (8)	8-bit D/A converter lower reference voltage input terminal
6, 10, 16, 20, 56, 60, 66, 70	DAout (8)	8-bit D/A converter output terminal
7, 11, 15, 19, 57, 61, 65, 69	VrefU (8)	8-bit D/A converter upper reference voltage input terminal
27, 49	V <sub>CC</sub>	Analog power supply terminal
12, 14, 62, 64, 78	GND	Analog GND terminal
47	V <sub>DD</sub>	Digital power supply terminal
28, 48, 98	V <sub>SS</sub>	Digital GND terminal
30, 31, 33, 34, 36, 37, 39, 40, 42	A00 to A08	Address terminal
79, 81, 82, 84, 85, 87, 89, 91, 92, 94, 95, 97	D00 to D11	D/A data terminal
43	LD	D/A LD terminal
46	Z00	Zero level data assignment terminal
45	Z01	Zero level data load terminal
4, 8, 13, 18, 22, 29, 32, 35, 38, 41, 44, 50, 54, 58, 63, 68, 72, 76, 77, 80, 83, 86, 88, 90, 93, 96, 99, 100	NC	Non-connection

## Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Digital supply voltage	V <sub>DD</sub>	-0.3 to +7.0	V
Analog supply voltage	V <sub>CC</sub>	-0.3 to +7.0	V
Digital input voltage	V <sub>DIN</sub>	-0.3 to V <sub>DD</sub> + 0.3 ≤ 7.0	V
D/A reference voltage	V <sub>ref</sub>	-0.3 to V <sub>DD</sub> + 0.3 ≤ 7.0	V
D/A output voltage	V <sub>DAout</sub>	-0.3 to V <sub>DD</sub> + 0.3 ≤ 7.0	V
Operating temperature	Topr	-20 to +85	°C
Storage temperature	Tstr	-40 to +125	°C

## Electrical Characteristics

### <Digital Part>

( $V_{DD} = V_{CC} = 5\text{ V}$ ,  $V_{SS} = \text{GND} (= 0\text{ V})$ ,  $V_{refU} = V_{CC}$ ,  $V_{refL} = \text{GND}$ ,  $T_a = -20\text{ to }+85^\circ\text{C}$ , unless otherwise noted.)

Item	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Digital supply current	$I_{DD}$	—	—	3.0	mA	$f_{LD} = 1\text{ MHz}$ , $V_{DIN} = V_{SS}$ , or $V_{DD}$
Input leak current	$I_{ILK}$	-10	—	+10	$\mu\text{A}$	$V_{DIN} = V_{SS}$ to $V_{DD}$
Input capacitive load	$C_{IN}$	—	—	1.2	pF	

### <Analog Part>

( $V_{DD} = V_{CC} = 5\text{ V}$ ,  $V_{SS} = \text{GND} (= 0\text{ V})$ ,  $V_{refU} = V_{CC}$ ,  $V_{refL} = \text{GND}$ ,  $T_a = -20\text{ to }+85^\circ\text{C}$ , unless otherwise noted.)

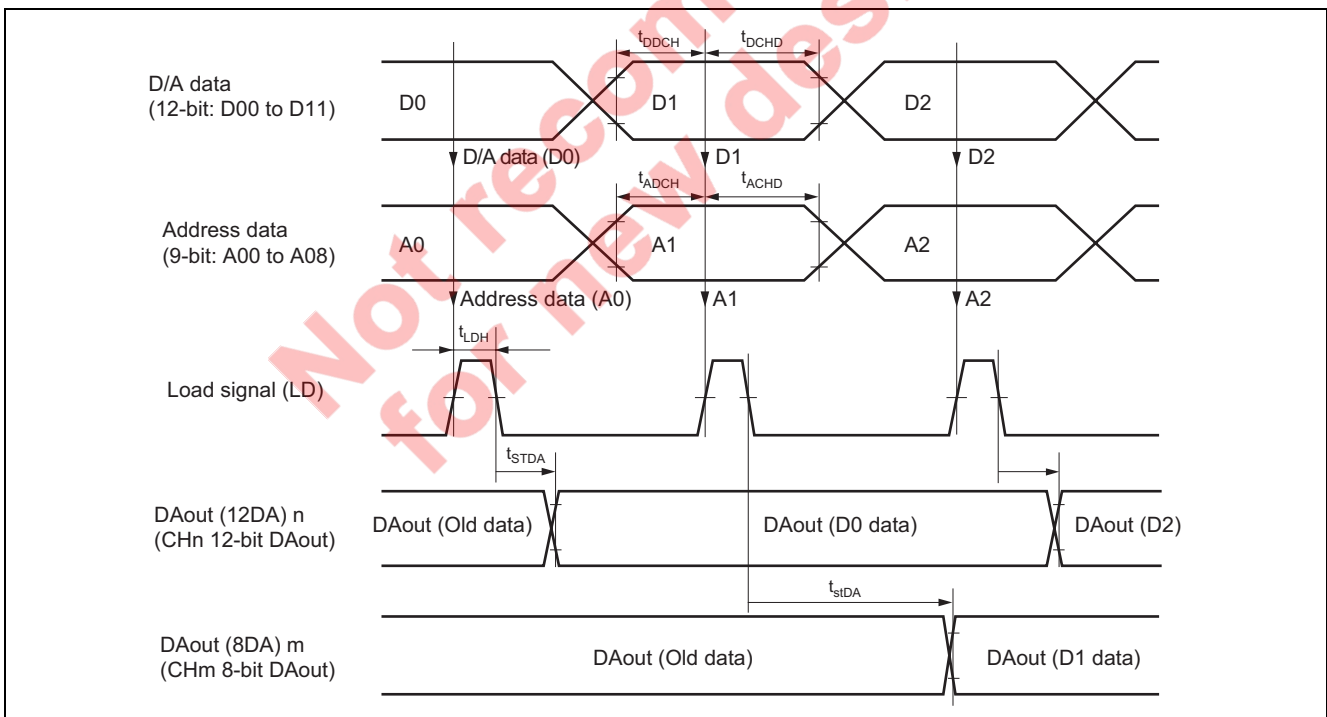
Item	Symbol	Limits			Unit	Conditions	
		Min	Typ	Max			
Analog supply current	$I_{CC}$	—	1.6	6.0	mA	D/A output = 1/2 MSB	
Reference current for D/A converter (U to L)	$I_{ref}$	—	0.7	2.0	mA	12-bit D/A	D/A data for maximum current of D/A reference, each circuit current from $V_{refU}$ to $V_{refL}$
		—	0.1	0.4	mA	8-bit D/A	
Buffer amplifier output drive range	$I_{OA}$	$\pm 1.5$	—	—	mA	Upper side saturation voltage = 0.3 V Lower side saturation voltage = 0.3 V	
Output resistance	$R_O$	—	2.2	—	k $\Omega$	12-bit D/A: R-2R ladder output	
		—	10	—	$\Omega$	8-bit D/A: Buffer amplifier output	
Differential nonlinearity error	$S_{DL}$	-1.5	—	+1.5	LSB	12-bit D/A	$V_{refU} = 5.0\text{ V}$ , $V_{refL} = 0.0\text{ V}$ $T_a = 25^\circ\text{C}$
		-1.0	—	+1.0		8-bit D/A	
Nonlinearity error	$S_{NL}$	-2.0	—	+2.0	LSB	12-bit D/A	$V_{refU} = 5.0\text{ V}$ , $V_{refL} = 0.0\text{ V}$ $T_a = 25^\circ\text{C}$
		-1.0	—	+1.0		8-bit D/A	
Zero code error	$S_{ZERO}$	-3.0	—	+3.0	LSB	$V_{refU} = 5.0\text{ V}$ , $V_{refL} = 0.0\text{ V}$ $T_a = 25^\circ\text{C}$	
Full code error	$S_{FULL}$	-3.0	—	+3.0	LSB	$V_{refU} = 5.0\text{ V}$ , $V_{refL} = 0.0\text{ V}$ $T_a = 25^\circ\text{C}$	
Temperature coefficient of nonlinearity error	$\Delta\text{NL}/t$	—	—	0.05	LSB/ $^\circ\text{C}$	$V_{refU} = 5.0\text{ V}$ , $V_{refL} = 0.0\text{ V}$ $S_{NL\ 12\text{-bit D/A}} / 60^\circ\text{C}$ ( $T_a = 25\text{ to }85^\circ\text{C}$ )	
Cross talk between the channels	CT	—	75	—	dB	12-bit D/A	$V_{in} = -10\text{ dBm}$ $f = 100\text{ Hz to }1\text{ kHz}$
		—	65	—		8-bit D/A	
Power supply rejection ratio	PSRR	—	65	—	dB	12-bit D/A	$V_{CCin} = V_{CC} - 10\text{ dBm}$ $f = 100\text{ Hz to }1\text{ kHz}$
		—	55	—		8-bit D/A	
Temperature coefficient of D/A output	TCo	—	20	—	ppm/ $^\circ\text{C}$		
Settling time of 12-bit D/A	$t_{STDA}$	—	1.4	—	$\mu\text{s}$	Without load ( $I_{OA} = 0\text{ mA}$ )	
Settling time of 8-bit D/A	$t_{stDA}$	—	70	—	$\mu\text{s}$	Until output takes 1/2 LSB of the final value	

### Recommended Operating Condition

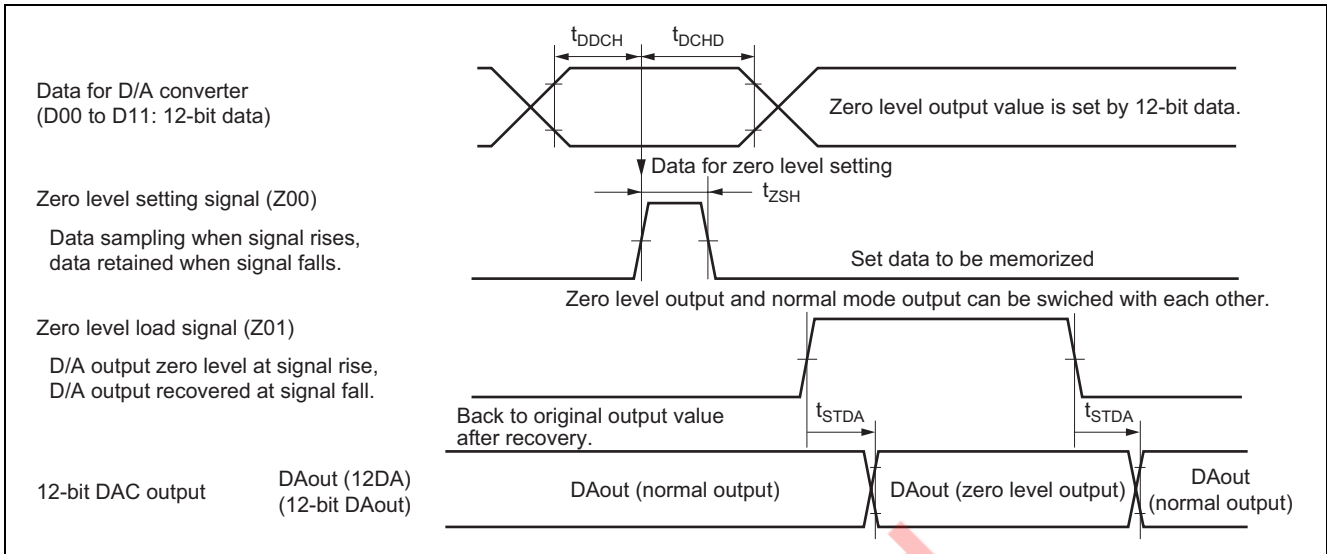
(Ta = 25 to 75°C)

Item	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Analog power supply voltage	V <sub>CC</sub>	4.5	5.0	5.5	V	
Digital power supply voltage	V <sub>DD</sub>	4.5	5.0	5.5	V	
H side D/A reference voltage	V <sub>refH</sub>	V <sub>CC</sub> - 0.5	—	V <sub>CC</sub>	V	
L side D/A reference voltage	V <sub>refL</sub>	GND	—	0.5	V	
H level digital input voltage	V <sub>IH</sub>	2	—	V <sub>DD</sub>	V	
L level digital input voltage	V <sub>IL</sub>	GND	—	0.8	V	
D/A data set up time	t <sub>DDCH</sub>	10	—	—	ns	Driving 12-bit and 8-bit D/A converters at same time
Address data set up time	t <sub>ADCH</sub>	150	—	—	ns	Driving 12-bit and 8-bit D/A converters at same time
D/A data hold time	t <sub>DCHD</sub>	t <sub>LDH</sub> + 35	—	—	ns	Driving 12-bit and 8-bit D/A converters at same time
Address data hold time	t <sub>ACHD</sub>	t <sub>LDH</sub> + 10	—	—	ns	Driving 12-bit and 8-bit D/A converters at same time
Load signal H level hold time	t <sub>LDH</sub>	100	—	—	ns	Driving 12-bit and 8-bit D/A converters at same time
Z00 signal H level hold time	t <sub>ZSH</sub>	15	—	—	ns	

### Timing Chart



## Zero Level Setting (input/output): Z00, Z01



## Digital Format

### 1. Channel Select Setting (A01, A02)

Setting Select	A01	A00
CH1 select	0	0
CH2 select	0	1
CH3 select	1	0
CH4 select	1	1

### 2. Channel Assign Mode Setting (A02)

Channel Assign Mode Setting	A02
A channel assign mode	0
B channel assign mode	1

### 3. 8-bit D/A Converter Select Setting (A03)

8-bit D/A Converter Select Setting	A03
D/A select for offset	0
D/A select for gain	1

### 4. D/A Converter Select Setting (A04)

D/A Converter Select Setting	A04
12-bit D/A converter select	0
8-bit D/A converter select	1

### 5. Channel Select Setting B (A05, A06, A07, A08)

Setting Select	A05	A06	A07	A08
CH1 select	1	0	0	0
CH2 select	0	1	0	0
CH3 select	0	0	1	0
CH4 select	0	0	0	1

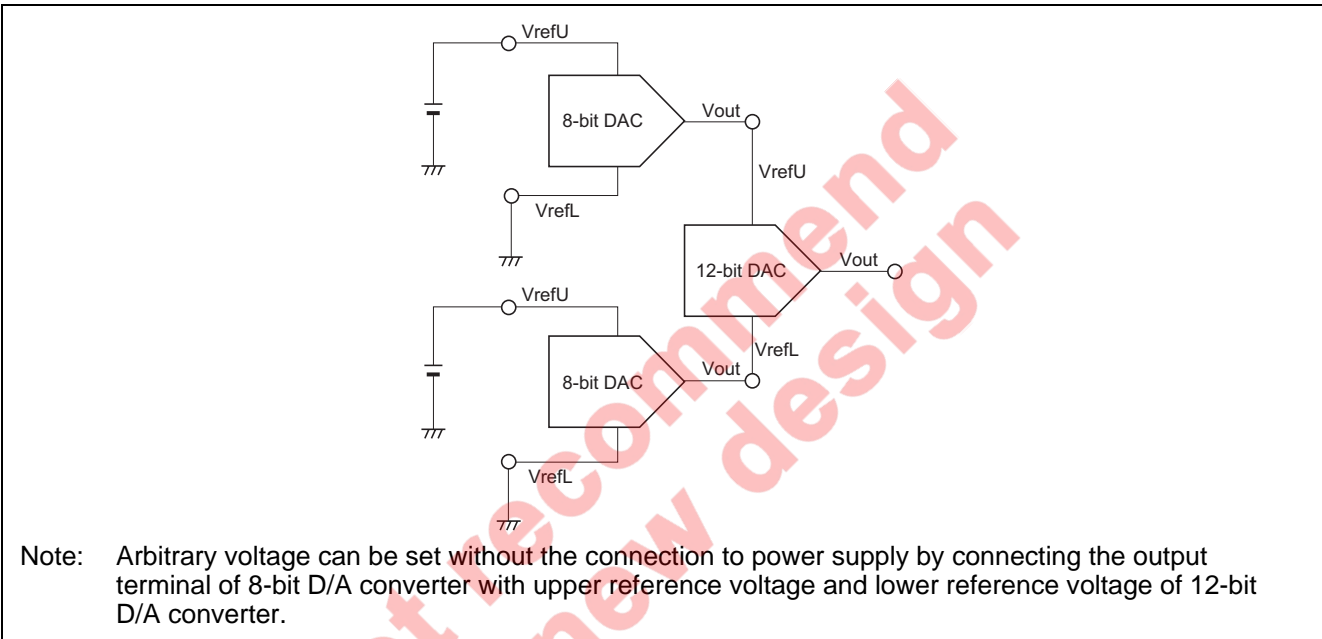
## 12-bit D/A

D00	D01	D02	D03	D04	D05	D06	D07	D08	D09	D10	D11	D/A Output
0	0	0	0	0	0	0	0	0	0	0	0	$V_{refL12}$
1	0	0	0	0	0	0	0	0	0	0	0	$(V_{refU12} - V_{refL12}) / 4096 \times 1$
0	1	0	0	0	0	0	0	0	0	0	0	$(V_{refU12} - V_{refL12}) / 4096 \times 2$
1	1	0	0	0	0	0	0	0	0	0	0	$(V_{refU12} - V_{refL12}) / 4096 \times 3$
:	:	:	:	:	:	:	:	:	:	:	:	:
0	0	1	1	1	1	1	1	1	1	1	1	$(V_{refU12} - V_{refL12}) / 4096 \times 4092$
1	0	1	1	1	1	1	1	1	1	1	1	$(V_{refU12} - V_{refL12}) / 4096 \times 4093$
0	1	1	1	1	1	1	1	1	1	1	1	$(V_{refU12} - V_{refL12}) / 4096 \times 4094$
1	1	1	1	1	1	1	1	1	1	1	1	$(V_{refU12} - V_{refL12}) / 4096 \times 4095$

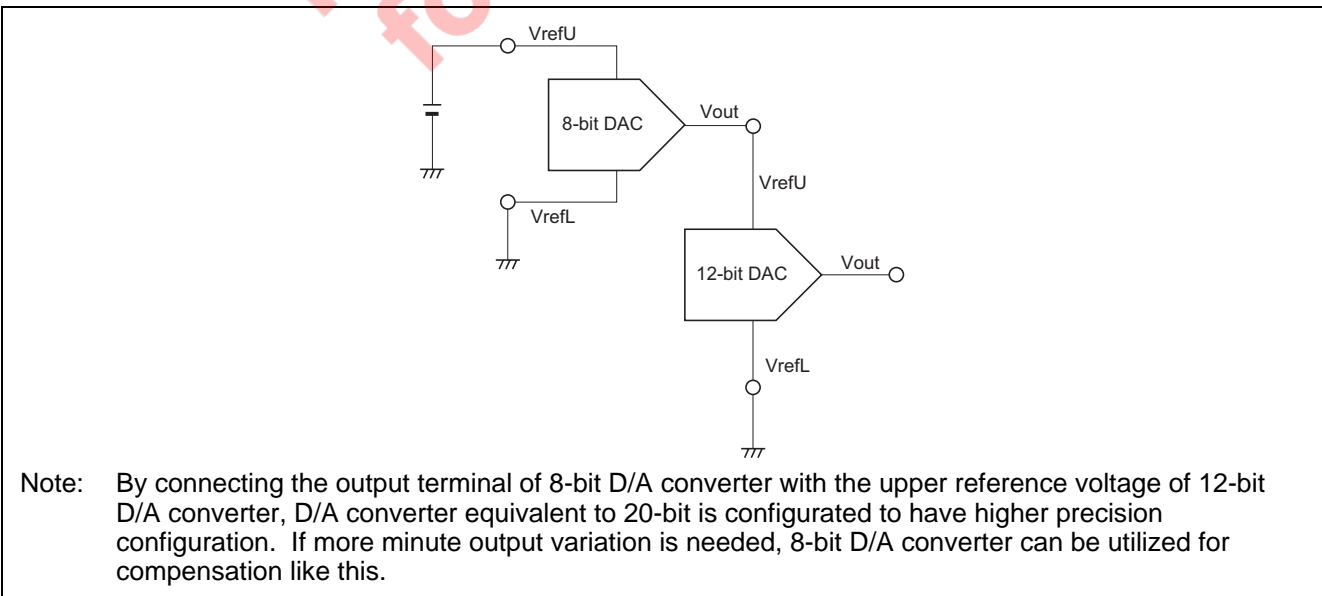
8-bit D/A

D00	D01	D02	D03	D04	D05	D06	D07	D08	D09	D10	D11	D/A Output
0	0	0	0	0	0	0	0	—	—	—	—	VrefL8
1	0	0	0	0	0	0	0	—	—	—	—	$(VrefU8 - VrefL8) / 256 \times 1$
0	1	0	0	0	0	0	0	—	—	—	—	$(VrefU8 - VrefL8) / 256 \times 2$
1	1	0	0	0	0	0	0	—	—	—	—	$(VrefU8 - VrefL8) / 256 \times 3$
:	:	:	:	:	:	:	:	:	:	:	:	:
0	0	1	1	1	1	1	1	—	—	—	—	$(VrefU8 - VrefL8) / 256 \times 252$
1	0	1	1	1	1	1	1	—	—	—	—	$(VrefU8 - VrefL8) / 256 \times 253$
0	1	1	1	1	1	1	1	—	—	—	—	$(VrefU8 - VrefL8) / 256 \times 254$
1	1	1	1	1	1	1	1	—	—	—	—	$(VrefU8 - VrefL8) / 256 \times 255$

8-bit D/A Converter for Reference Voltage Power Supply

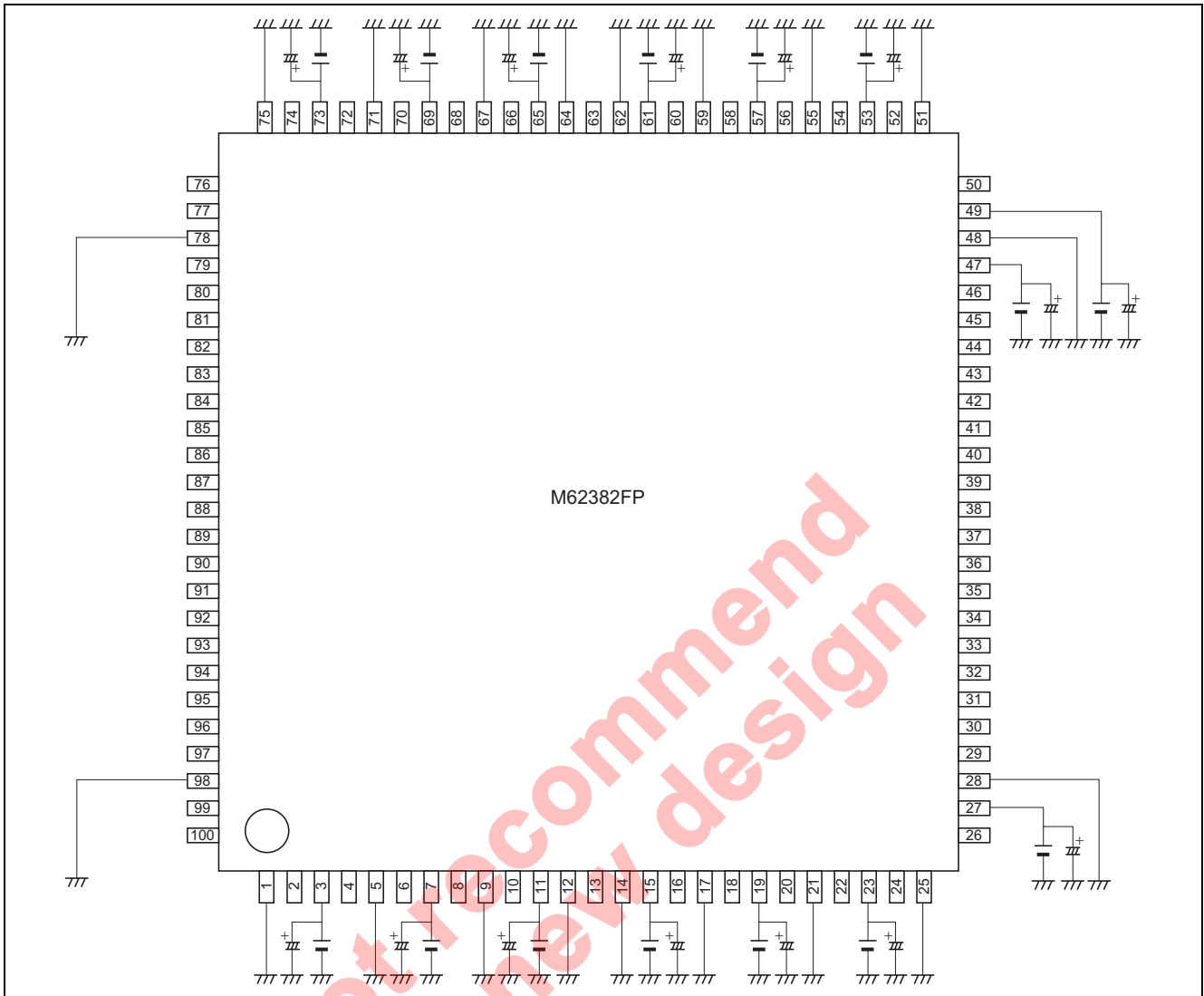


Ultra High Precision D/A Converter





Application Circuit



**Caution**

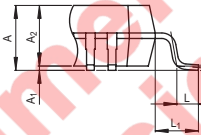
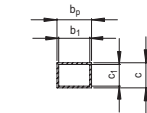
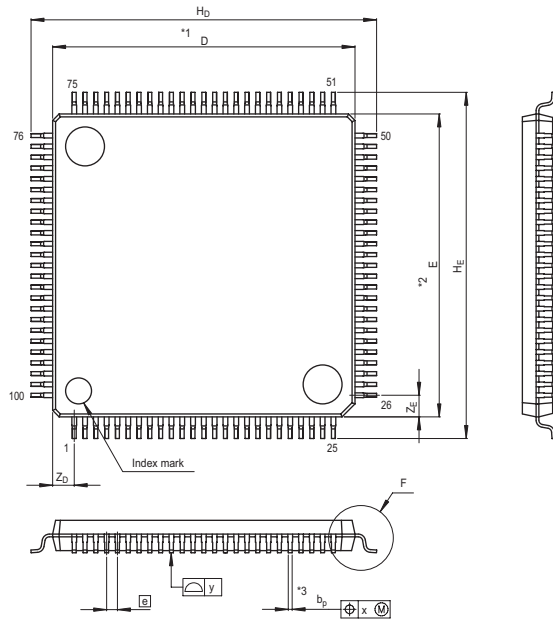
This IC has four different kinds of terminals, which are to be applied by constant voltage when used. ( $V_{CC}$ ,  $V_{DD}$ ,  $V_{refU}$ ,  $V_{refL}$ )

D/A converter precision may be worsened when ripple voltage or spike is duplicated on these four terminals.

So please be sure to put capacitor between each terminal and GND for stabilized D/A converter operation.

### Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP100-14x14-0.50	PLQP0100KB-A	100P6Q-A / FP-100U / FP-100UV	0.6g



NOTE)  
 1. DIMENSIONS \*\*1" AND \*\*2"  
 DO NOT INCLUDE MOLD FLASH.  
 2. DIMENSION \*\*3" DOES NOT  
 INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A <sub>2</sub>	—	1.4	—
H <sub>D</sub>	15.8	16.0	16.2
H <sub>E</sub>	15.8	16.0	16.2
A	—	—	1.7
A <sub>1</sub>	0.05	0.1	0.15
b <sub>p</sub>	0.15	0.20	0.25
b <sub>1</sub>	—	0.18	—
c	0.09	0.145	0.20
c <sub>1</sub>	—	0.125	—
θ	0°	—	8°
Ⓜ	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z <sub>D</sub>	—	1.0	—
Z <sub>E</sub>	—	1.0	—
L	0.35	0.5	0.65
L <sub>1</sub>	—	1.0	—

Not recommended for new design

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