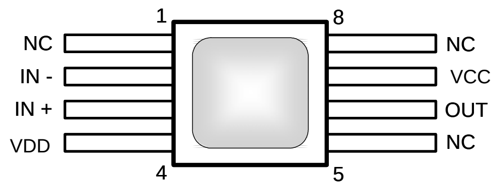
RHF43B

RAD-hardened precision bipolar single operational amplifier

Features

- High immunity to radiations, 300kRad TID; SEL immune at 68MeV/cm²/mg LET ions.
- Rail-to-rail input/output
- 8MHz gain bandwidth at 16V
- Stable for gain ≥ 5
- Low input offset voltage: 100µV typ
- Supply current: 2.2mA typ
- Operating from 3V to 16V
- Input bias current: 30nA typ
- ESD internal protection ≥ 2kV
- Latch-up immunity: 200mA
- Soon RHA QML-V qualified with smd n° 5962-062xx

Ceramic Flat-8



Description

The RHF43B is a precision bipolar operational amplifier available in hermetic 8-pin flat package and in die form. In addition to its low offset voltage, rail-to-rail feature, wide supply voltage, the RHF43B is designed for increased tolerance to radiation. Its intrinsic ELDRS-free rad-hard design allows this product to be used in space environment and in applications operating in harsh environments.

Applications

- Space probes and satellites
- Defense systems
- Scientific instrumentation
- Nuclear systems

1 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings (AMR)

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage(1)	18 ±9	V
V_{id}	Differential input voltage (2)	±1.2	V
V_{in}	Input voltage range(3)	V_{DD}-0.3 to 16	V
I_{IN}	Input current	45	mA
T_{stg}	Storage temperature	-65 to +150	°C
R_{thja}	Thermal resistance junction to ambient(4)(5)	125	°C/W
R_{thjc}	Thermal resistance junction to case(4)(5)	80	°C/W
T_j	Maximum junction temperature	150	°C
ESD	HBM: human body model(6)	2	kV
	Latch-up immunity	200	mA
	Lead temperature (soldering, 10 sec)	260	°C
Radiation related parameters			
	Low dose rate of 0.01 rad.sec^{-1}	300	kRad
	High dose rate of 50-300 rad.sec^{-1}	300	kRad
	Heavy ion latch-up (SEL) immune with heavy ions characterized by:	68	MeV.cm^{-2}.mg
	Neutron immunity	2^{+14}	n.cm^{-2}

1. All values, except differential voltage are with respect to network terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of input and output terminal must never exceed V_{CC}+0.3V.
4. Short-circuits can cause excessive heating and destructive dissipation.
5. R_{th} are typical values.
6. Human body model: 100pF discharged through a 1.5kΩ resistor between two pins of the device, done for all couples of pin combinations with other pins floating.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	3 to 16	V
V_{icm}	Common mode input voltage range	V_{DD} to V_{CC}	V
T_{oper}	Operating free air temperature range	-55 to +125	°C

2 Electrical characteristics

Table 3. V_{CC} = +16V, V_{DD} = 0V, V_{icm} = V_{CC}/2, T_{amb} = 25°C, R_L connected to V_{CC}/2 (unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Offset voltage	T= 25°C		100	300	µV
		$T_{min} < T_{op} < T_{max}$			500	
DV_{io}	Input offset voltage drift			1		µV/°C
I_{ib}	Input bias current	$V_{icm} = V_{CC}/2$, T = 25°C $T_{min} < T_{op} < T_{max}$		30	60 100	nA
DI_{ib}	Input offset current temperature drift			100		pA/°C
I_{io}	Input offset current ($V_{out} = V_{CC}/2$)	$V_{icm} = V_{CC}/2$, T = 25°C $T_{min} < T_{op} < T_{max}$		1	15 35	nA
CMR	Common mode rejection ratio	$0 < V_{icm} < 16V$ $T_{min} < T_{op} < T_{max}$	72 72	110		dB
SVR	Supply rejection ratio	$3V < V_{CC} < 16V$, $V_{icm} = V_{CC}/2$ $T_{min} < T_{op} < T_{max}$	90 80	120		dB
A_{VD}	Large signal voltage gain	$R_L = 10k\Omega$, V_{out}= 0.5V to 15.5V $T_{min} < T_{op} < T_{max}$	74 60	85		dB
V_{OH}	High level output voltage	$R_L = 1k\Omega$ connected to $V_{CC}/2$ $T_{min} < T_{op} < T_{max}$	15.7 15.6	15.8		V
		$R_L = 10k\Omega$ connected to $V_{CC}/2$ $T_{min} < T_{op} < T_{max}$	15.9 15.8	15.96		V
V_{OL}	Low level output voltage	$R_L = 1k\Omega$ connected to $V_{CC}/2$ $T_{min.} < T_{op} < T_{max.}$		0.1	0.2 0.3	V
		$R_L = 10k\Omega$ connected to $V_{CC}/2$ $T_{min} < T_{op} < T_{max}$		0.04	0.06 0.1	V
I_{out}	Output sink current	$V_{out} = V_{CC}$ $T_{min} < T_{op} < T_{max}$	20 15	30		mA
	Output source current	$V_{out} = V_{DD}$ $T_{min} < T_{op} < T_{max}$	15 10	25		
I_{CC}	Supply current	No load $T_{min} < T_{op} < T_{max}$		2.5	2.9	mA
AC performance						
GBP	Gain bandwidth product	$R_L = 1k\Omega$, C_L= 100pF, f= 100kHz $T_{min} < T_{op} < T_{max}$	6 3.5	8		MHz
F_u	Unity gain frequency	$R_L = 1k\Omega$, C_L= 100pF		5		MHz
ϕm	Phase margin	$R_L = 1k\Omega$, C_L = 100pF, G=5		50		Degrees

Table 3. V_{CC} = +16V, V_{DD} = 0V, V_{icm} = V_{CC}/2, T_{amb} = 25°C, R_L connected to V_{CC}/2 (unless otherwise specified) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
SR	Slew rate	R_L = 1kΩ, C_L = 100pF $T_{min} < T_{op} < T_{max}$	2 1.7	3		V/μs
e_n	Equivalent input noise voltage	f = 1kHz		8		$\frac{nV}{\sqrt{Hz}}$
THD+e_n	Total harmonic distortion	V_{out} = (V_{CC}-1V)/5, G= -5.1, V_{icm}=V_{CC}/2		0.01		%

Table 4. V_{CC} = +3V, V_{DD} = 0V, V_{icm} = V_{CC}/2, T_{amb} = 25°C, R_L connected to V_{CC}/2 (unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Offset voltage	T=25°C		100	300	µV
		T_{min} < T_{op} < T_{max}			500	
DV_{io}	Input offset voltage drift			1		µV/°C
I_{ib}	Input bias current	V_{CC}= 4V, V_{icm}= V_{CC}/2, T= 25°C T_{min} < T_{op} < T_{max}		30	60 100	nA
DI_{ib}	Input offset current temperature drift	V_{CC} = 4V, V_{icm} = V_{CC}/2		100		pA/°C
I_{io}	Input offset current (V_{out} = V_{cc}/2)	V_{CC} = 4V, V_{icm} = V_{CC}/2, T= 25°C T_{min} < T_{op} < T_{max}		1	15 35	nA
CMR	Common mode rejection ratio	0 < V_{icm} < 3V T_{min} < T_{op} < T_{max}	72 72	90		dB
A_{VD}	Large signal voltage gain	R_L = 10kΩ, V_{out}= 0.5V to 2.5V T_{min} < T_{op} < T_{max}	74 60	85		dB
V_{OH}	High level output voltage	R_L = 1kΩ connected to V_{CC}/2 T_{min} < T_{op} < T_{max}	2.9 2.8	2.95		V
		R_L = 10kΩ connected to V_{CC}/2 T_{min} < T_{op} < T_{max}	2.94 2.9	2.98		V
V_{OL}	Low level output voltage	R_L = 1kΩ connected to V_{CC}/2 T_{min} < T_{op} < T_{max}		0.05	0.1 0.2	V
		R_L = 10kΩ connected to V_{CC}/2 T_{min} < T_{op} < T_{max}		0.02	0.06 0.1	V
I_{out}	Output sink current	V_{out} = V_{CC} T_{min} < T_{op} < T_{max}	20 15	30		mA
	Output source current	V_{out} = V_{DD} T_{min} < T_{op} < T_{max}	15 10	25		
I_{CC}	Supply current per amplifier	No load T_{min} < T_{op} < T_{max}		2.2	 2.6	mA
AC performance						
GBP	Gain bandwidth product	R_L= 1kΩ, C_L= 100pF, f = 100kHz T_{min} < T_{op} < T_{max}	6 3.5	7.5		MHz
F_u	Unity gain frequency	R_L = 1kΩ, C_L = 100pF		5		MHz
ϕm	Phase margin	R_L = 1kΩ, C_L = 100pF, G=5		50		Degrees
SR	Slew rate	R_L = 1kΩ, C_L = 100pF T_{min} < T_{op} < T_{max}	2 1.7	2.7		V/µs
e_n	Equivalent input noise voltage	f = 1kHz		8		$\frac{nV}{\sqrt{Hz}}$
THD+e_n	Total harmonic distortion	V_{out} = (V_{CC}-1V)/5, G= -5.1, V_{icm}=V_{CC}/2		0.01		%

Figure 1. Input offset voltage distribution at T = 25°C

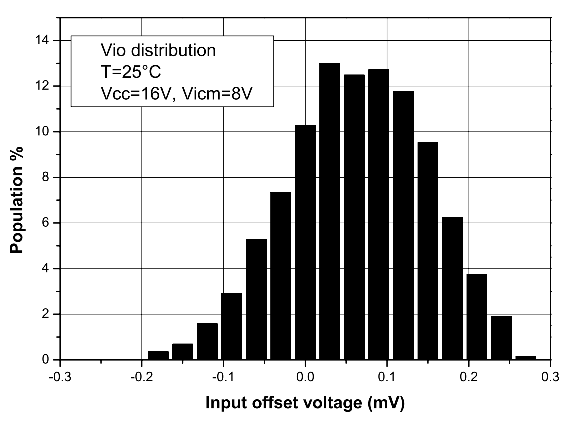


Figure 2. Input bias current vs. supply voltage

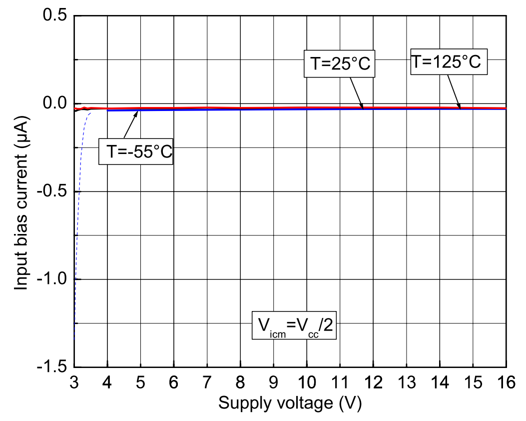


Figure 3. Input bias current vs. input common mode voltage at V_{CC}= 3V

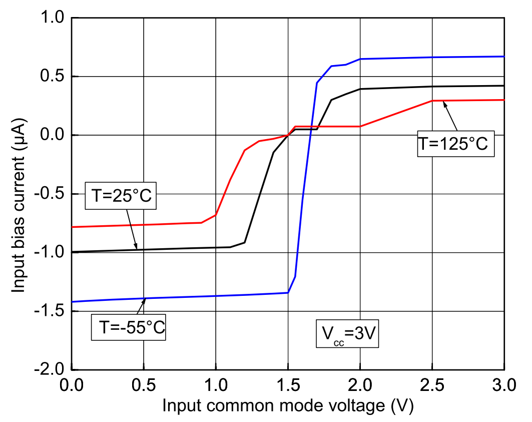


Figure 4. Supply current vs. input common mode voltage in follower configuration at V_{CC}= 3V

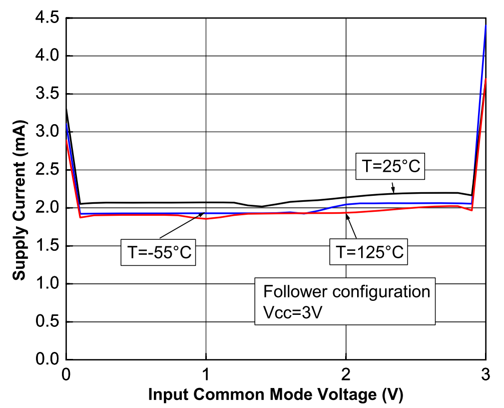


Figure 5. Supply current vs. input common mode voltage in follower configuration at V_{CC}= 16V

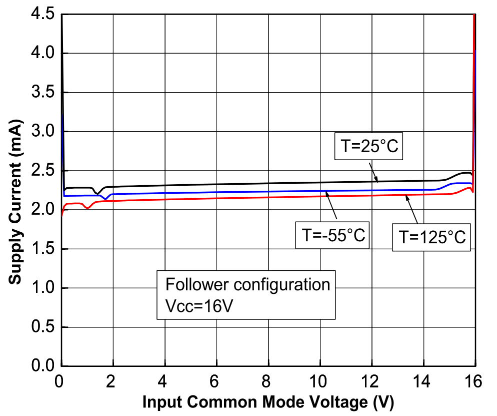


Figure 6. Supply current vs. supply voltage at V_{icm}= V_{CC}/2

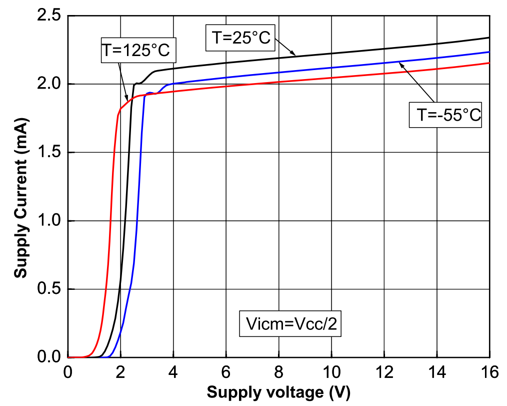


Figure 7. Output current vs.supply voltage at $V_{icm} = V_{CC}/2$

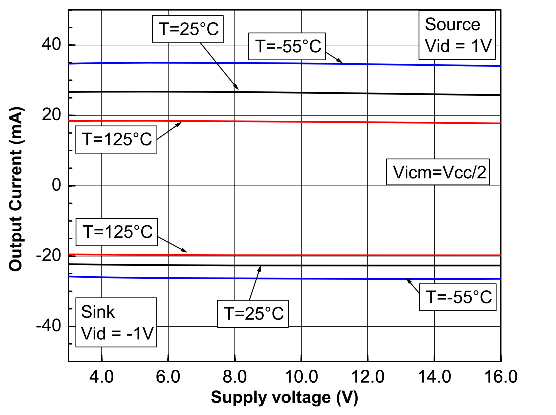


Figure 8. Output current vs. output voltage at V_{CC}= 3V

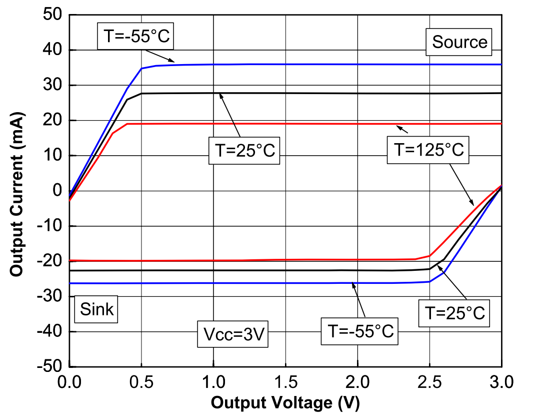


Figure 9. Output current vs. output voltage at V_{CC}= 16V

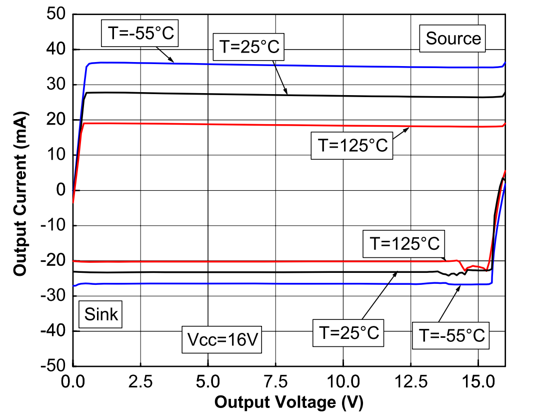


Figure 10. Differential input voltage vs. output voltage at V_{CC}= 3V

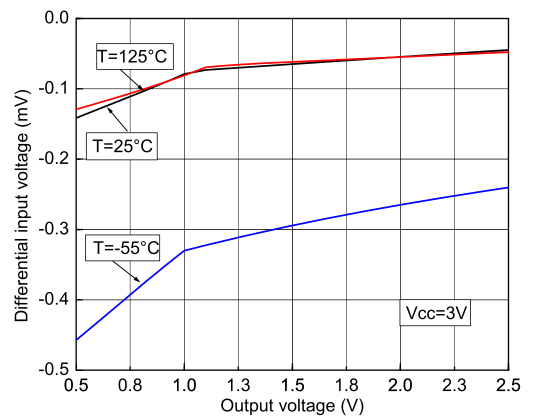


Figure 11. Differential input voltage vs. output voltage at V_{CC}= 16V

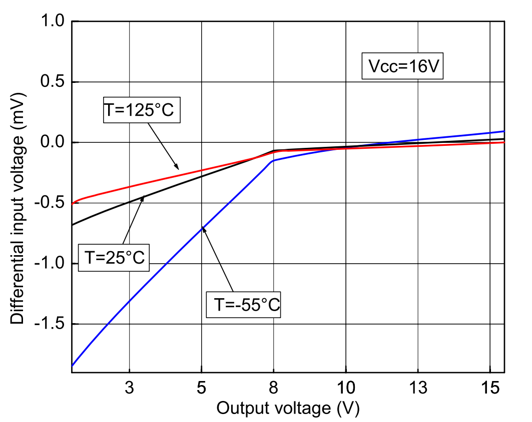


Figure 12. Noise vs. frequency at V_{CC}= 3V and V_{CC}= 16V

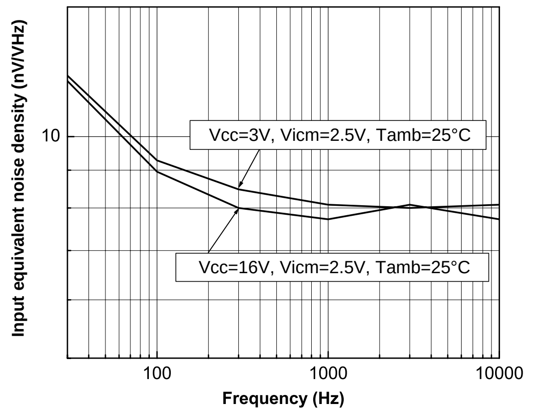


Figure 13. Voltage gain and phase vs. frequency at V_{CC}= 3V, V_{icm}= 1.5V, and T= 25°C

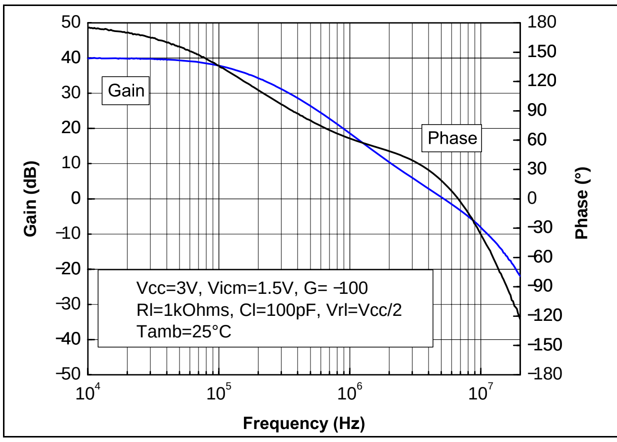


Figure 14. Voltage gain and phase vs. frequency at V_{CC}= 3V and V_{icm}= 2.5V at T= 25°C

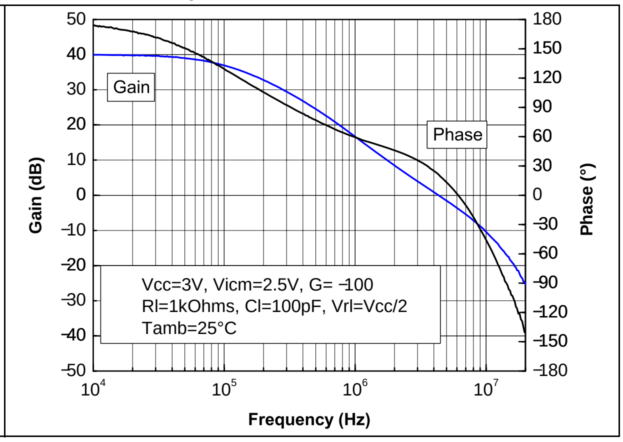


Figure 15. Voltage gain and phase vs. frequency at V_{CC}= 3V and V_{icm}= 0.5V at T= 25°C

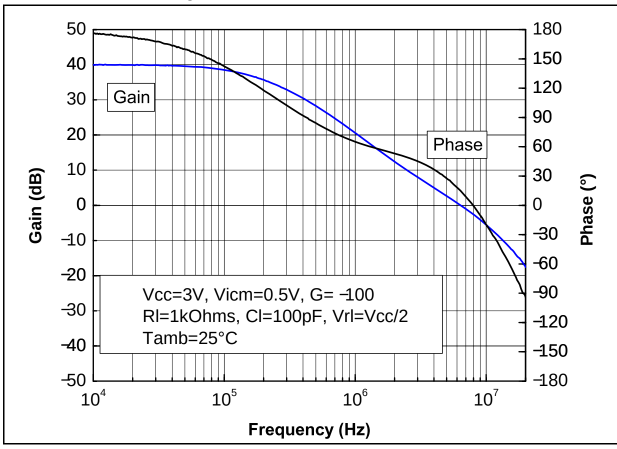


Figure 16. Voltage gain and phase vs. frequency at V_{CC}= 16V and V_{icm}= 8V at T= 25°C

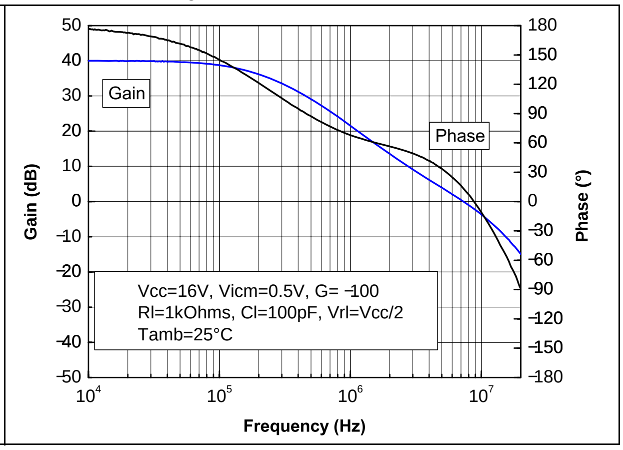


Figure 17. Voltage gain and phase vs. frequency at V_{CC}=16V and V_{icm}= 15.5V at T= 25°C

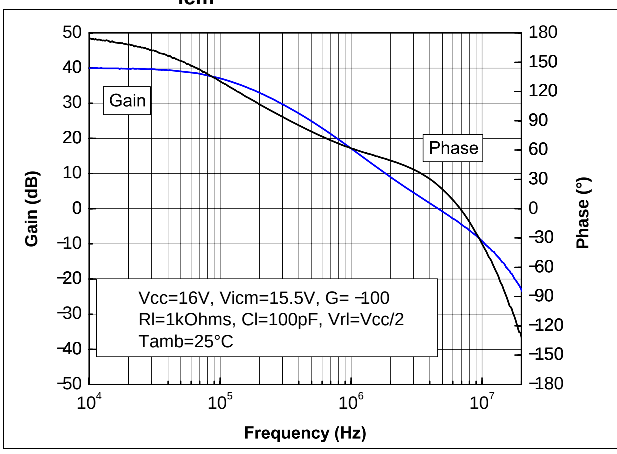


Figure 18. Voltage gain and phase vs. frequency at V_{CC}=16V and V_{icm}= 0.5V at T= 25°C

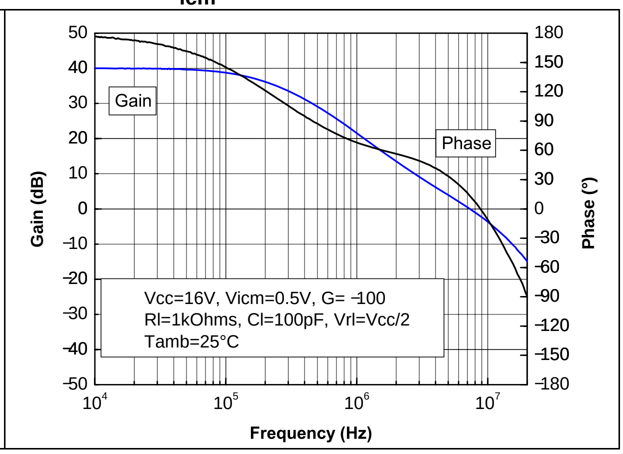


Figure 19. Inverting large signal pulse response at V_{CC}= 3V, T= 25°C

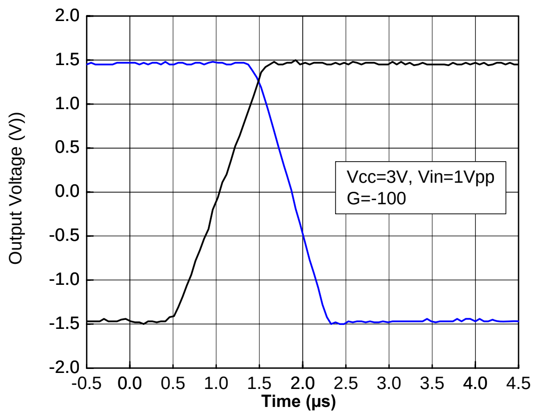
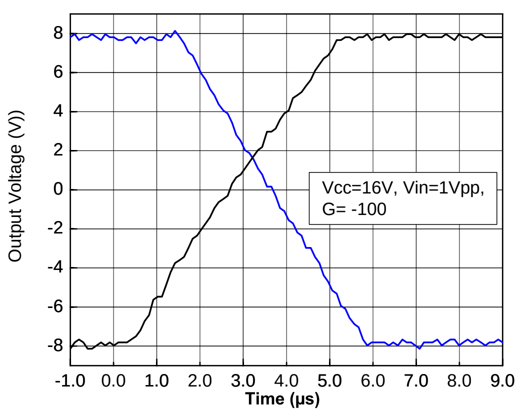
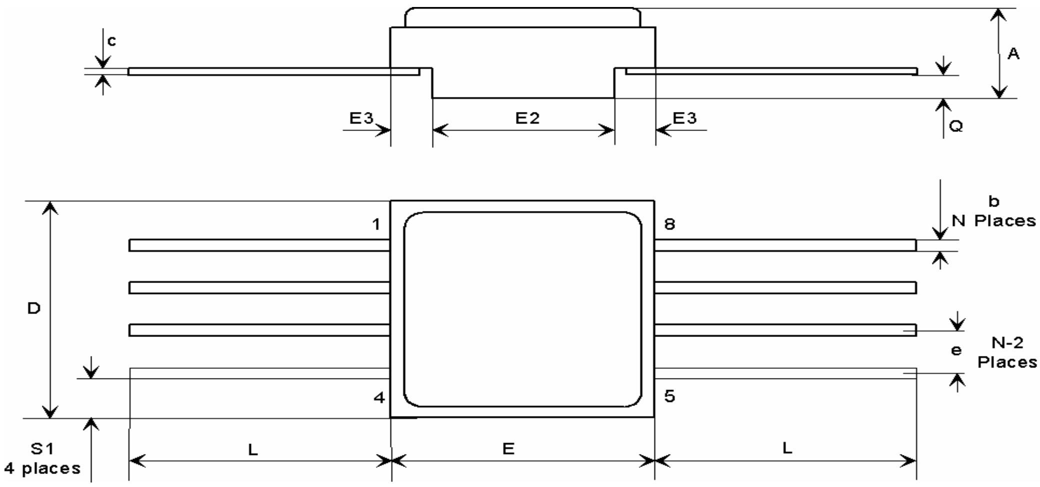


Figure 20. Inverting Large signal pulse response at V_{CC}= 16V, T= 25°C



3 Package information

Figure 21. Ceramic Flat08 package mechanical data



Symbol	Inches			Millimeters		
	Min	Nom	Max	Min	Nom	Max
A	.088	.096	.104	2.24	2.44	2.64
b	.015	.017	.019	0.38	0.43	0.48
c	.004	.005	.006	0.10	0.13	0.16
D	.250	.255	.260	6.35	6.48	6.61
E	.250	.255	.260	6.35	6.48	6.61
E2	.170	.175	.180	4.32	4.45	4.58
E3	.035	.040	.045	0.88	1.01	1.14
e		.050			1.27	
L	.335	-	.378	8.5	-	9.6
Q	.026	.031	.036	0.66	0.79	0.92
S1	.036	.044	.052	0.92	1.12	1.32
N		08			08	

4 Ordering information

Table 5. Order codes

Order code	Description	Temperature range	Package	Packing	Marking
RHF43BK-01V	Flight parts	-55°C, +125°C	Flat08	Individual cavity anti-static material trays	Marked against QML SMD
RHF43BK1	Engineering samples	-55°C, +125°C	Flat08	Individual cavity anti-static material trays	RHF43BK1
RHF43BK2	Engineering samples with 48h burn-in	-55°C, +125°C	Flat08	Individual cavity anti-static material trays	RHF43BK2
43BDIE2V	QMLV	-55°C, +125°C	Naked die	Waffle-pack	No die marking

5 Revision history

Table 6. Document revision history

Date	Revision	Changes
21-May-2007	1	First public release.
10-Dec-2007	2	Changed name of pins on pinout diagram on cover page. Modified supply current values over temperature range in electrical characteristics. Power dissipation removed from AMR table.
29-Jan-2008	3	Added ELRS-free rad-hard design in description on cover page. Modified description of heavy ion latch-up (SEL) immunity parameter in *Table 1 on page 2*.