HD74LS166A

8-bit Shift Register

REJ03D0450-0400
Rev.4.00
May 10, 2006

The inputs are buffered to lower the drive requirements to one series 74 or 74LS standard load, respectively. Input clamping diodes minimize switching transients and simplify system design. This parallel in or serial-in, serial-out shift register has a complexity of 77 equivalent gates on a monolithic chip. This device features gated clock inputs and an overriding clear input.

The parallel-in or serial-in modes are established by the shift / load input.

When high, this input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse. When low, the parallel (broadside) data inputs are enabled and synchronous loading occurs on the next clock pulse, during parallel loading, serial data flow is inhibited.

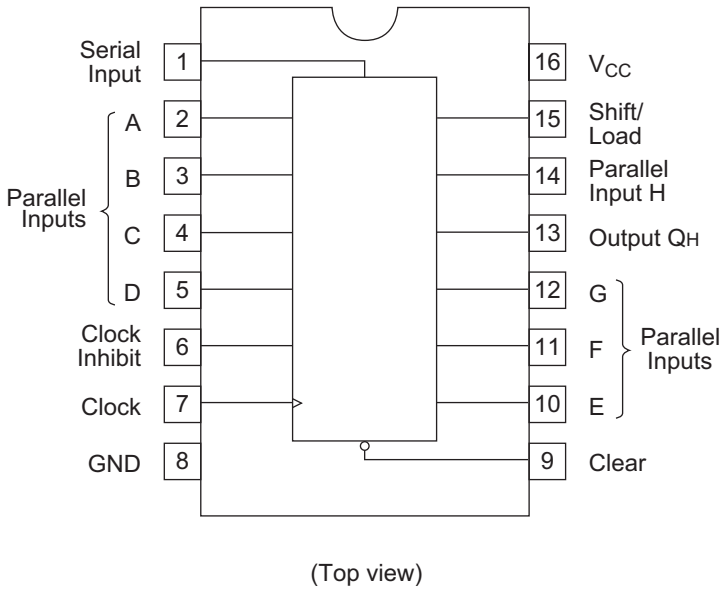
This, of course, allows the system clock to be free running and the register can be stopped on command with the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. A buffered, direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero.

Features

- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LS166AP	DILP-16 pin	PRDP0016AE-B (DP-16FV)	P	—

Pin Arrangement



(Top view)

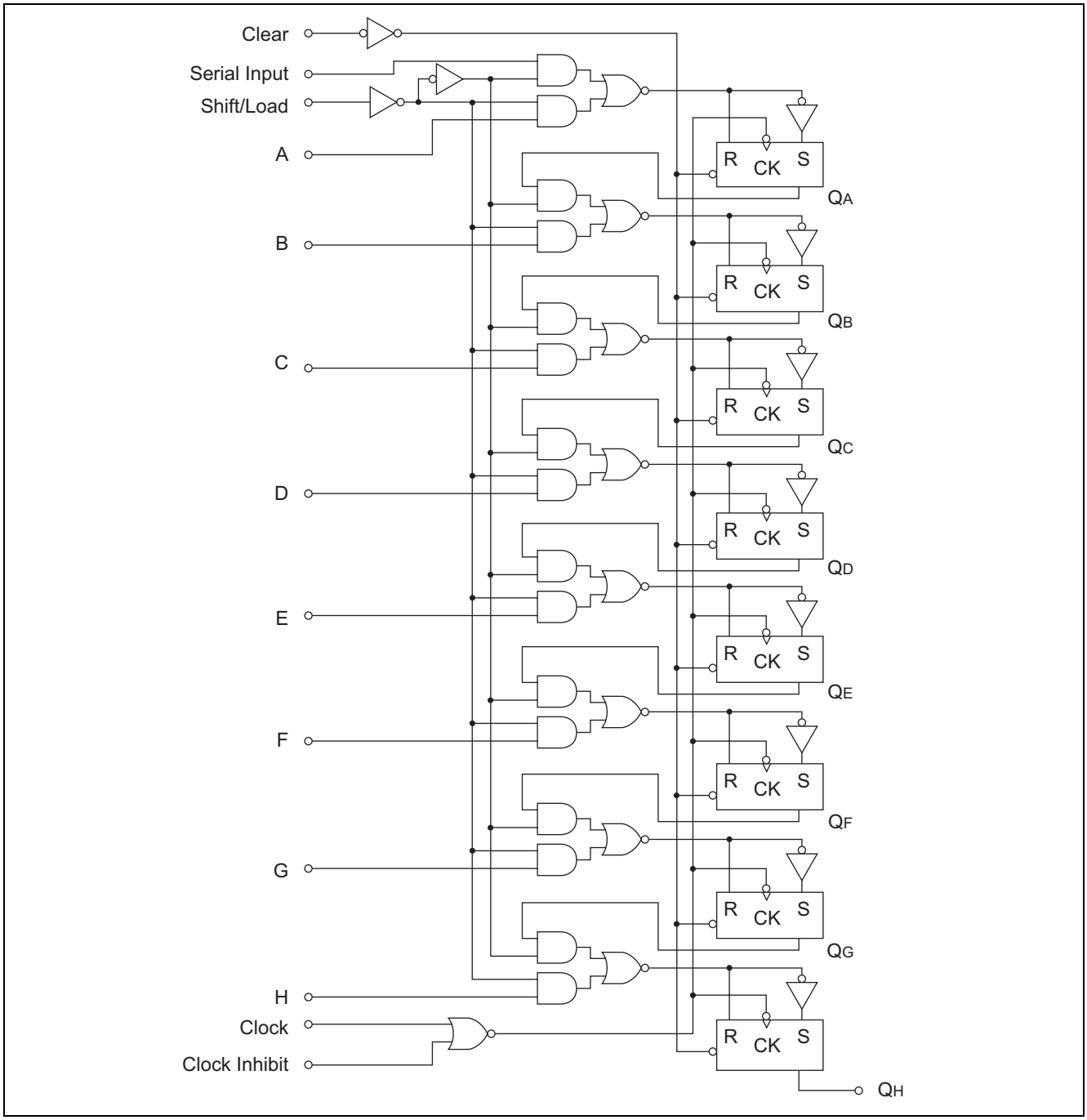
Function Table

Inputs						Internal outputs		Output Q_H
Clear	Shift Load	Clock Inhibit	Clock	Serial	Parallel A…H	Q_A	Q_B	
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	L	↑	X	a…h	a	b	h
H	H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	X	H	↑	X	X	Q_{A0}	Q_{B0}	Q_{H0}

Notes: 1. H; high level, L; low level, X; irrelevant

2. ↑; transition from low to high level
3. a to h; the level of steady-state input at inputs A to H respectively
4. Q_{A0} to Q_{H0}; the level of Q_A to Q_H, respectively, before the indicated steady-state input conditions were established.
5. Q_{An} to Q_{Gn}; the level of Q_A to Q_G, respectively, before the most recent ↑ transition of the clock.

Block Diagram



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	7	V
Input voltage	V_{IN}	7	V
Power dissipation	P_T	400	mW
Storage temperature	Tstg	–65 to +150	°C

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}	—	—	–400	µA
	I_{OL}	—	—	8	mA
Operating temperature	T_{opr}	–20	25	75	°C
Clock frequency	f_{clock}	0	—	25	MHz
Clock and clear pulse width	t_w	20	—	—	ns
Mode control setup time	t_{su}	30	—	—	ns
Data setup time	t_{su}	20	—	—	ns
Hold time	t_h	0	—	—	ns

Electrical Characteristics

(Ta = –20 to +75 °C)

Item	Symbol	min.	typ.*	max.	Unit	Condition
Input voltage	V_{IH}	2.0	—	—	V	
	V_{IL}	—	—	0.8	V	
Output voltage	V_{OH}	2.7	—	—	V	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = –400 µA
	V_{OL}	—	—	0.4	V	I_{OL} = 4 mA; V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V
		—	—	0.5		I_{OL} = 8 mA
Input current	I_{IH}	—	—	20	µA	V_{CC} = 5.25 V, V_I = 2.7 V
	I_{IL}	—	—	–0.4	mA	V_{CC} = 5.25 V, V_I = 0.4 V
	I_I	—	—	0.1	mA	V_{CC} = 5.25 V, V_I = 7 V
Short-circuit output current	I_{OS}	–20	—	–100	mA	V_{CC} = 5.25 V
Supply current**	I_{CC}	—	20	32	mA	V_{CC} = 5.25 V
Input clamp voltage	V_{IK}	—	—	–1.5	V	V_{CC} = 4.75 V, I_{IN} = –18 mA

Notes: * V_{CC} = 5 V, Ta = 25°C

** With the outputs open, 4.5 V applied to the serial input and all other inputs except the clock grounded, I_{CC} is measured after a momentary ground, then 4.5 V, is applied to clock.

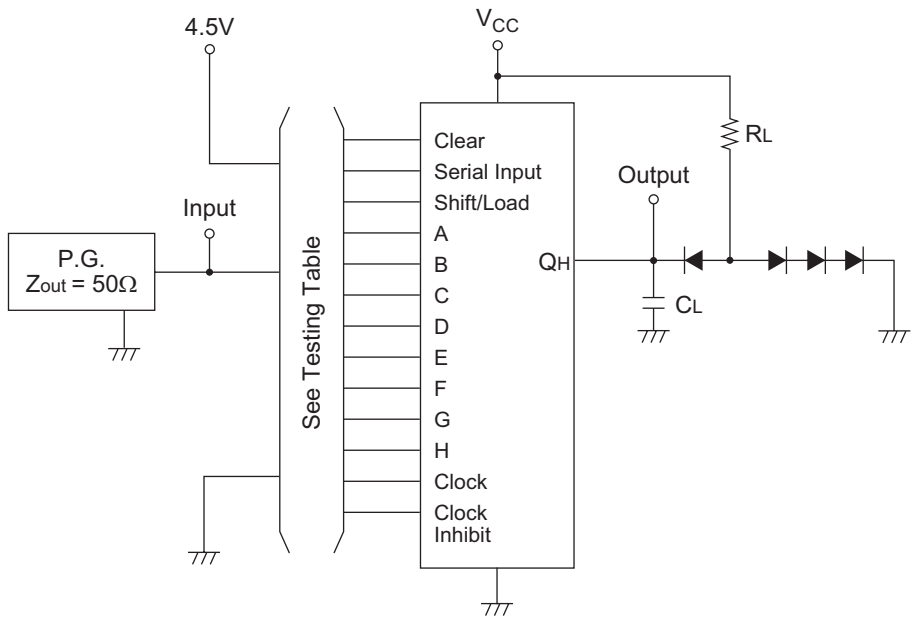
Switching Characteristics

(V_{CC} = 5 V, Ta = 25°C)

Item	Symbol	Inputs	min.	typ.	max.	Unit	Condition
Maximum clock frequency	f_{max}		25	35	—	MHz	C_L = 15 pF, R_L = 2 kΩ
Propagation delay time	t_{PHL}	Clear	—	19	30	ns	
	t_{PHL}	Clock	7	14	25	ns	
	t_{PLH}		5	11	20	ns	

Testing Method

Test Circuit

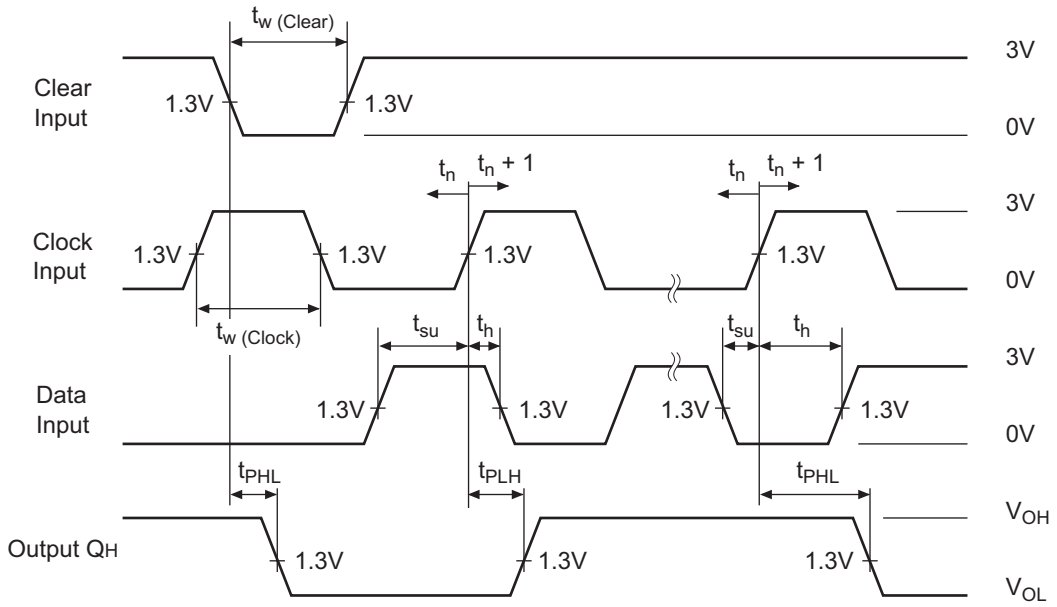


Notes: 1. C_L includes probe and jig capacitance.
2. All diodes are 1S2074(H).

Testing table

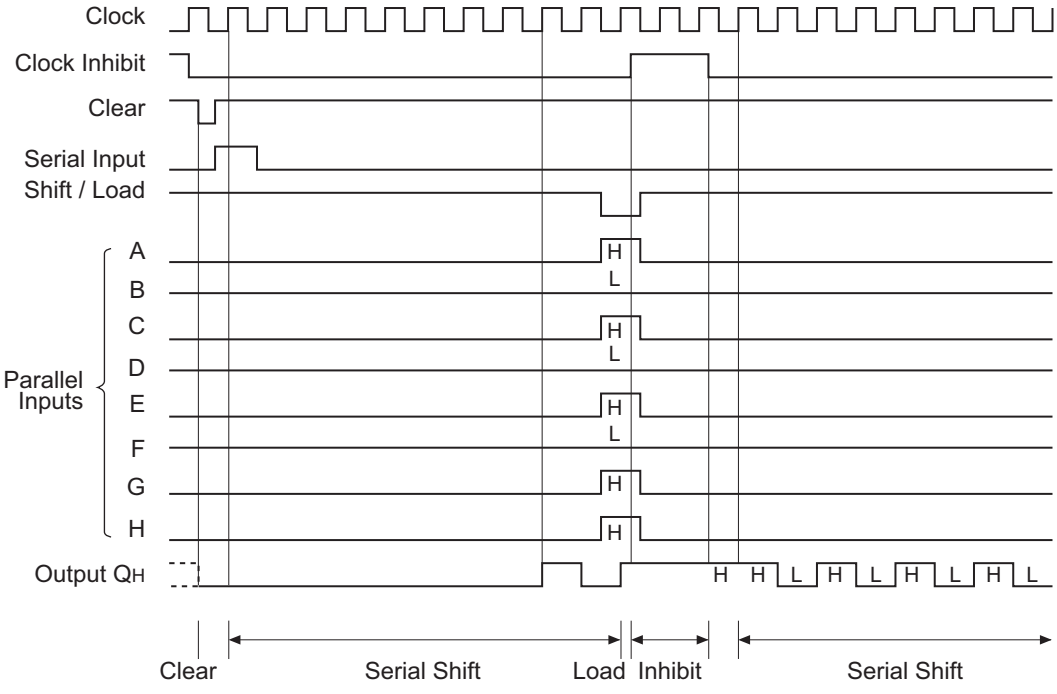
Data inputs	Shift / Load	Output	Bit time
Data H	0 V	Q_H	t_{n+1}
Serial-in	4.5 V	Q_H	t_{n+8}

Waveform



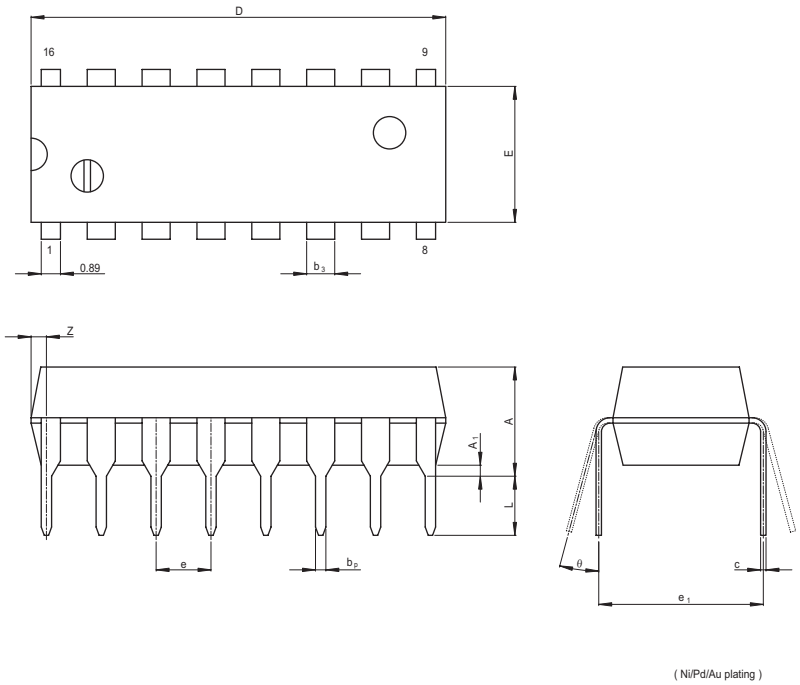
Notes:
1. Input pulse; ≤ 15 ns, t_{THL} ≤ 6 ns, PRR = 1 MHz, duty cycle 50%
   Clock input; t_w ≥ 20 ns
   Clear inpu; t_w ≥ 20 ns, t_h = 10 ns, when testing f_{max}, vary the clock PRR.
2. Propagation delay time (t_{PLH} and t_{PHL}) are measured at t_{n+1}. Proper shifting of data is verified at t_{n+8} with a functional test.
3. t_n; bit time before clocking transition.
   t_{n+1}; bit time after one clocking transition.
   t_{n+8}; bit time after eight clocking transition.

Typical Clear, Shift, Load, Inhibit, and Shift Sequences



Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-DIP16-6.3x19.2-2.54	PRDP0016AE-B	DP-16FV	1.05g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e_1	—	7.62	—
D	—	19.2	20.32
E	—	6.3	7.4
A	—	—	5.06
A_1	0.51	—	—
b_p	0.40	0.48	0.56
b_3	—	1.30	—
c	0.19	0.25	0.31
θ	0°	—	15°
e	2.29	2.54	2.79
Z	—	—	1.12
L	2.54	—	—

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