RTAX-DSP Radiation-Tolerant FPGAs

Radiation Performance

- SEU-Hardened Registers Eliminate the Need for Triple-Module Redundancy (TMR)
  - Immune to Single-Event Upsets (SEU) to LET_{TH} > 37 MeV-cm^2/mg
  - SEU Rate < 10^{-10} Errors/Bit-Day in Worst-Case Geosynchronous Orbit
- Expected SRAM Upset Rate of <10^{-10} Errors/Bit-Day with Use of Error Detection and Correction (EDAC) IP (included) with Integrated SRAM Scrubber
  - Single-Bit Correction, Double-Bit Detection
  - Variable-Rate Background Refreshing
- Total Ionizing Dose Up to 300 krad (Si, Functional)
- Single-Event Latch-Up Immunity (SEL) to LET_{TH} > 117 MeV-cm^2/mg
- TM1019 Test Data Available

Embedded Multiply/Accumulate Blocks

- Up to 120 Multiply/Accumulate Blocks
- Fully SEU- and SET-Hardened
- 125 MHz Performance throughout Military Temperature Range
- Flexible, Cascadable Accumulate Function

Processing Flows

- B-Flow – MIL-STD-883B
- E-Flow – Actel Extended Flow
- EV-Flow – Class V Equivalent Flow Processing

Prototyping Options

- RTAX-DSP PROTO Devices with Same Functional and Timing Characteristics as Flight Unit in a Non-Hermetic Package

Leading-Edge Performance

- High-Performance Embedded FIFOs
- 350+ MHz System Performance
- 500+ MHz Internal Performance
- 700 Mbps LVDS Capable I/Os

Specifications

- Up to 4 Million Equivalent System Gates or 500 k Equivalent ASIC Gates
- Up to 16,800 SEU-Hardened Flip-Flops
- Up to 840 I/Os
- Up to 540 kbits Embedded SRAM
- Manufactured on Advanced 0.15 µm CMOS Antifuse Process Technology, 7 Layers of Metal

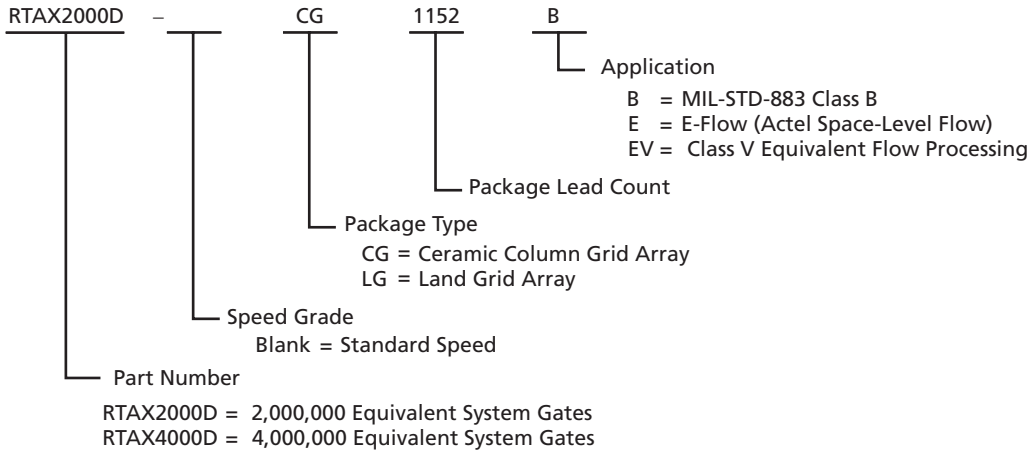
Features

- Single-Chip, Nonvolatile Solution
- 1.5 V Core Voltage for Low Power
- Flexible, Multi-Standard I/Os:
  - 1.5 V, 1.8 V, 2.5 V, 3.3 V Mixed Voltage Operation
  - Bank-Selectable I/Os – 8 Banks per Chip
  - Single-Ended I/O Standards: LVTTL, LVCMOS, 3.3 V PCI
  - JTAG Boundary Scan Testing (as per IEEE 1149.1)
  - Differential I/O Standards: LVPECL and LVDS
  - Voltage-Referenced I/O Standards: GTL+, HSTL Class 1, SSTL2 Class 1 and 2, SSTL3 Class 1 and 2
  - Hot-Swap Compliant with Cold-Sparing Support (Except PCI)
- Embedded Memory with Variable Aspect Ratio and Organizations:
  - Independent, Width-Configurable Read and Write Ports
  - Programmable Embedded FIFO Control Logic
  - ROM Emulation Capability
- Deterministic, User-Controllable Timing
- Unique In-System Diagnostic and Debug Capability

Table 1 • **RTAX-DSP Family Product Profile**

Device	RTAX2000D	RTAX4000D
Capacity		
Equivalent System Gates	2,000,000	4,000,000
ASIC Gates	250,000	500,000
Modules		
Register (R-cells)	8,960	16,800
Combinatorial (C-cells)	17,920	33,600
Flip-Flops (maximum)	17,920	33,600
Embedded Multiply / Accumulate Blocks		
DSP Mathblocks	64	120
Embedded RAM/FIFO (without EDAC)		
Core RAM Blocks	64	120
Core RAM Bits (k = 1,024)	288 k	540 k
Clocks (segmentable)		
Hardwired	4	4
Routed	4	4
I/Os		
I/O Banks	8	8
User I/Os (maximum)	684	840
I/O Registers	2,052	2,520
Package		
CCGA/LGA	1152	1272

Ordering Information



Temperature Grade Offerings

Package	RTAX2000D	RTAX4000D
CG1152/LG1152	B, E, EV	–
CG1272/LG1272	–	B, E, EV

Note: **The CCGA offerings (1152 and 1272) are offered with Six Sigma columns.*
B = MIL-STD-883 Class B
E = E-Flow (Actel Space-Level Flow)
EV = Actel "V" Equivalent Flow

Speed Grade and Temperature Grade Matrix

	Std.
B	✓
E	✓
EV	✓

Contact your local Actel representative for device availability.

Device Resources

	User I/Os (including clock buffers)	
Device	**RTAX2000D**	**RTAX4000D**
CG484/LG1152	684	–
CG896/LG1272	–	840

Note: *CCGA = Ceramic Column Grid Array, LGA = Land Grid Array*

Actel MIL-STD-883 Class B Product Flow

Table 2 • **Actel MIL-STD-883 Class B Product Flow for RTAX-DSP***

Step	Screen	Method	Requirement
1	Internal Visual	2010, Condition B	100%
2	Serialization		100%
3	Temperature Cycling	1010, Condition C, 10 cycles minimum	100%
4	Constant Acceleration	2001, Y1 Orientation Only Condition TBD	100%
5	Particle Impact Noise Detection	2020, Condition A	100%
6	Seal (Fine & Gross Leak Test)	1014	100%
7	Pre-Burn-In Electrical Parameters	In accordance with applicable Actel device specification	100%
8	Dynamic Burn-In	1015, Condition D, 160 hours at 125°C or 80 hours at 150°C minimum	100%
9	Interim (Post-Burn-In) Electrical Parameters	In accordance with applicable Actel device specification	100%
10	Percent Defective Allowable (PDA) Calculation	5%	All Lots
11	Final Electrical Test a. Static Tests (1) 25°C (2) –55°C and +125°C b. Functional Tests (1) 25°C (2) –55°C and +125°C c. Switching Tests at 25°C	In accordance with applicable Actel device specification, which includes a, b, and c: 5005, Table 1, Subgroup 1 5005, Table 1, Subgroup 2, 3 5005, Table 1, Subgroup 7 5005, Table 1, Subgroup 8a, 8b 5005, Table 1, Subgroup 9	100%
12	External Visual	2009	100%

Note: **For CCGA devices, all Assembly, Screening, and TCI testing is performed at LGA level. Only QA electrical and mechanical visual tests are performed after solder column attachment.*

Actel Extended Flow

Table 3 • **Actel Extended Flow for RTAX-DSP[1, 2, 3]**

Step	Screen	Method	Requirement
1	Destructive Bond Pull[4]	2011, Condition D	Extended Sample
2	Internal Visual	2010, Condition A	100%
3	Serialization		100%
4	Temperature Cycling	1010, Condition C, 10 cycles minimum	100%
5	Constant Acceleration	2001, Y1 Orientation Only Condition TBD	
6	Particle Impact Noise Detection	2020, Condition A	100%
7	Radiographic (X-Ray)	2012, One View (Y1 Orientation) Only	100%
8	Pre-Burn-In Electrical Parameters	In accordance with applicable Actel device specification	
9	Dynamic Burn-In	1015, Condition D, 240 hours at 125°C or 120 hours at 150°C minimum	100%
10	Interim (Post-Dynamic-Burn-In) Electrical Parameters	In accordance with applicable Actel device specification	100%
11	Static Burn-In	1015, Condition C, 72 hours at 150°C or 144 hours at 125°C minimum	100%
12	Interim (Post-Static-Burn-In) Electrical Parameters	In accordance with applicable Actel device specification	100%
13	Percent Defective Allowable (PDA) Calculation	5% Overall, 3% Functional Parameters at 25°C	All Lots
14	Final Electrical Test[4] a. Static Tests (1) 25°C (2) –55°C and +125°C b. Functional Tests (1) 25°C (2) –55°C and +125°C c. Switching Tests at 25°C	In accordance with applicable Actel device specification, which includes a, b, and c: 5005, Table 1, Subgroup 1 5005, Table 1, Subgroup 2, 3 5005, Table 1, Subgroup 7 5005, Table 1, Subgroup 8a, 8b 5005, Table 1, Subgroup 9	100%
15	Seal (Fine & Gross Leak Test)	1014	100%
16	External Visual	2009	100%

Notes:

1. *Actel offers Extended Flow for users requiring additional screening beyond MIL-STD-833, Class B requirement. Extended Flow incorporates the majority of the screening procedures as outlined in Method 5004 of MIL-STD-883, Class S.*
2. *The Quality Conformance Inspection (QCI) for Extended Flow devices still complies to the MIL-STD-833, Class B requirement.*
3. *For CCGA devices, all Assembly/Screening/TCI testing is performed at LGA level. Only QA electrical and mechanical visual tests are performed after solder column attachment.*
4. *Requirement for 100% nondestructive bond pull per Method 2003 is substituted by an extensive destructive bond pull to Method 2011 Condition D on an extended sample basis.*

Actel "EV" Flow (Class V Flow Equivalent Processing)

Table 4 • **Actel "EV" Flow (Class V Equivalent Flow Processing) for RTAX-DSP[1, 2]**

Step	Screen	Method	Requirement
1	Destructive Bond Pull[3]	2011, Condition D	Extended Sample
2	Internal Visual	2010, Condition A	100%
3	Serialization		100%
4	Temperature Cycling	1010, Condition C, 50 cycles minimum	100%
5	Constant Acceleration	2001, Y1 Orientation Only Condition TBD	100%
6	Particle Impact Noise Detection	2020, Condition A	100%
7	Radiographic (X-Ray)	2012, One View (Y1 Orientation) Only	100%
8	Pre-Burn-In Electrical Parameters	In accordance with applicable Actel device specification	100%
9	Dynamic Burn-In	1015, Condition D, 240 hours at 125°C or 120 hours at 150°C minimum	100%
10	Interim (Post-Dynamic-Burn-In) Electrical Parameters	In accordance with applicable Actel device specification	100%
11	Static Burn-In	1015, Condition C, 72 hours at 150°C or 144 hours at 125°C minimum	100%
12	Interim (Post-Static-Burn-In) Electrical Parameters	In accordance with applicable Actel device specification	100%
13	Percent Defective Allowable (PDA) Calculation	5% Overall, 3% Functional Parameters at 25°C	All Lots
14	Final Electrical Test[3, 4] a. Static Tests (1) 25°C (2) –55°C and +125°C b. Functional Tests (1) 25°C (2) –55°C and +125°C c. Switching Tests at 25°C	In accordance with applicable Actel device specification, which includes a, b, and c: 5005, Table 1, Subgroup 1 5005, Table 1, Subgroup 2, 3 5005, Table 1, Subgroup 7 5005, Table 1, Subgroup 8a, 8b 5005, Table 1, Subgroup 9	100%
15	Seal (Fine & Gross Leak Test)	1014	100%
16	External Visual	2009	100%
17	Wafer Lot Specific Life Test (Group C)	MIL-PRF-38535, Appendix B, sec. B.4.2.c	All Wafer Lots

Notes:

1. *Actel offers "EV" flow for users requiring full compliance to the MIL-PRF-38535 Class V requirement. The "EV" process flow is expanded from the existing E-flow requirement (it still meets the full SMD requirement for current E-flow devices) with the intention to be in full compliance to the MIL-PRF-38535 Table IA and Appendix B requirement, but without the official Class V certification from DSCC.*
2. *For CCGA devices, all Assembly/Screening/TCI testing is performed at LGA level. Only QA electrical and mechanical visual tests are performed after solder column attachment.*
3. *The requirement for 100% nondestructive bond pull per Method 2003 is fulfilled by substitution of an extensive extended sample basis.*
4. *Read and record performed at –55°C and +125°C (no delta calculation).*

General Description

RTAX-DSP Mathblock Functional Description

The flexible elements of the RTAX-DSP Mathblocks enable easy integration into many different signal processing topologies, such as Fast Fourier Transforms, Inverse Fast Fourier Transforms, Finite Impulse Response Filters, Infinite Impulse Response Filters, and Discrete Cosine Transforms. The hardwired Mathblocks also enable acceleration of high precision single- and double-floating point multiplications. Figure 1-1 shows a basic functional diagram of a Mathblock.

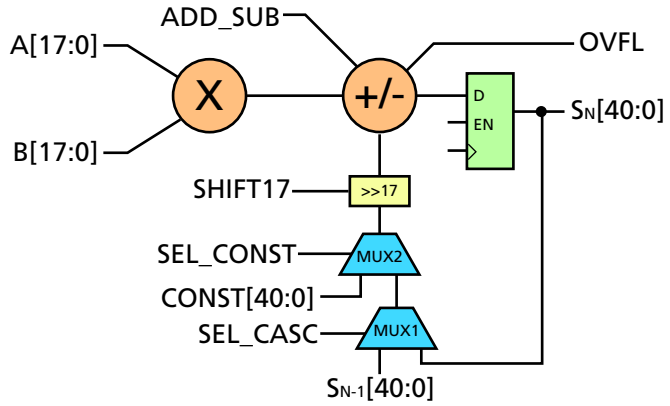


Figure 1-1 • **RTAX-DSP Mathblock**

The Mathblocks comprise the following elements:

1. Multiplier

   The multiplier operates on two signed 18-bit factors, A[17:0] and B[17:0] (Figure 1-2). The multiplier produces a signed 36-bit output, which is provided as an input to the add/subtract function. The output of the multiplier can optionally bypass the add/subtract function.

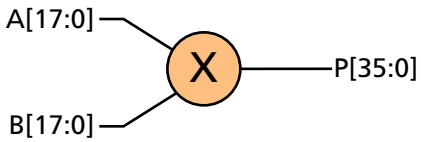


Figure 1-2 • **RTAX-DSP Mathblock Multiplier Configured as Signed 18x18**

The multiplier can be fractured to implement two instances of signed 9x9 multiplication (Figure 1-3).

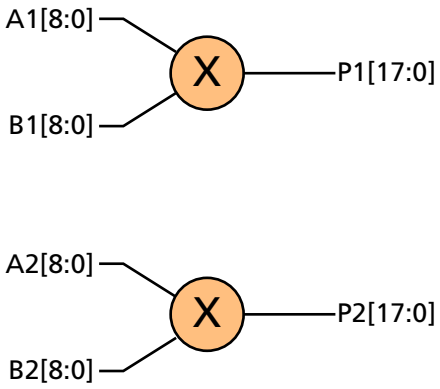


Figure 1-3 • **Mathblock Configured with Two Independent Signed 9x9 multipliers**

2. Adder/Subtractor plus MUX Control

- The adder/subtractor can perform the following functions:
  - Accumulate using feedback.
  - Create higher precision multipliers using the S_{N-1} input and the 17-bit shift function.
  - Create complex DSP functions, such as FIR filters, by cascading Mathblocks together using the S_{N-1} input.
  - The initial value of the accumulate function can be set using the value defined on the CONST bus.

Overflow or underflow of the add/subtract function is indicated by the OVFL output.

Figure 1-4 shows the Mathblock configured to perform multiply and accumulate functions. FPGA resources can be used to extend the accumulate width.

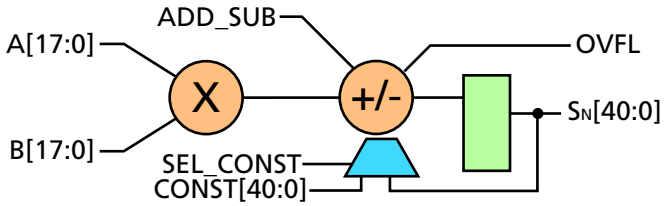


Figure 1-4 • **Mathblock Configured to Perform Multiply and Accumulate Functions**

3. Output Register

   The output of the adder/subtractor block is presented to a 41-bit output register. The register has a clock input, an enable input, a set or reset input, and provides a 41-bit output S_N[40:0] to the exterior of the Mathblock. Signals S_N[40:0] are also fed back within the Mathblock to the accumulator multiplexer stack to enable various accumulation functions.

4. Cascading Mathblocks

   Mathblocks may be cascaded together to form complex DSP structures such as FIR filters and FFTs. Figure 1-5 shows the configuration of Mathblocks cascaded together.

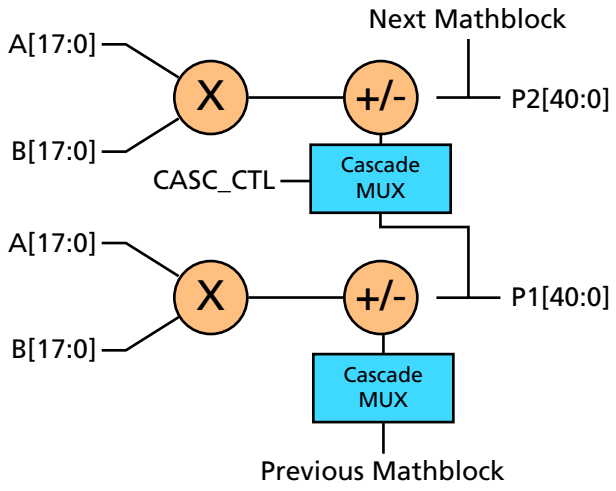


Figure 1-5 • **Mathblocks Cascaded Together as Part of a Complex DSP Function**

RTAX-DSP Architecture

The overall RTAX-DSP device architecture is shown in Figure 1-6. In each core tile, there are four Mathblocks, which are located adjacent to the SRAM/FIFO blocks. The Mathblocks are evenly distributed across the device, to help achieve uniform performance of DSP functions.

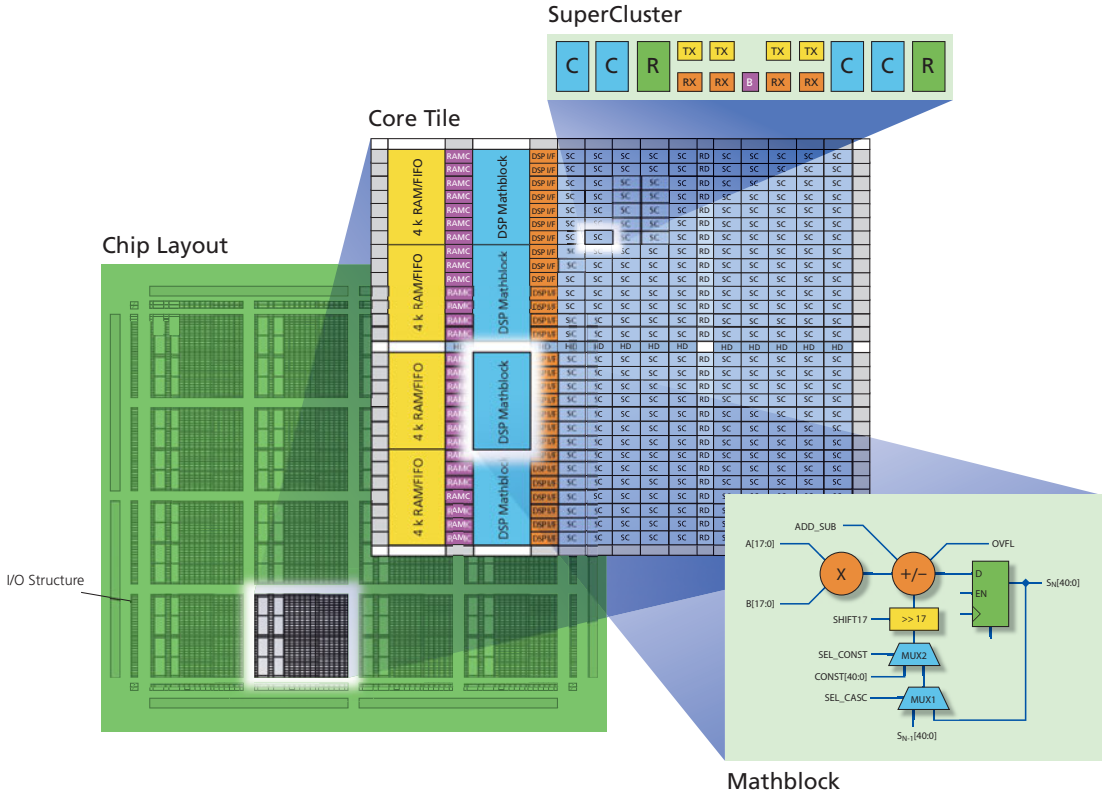


Figure 1-6 • **RTAX-DSP Device Architecture Overview**

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