

**AO4478L**
**N-Channel Enhancement Mode Field Effect Transistor**
**General Description**

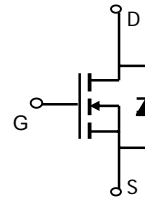
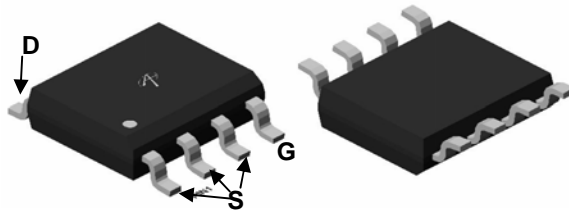
The AO4478L uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge. This device is suitable for use as general purpose, PWM and a load switch applications.

- RoHS Compliant
- Halogen Free

**Features**

$V_{DS}$  (V) = 30V  
 $I_D$  = 9A ( $V_{GS}$  = 10V)  
 $R_{DS(ON)}$  < 19m $\Omega$  ( $V_{GS}$  = 10V)  
 $R_{DS(ON)}$  < 26m $\Omega$  ( $V_{GS}$  = 4.5V)

**100% UIS Tested!**  
**100% Rg Tested!**

**SOIC-8**

**Absolute Maximum Ratings  $T_A=25^\circ\text{C}$  unless otherwise noted**

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	30	V
Gate-Source Voltage	$V_{GS}$	$\pm 25$	V
Continuous Drain Current	$I_D$	$T_A=25^\circ\text{C}$	A
		$T_A=70^\circ\text{C}$	
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	60	
Avalanche Current <sup>C</sup>	$I_{AR}$	17	
Repetitive avalanche energy $L=0.1\text{mH}^C$	$E_{AR}$	14	mJ
Power Dissipation <sup>B</sup>	$P_D$	$T_A=25^\circ\text{C}$	W
		$T_A=70^\circ\text{C}$	
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150	$^\circ\text{C}$

**Thermal Characteristics**

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	31	40	$^\circ\text{C/W}$
Maximum Junction-to-Ambient <sup>AD</sup>				
Maximum Junction-to-Lead <sup>C</sup>	$R_{\theta JL}$	16	24	$^\circ\text{C/W}$

Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V	30			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			1 5	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±25V			100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1	1.6	2	V
I <sub>D(ON)</sub>	On state drain current	V <sub>GS</sub> =10V, V <sub>DS</sub> =5V	60			A
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =9A T <sub>J</sub> =125°C		16 25	19 30	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =8A		21	26	mΩ
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =10A		24		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =1A, V <sub>GS</sub> =0V		0.70	1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current				4	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance			466	560	pF
C <sub>oss</sub>	Output Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =15V, f=1MHz		90		pF
C <sub>riss</sub>	Reverse Transfer Capacitance			61		pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz		3.7	5.6	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g</sub> (10V)	Total Gate Charge			9.3	11	nC
Q <sub>g</sub> (4.5V)	Total Gate Charge	V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, I <sub>D</sub> =9A		4.3	5.2	nC
Q <sub>gs</sub>	Gate Source Charge			1		nC
Q <sub>gd</sub>	Gate Drain Charge			2.3		nC
t <sub>D(on)</sub>	Turn-On Delay Time			5		ns
t <sub>r</sub>	Turn-On Rise Time	V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, R <sub>L</sub> =1.65Ω,		8		ns
t <sub>D(off)</sub>	Turn-Off Delay Time	R <sub>GEN</sub> =3Ω		20		ns
t <sub>f</sub>	Turn-Off Fall Time			5		ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =9A, dI/dt=500A/μs		7.5	9	ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =9A, dI/dt=500A/μs		9.8		nC

A. The value of R<sub>θJA</sub> is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C. The value in any given application depends on the user's specific board design.

B. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=150°C, using ≤ 10s junction-to-ambient thermal resistance.

C. Ratings are based on low frequency and duty cycles to keep initial T<sub>J</sub>=25°C.

D. The R<sub>θJA</sub> is the sum of the thermal impedance from junction to lead R<sub>θJL</sub> and lead to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300ns pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=150°C. The SOA curve provides a single pulse rating.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

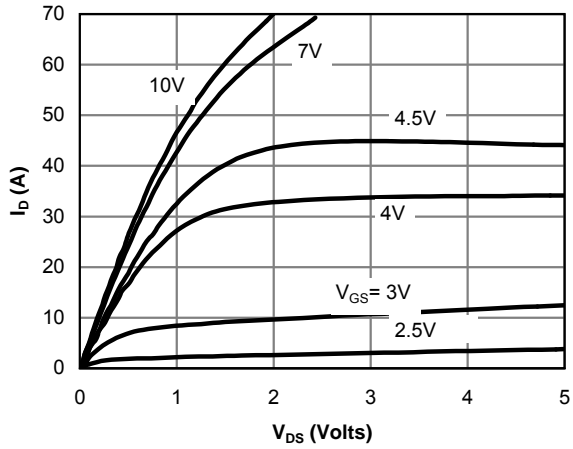


Figure 1: On-Region Characteristics(Note E)

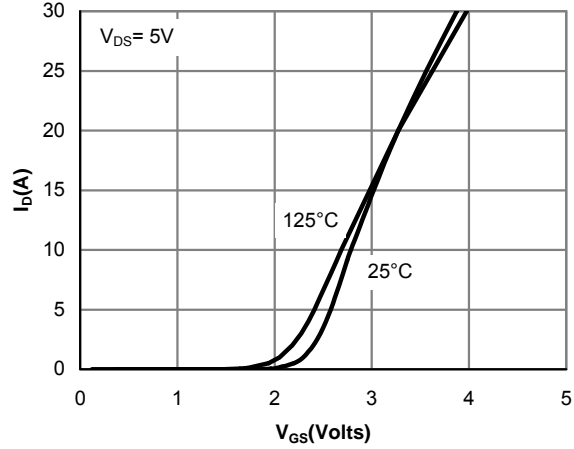


Figure 2: Transfer Characteristics(Note E)

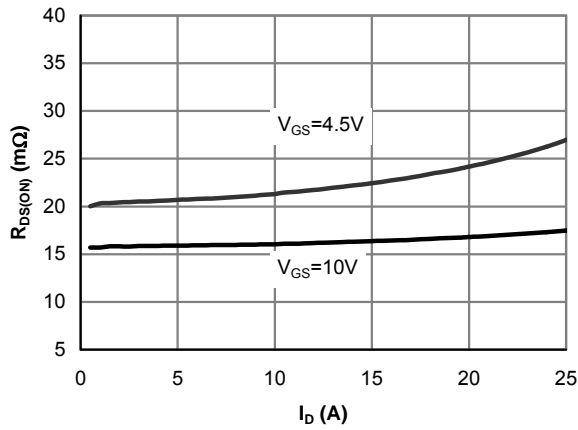


Figure 3: On-Resistance vs. Drain Current and Gate Voltage(Note E)

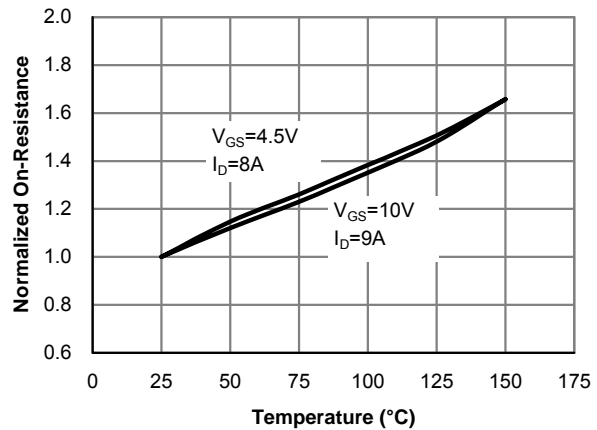


Figure 4: On-Resistance vs. Junction Temperature(Note E)

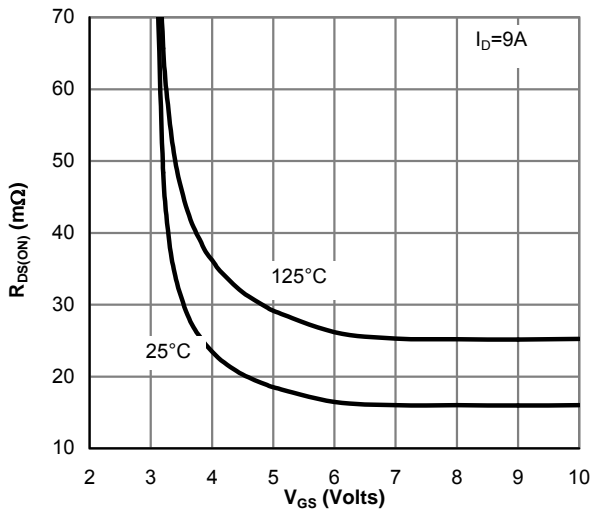


Figure 5: On-Resistance vs. Gate-Source Voltage(Note E)

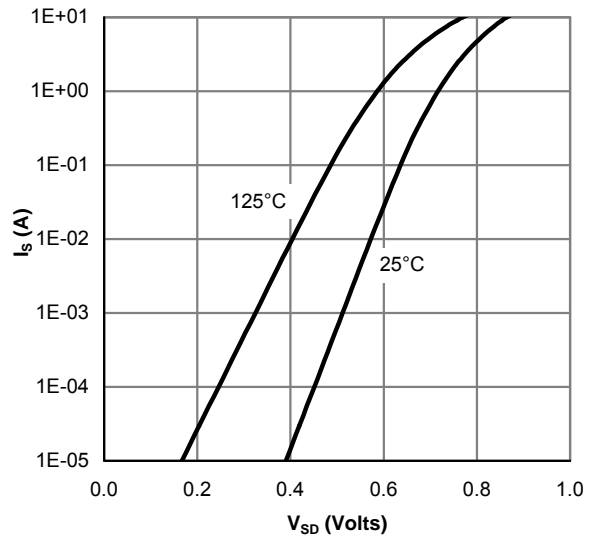


Figure 6: Body-Diode Characteristics(Note E)

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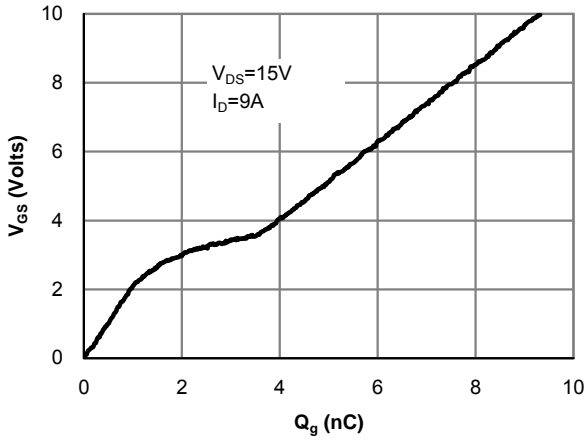


Figure 7: Gate-Charge Characteristics

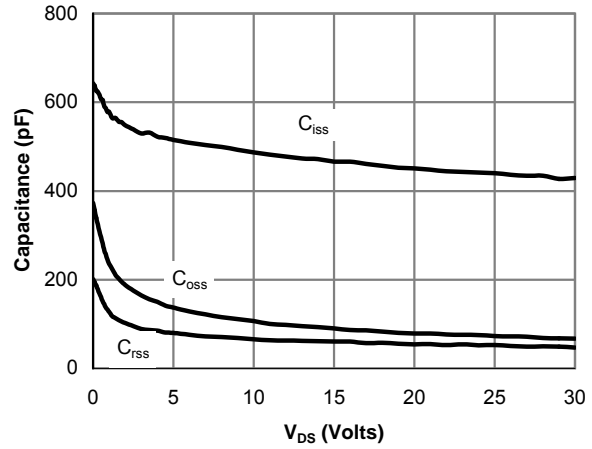


Figure 8: Capacitance Characteristics

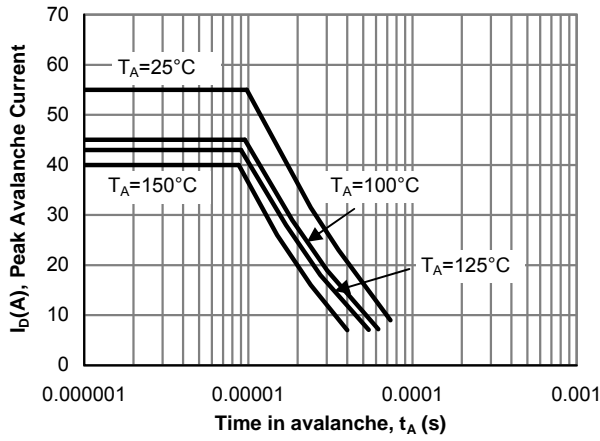


Figure 9: Single Pulse Avalanche capability (Note C)

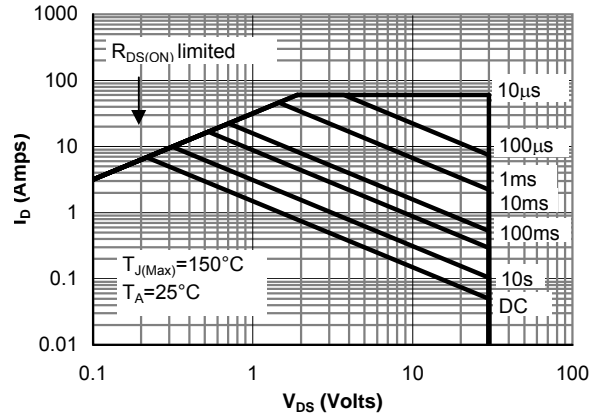


Figure 10: Maximum Forward Biased Safe Operating Area (Note F)

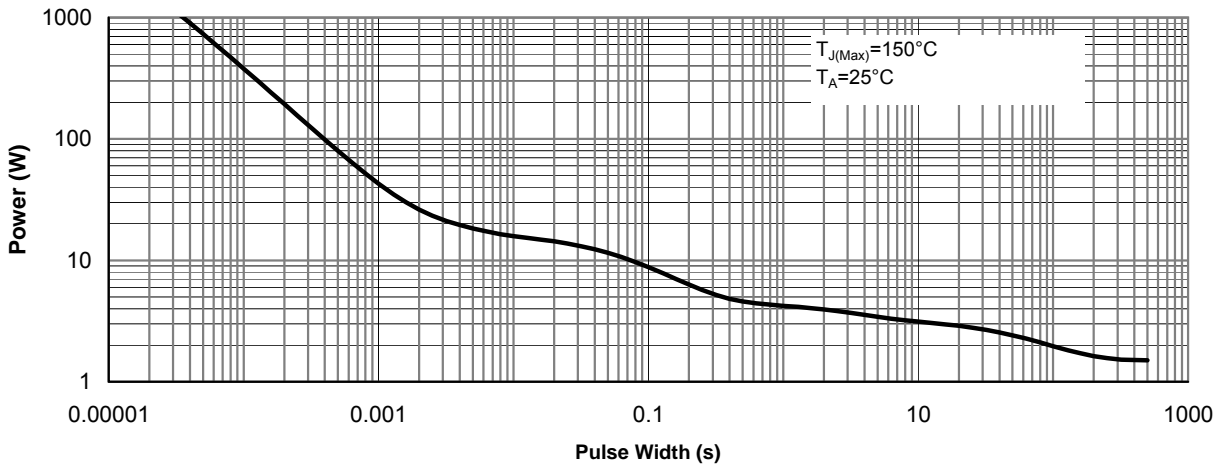
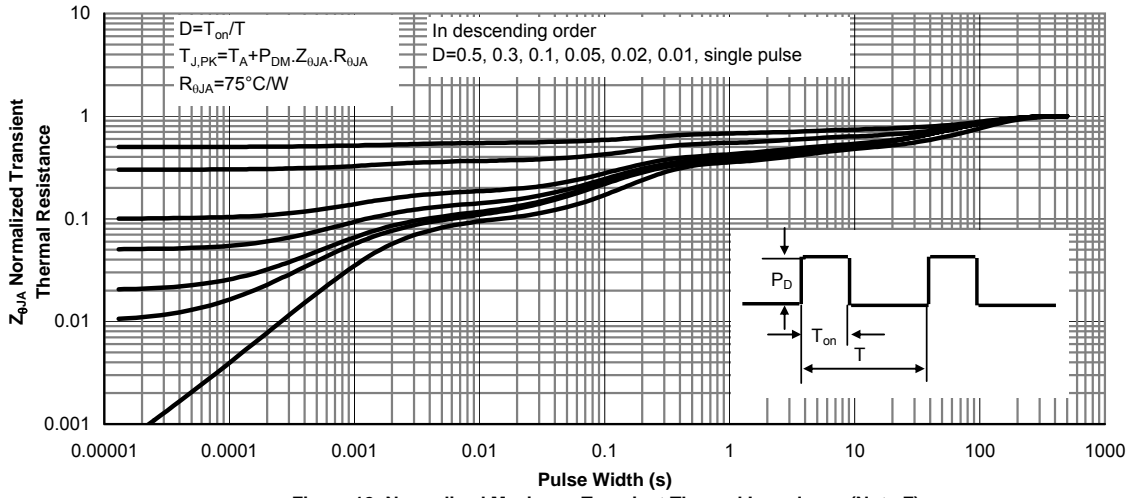
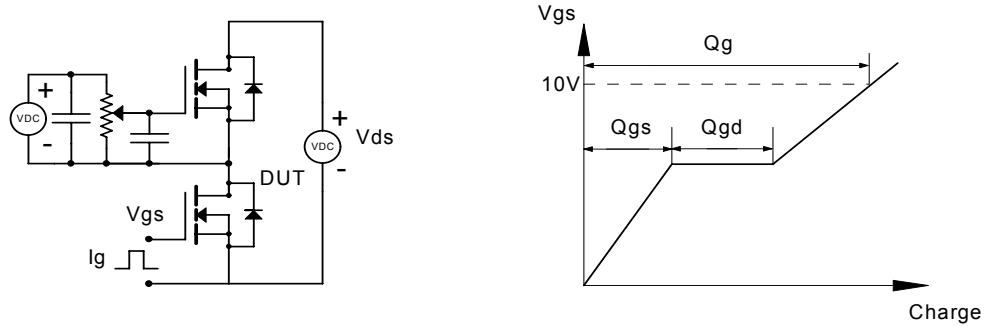


Figure 11: Single Pulse Power Rating Junction-to-Ambient (Note F)

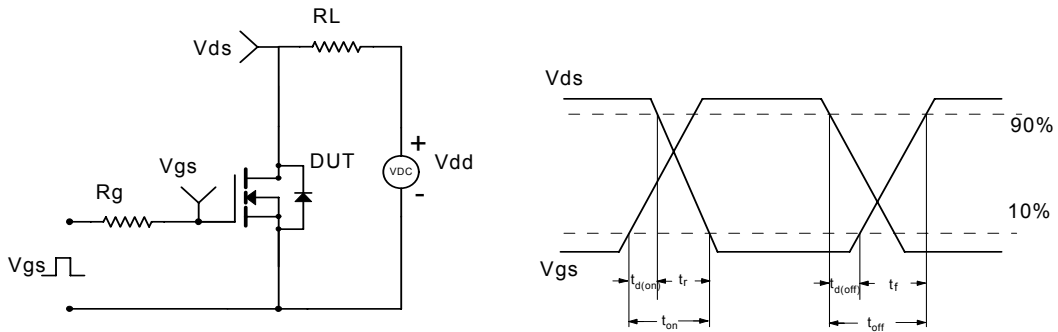
TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS



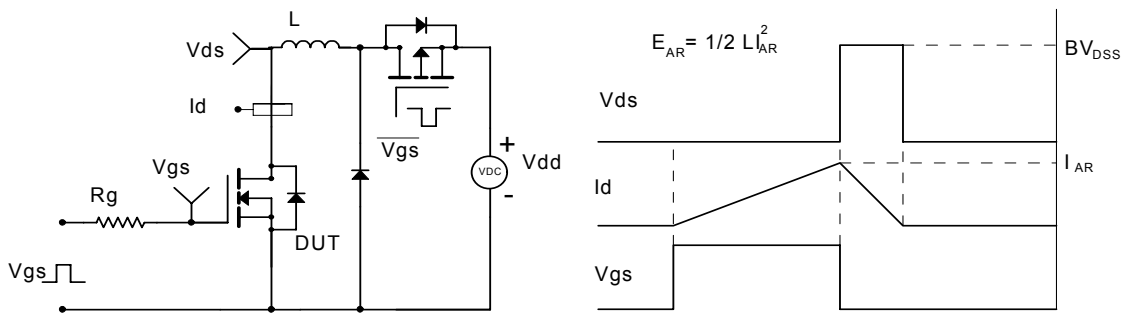
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

