

# HD74HC194

## 4-bit Bidirectional Universal Shift Register

REJ03D0589-0200  
(Previous ADE-205-466)  
Rev.2.00  
Jan 31, 2006

### Description

This bidirectional shift register is designed to incorporate virtually all of the features a system designer may want in a shift register. It features parallel inputs, parallel outputs, right shift and left shift serial inputs, operating mode control inputs, and a direct overriding clear line. The register has four distinct modes of operation: parallel (broadside) load, shift right (in the direction  $Q_A$  toward  $Q_D$ ); shift left; inhibit clock (do nothing).

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs,  $S_0$  and  $S_1$ , high. The data are loaded into their respective flip-flops and appear at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited. Shift right is accomplished synchronously with the rising edge of the clock pulse when  $S_0$  is high and  $S_1$  is low. Serial data for this mode is entered at the shift right data input. When  $S_0$  is low and  $S_1$  is high, data shifts left synchronously and new data is entered at the shift left serial input. Clocking of the flip-flops is inhibited when both mode control inputs are low. The mode control inputs should be changed only when the clock input is high.

### Features

- High Speed Operation:  $t_{pd}$  (Clock to Q) = 12 ns typ ( $C_L = 50$  pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage:  $V_{CC} = 2$  to 6 V
- Low Input Current: 1  $\mu$ A max
- Low Quiescent Supply Current:  $I_{CC}$  (static) = 4  $\mu$ A max
- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74HC194P	DILP-16 pin	PRDP0016AE-B (DP-16FV)	P	—

### Function Table

Operating Mode	Inputs										Outputs			
	Clear	Mode		Clock	Serial		Parallel							
		S <sub>1</sub>	S <sub>0</sub>		Shift Left	Shift Right	A	B	C	D	Q <sub>A</sub>	Q <sub>B</sub>	Q <sub>C</sub>	Q <sub>D</sub>
Clear	L	X	X	X	X	X	X	X	X	X	L	L	L	L
Parallel load	H	H	H		X	X	a	b	c	d	a	b	c	d
Shift right	H	L	H		X	H	X	X	X	X	H	Q <sub>An</sub>	Q <sub>Bn</sub>	Q <sub>Cn</sub>
	H	L	H		X	L	X	X	X	X	L	Q <sub>An</sub>	Q <sub>Bn</sub>	Q <sub>Cn</sub>
Shift left	H	H	L		H	X	X	X	X	X	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q <sub>Dn</sub>	H
	H	H	L		L	X	X	X	X	X	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q <sub>Dn</sub>	L
Hold	H	L	L	X	X	X	X	X	X	X	Q <sub>A0</sub>	Q <sub>B0</sub>	Q <sub>C0</sub>	Q <sub>D0</sub>
	H	X	X	L	X	X	X	X	X	X	Q <sub>A0</sub>	Q <sub>B0</sub>	Q <sub>C0</sub>	Q <sub>D0</sub>
	H	X	X	H	X	X	X	X	X	X	Q <sub>A0</sub>	Q <sub>B0</sub>	Q <sub>C0</sub>	Q <sub>D0</sub>

H : high level (Steady state)

L : low level (Steady state)

X : don't care

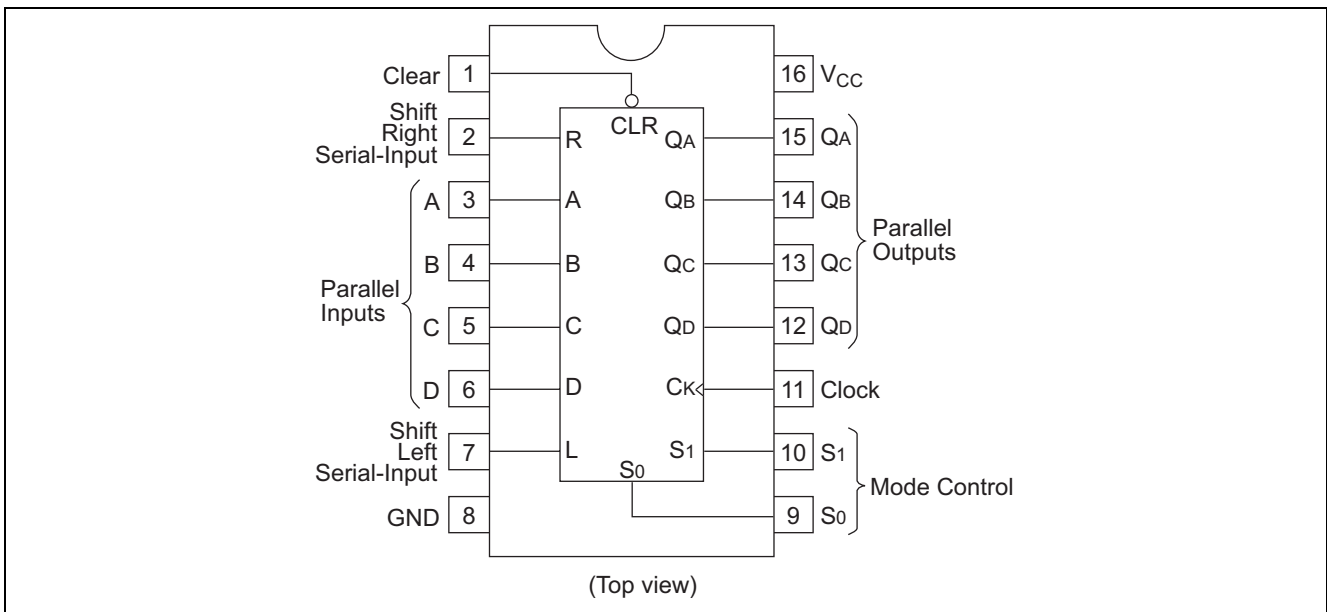
: transition from low to high level.

a, b, c, d : the level of steady-state input at inputs A, B, C or D respectively.

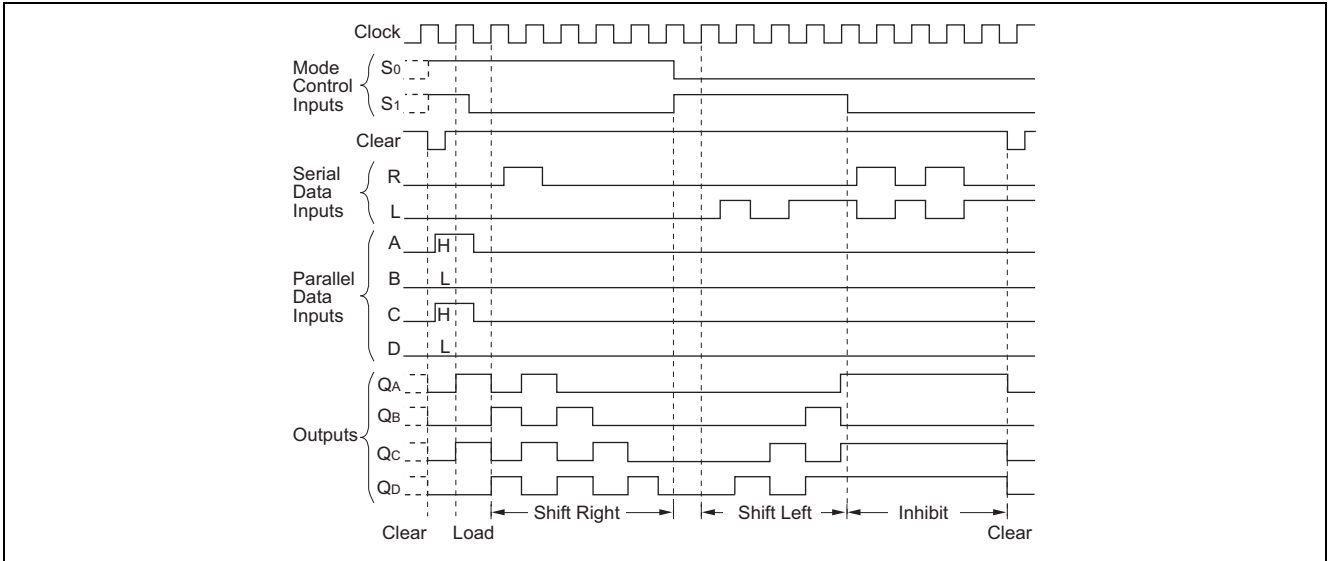
Q<sub>A0</sub>, Q<sub>B0</sub>, Q<sub>C0</sub>, Q<sub>D0</sub> : the level of Q<sub>A</sub>, Q<sub>B</sub>, Q<sub>C</sub> or Q<sub>D</sub> respectively, before the indicated steady-state input conditions were established.

Q<sub>An</sub>, Q<sub>Bn</sub>, Q<sub>Cn</sub>, Q<sub>Dn</sub> : the level of Q<sub>A</sub>, Q<sub>B</sub>, Q<sub>C</sub> or Q<sub>D</sub> respectively before the most recent transition of the clock.

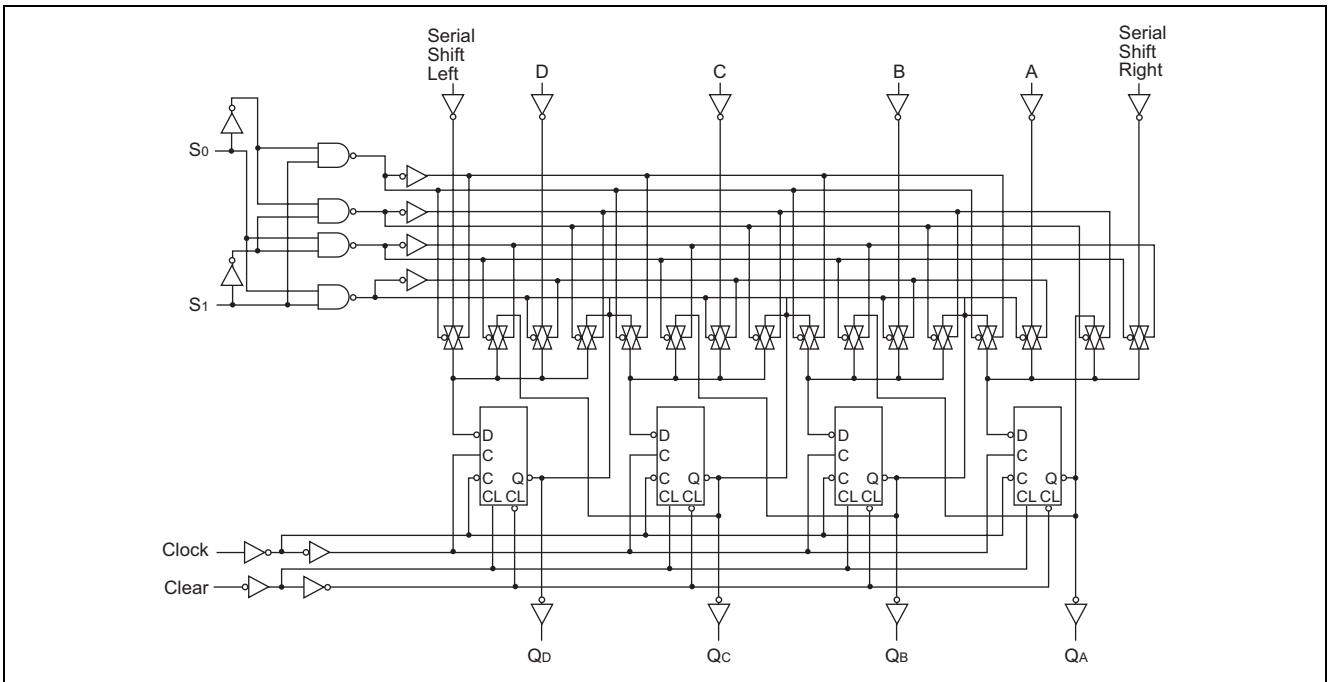
### Pin Arrangement



### Timing Diagram



### Logic Diagram



### Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage range	V <sub>CC</sub>	-0.5 to 7.0	V
Input / Output voltage	V <sub>IN</sub> , V <sub>OUT</sub>	-0.5 to V <sub>CC</sub> +0.5	V
Input / Output diode current	I <sub>IK</sub> , I <sub>OK</sub>	±20	mA
Output current	I <sub>O</sub>	±25	mA
V <sub>CC</sub> , GND current	I <sub>CC</sub> or I <sub>GND</sub>	±50	mA
Power dissipation	P <sub>T</sub>	500	mW
Storage temperature	T <sub>stg</sub>	-65 to +150	°C

Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

### Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	$V_{CC}$	2 to 6	V	
Input / Output voltage	$V_{IN}, V_{OUT}$	0 to $V_{CC}$	V	
Operating temperature	$T_a$	-40 to 85	°C	
Input rise / fall time <sup>*1</sup>	$t_r, t_f$	0 to 1000	ns	$V_{CC} = 2.0\text{ V}$
		0 to 500		$V_{CC} = 4.5\text{ V}$
		0 to 400		$V_{CC} = 6.0\text{ V}$

Notes: 1. This item guarantees maximum limit when one input switches.  
 Waveform: Refer to test circuit of switching characteristics.

### Electrical Characteristics

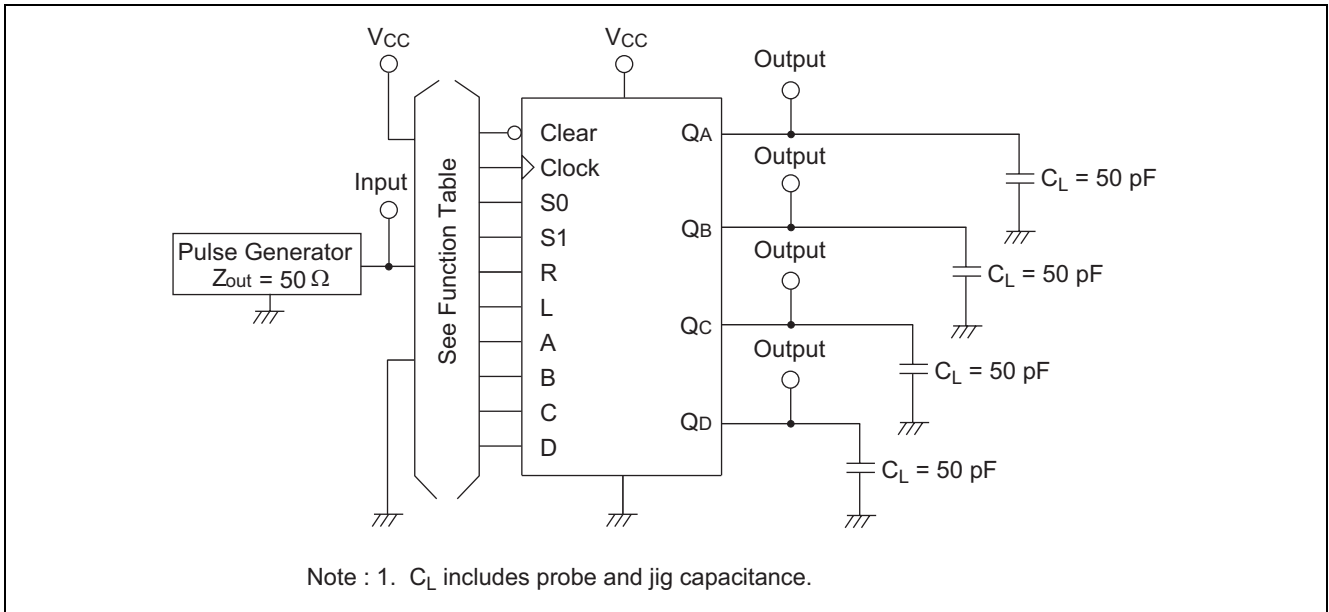
Item	Symbol	$V_{CC}$ (V)	$T_a = 25^\circ\text{C}$			$T_a = -40\text{ to }+85^\circ\text{C}$		Unit	Test Conditions	
			Min	Typ	Max	Min	Max			
Input voltage	$V_{IH}$	2.0	1.5	—	—	1.5	—	V		
		4.5	3.15	—	—	3.15	—			
		6.0	4.2	—	—	4.2	—			
	$V_{IL}$	2.0	—	—	0.5	—	0.5	V		
		4.5	—	—	1.35	—	1.35			
		6.0	—	—	1.8	—	1.8			
Output voltage	$V_{OH}$	2.0	1.9	2.0	—	1.9	—	V	$V_{in} = V_{IH}\text{ or }V_{IL}$	$I_{OH} = -20\ \mu\text{A}$
		4.5	4.4	4.5	—	4.4	—			$I_{OH} = -4\ \text{mA}$
		6.0	5.9	6.0	—	5.9	—			$I_{OH} = -5.2\ \text{mA}$
		4.5	4.18	—	—	4.13	—			
		6.0	5.68	—	—	5.63	—			
	$V_{OL}$	2.0	—	0.0	0.1	—	0.1	V	$V_{in} = V_{IH}\text{ or }V_{IL}$	$I_{OL} = 20\ \mu\text{A}$
		4.5	—	0.0	0.1	—	0.1			
		6.0	—	0.0	0.1	—	0.1			
		4.5	—	—	0.26	—	0.33			$I_{OL} = 4\ \text{mA}$
		6.0	—	—	0.26	—	0.33			$I_{OL} = 5.2\ \text{mA}$
Input current	$I_{in}$	6.0	—	—	$\pm 0.1$	—	$\pm 1.0$	$\mu\text{A}$	$V_{in} = V_{CC}\text{ or GND}$	
Quiescent supply current	$I_{CC}$	6.0	—	—	4.0	—	40	$\mu\text{A}$	$V_{in} = V_{CC}\text{ or GND}, I_{out} = 0\ \mu\text{A}$	

## Switching Characteristics

(C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

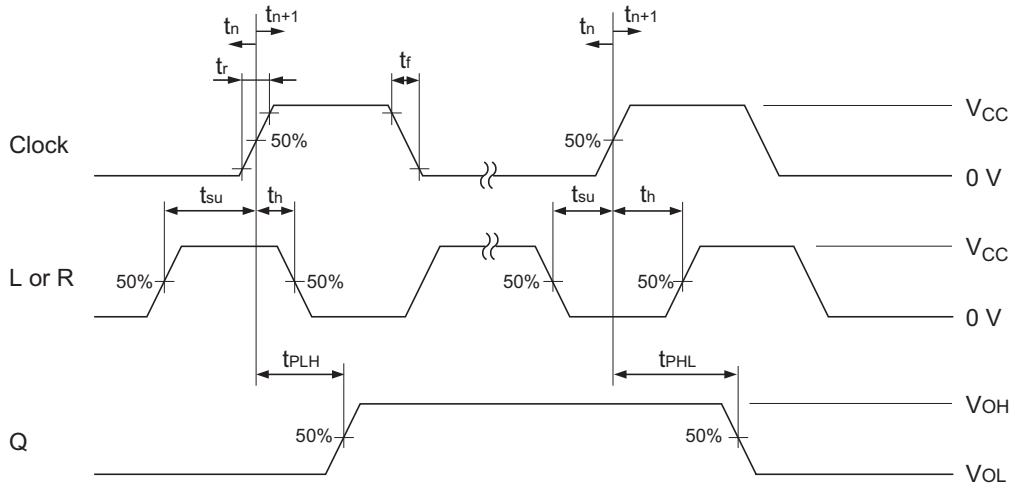
Item	Symbol	V <sub>CC</sub> (V)	Ta = 25°C			Ta = -40 to +85°C		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Maximum clock frequency	f <sub>max</sub>	2.0	—	—	6	—	5	ns	
		4.5	—	—	30	—	24		
		6.0	—	—	35	—	28		
Propagation delay time	t <sub>PHL</sub>	2.0	—	—	140	—	175	ns	Clock to Q
		4.5	—	12	28	—	35		
		6.0	—	—	24	—	30		
	t <sub>PLH</sub>	2.0	—	—	140	—	175	ns	
		4.5	—	12	28	—	35		
		6.0	—	—	24	—	30		
	t <sub>PHL</sub>	2.0	—	—	150	—	190	ns	Clear to Q
		4.5	—	13	30	—	38		
		6.0	—	—	26	—	33		
Pulse width	t <sub>w</sub>	2.0	80	—	—	100	—	ns	Clock or Clear
		4.5	16	6	—	20	—		
		6.0	14	—	—	17	—		
Setup time	t <sub>su</sub>	2.0	100	—	—	125	—	ns	A, B, C or D to Clock
		4.5	20	7	—	25	—		
		6.0	17	—	—	21	—		
	t <sub>su</sub>	2.0	150	—	—	187	—	ns	Mode controls to Clock
		4.5	30	17	—	37	—		
		6.0	25	—	—	31	—		
Hold time	t <sub>h</sub>	2.0	0	—	—	0	—	ns	Any input
		4.5	0	-4	—	0	—		
		6.0	0	—	—	0	—		
Removal time	t <sub>rem</sub>	2.0	25	—	—	31	—	ns	Clear inactive to Clock
		4.5	5	1	—	6	—		
		6.0	4	—	—	5	—		
Output rise/fall time	t <sub>TLH</sub>	2.0	—	—	75	—	95	ns	
	t <sub>THL</sub>	4.5	—	5	15	—	19		
	t <sub>THL</sub>	6.0	—	—	13	—	16		
Input capacitance	C <sub>in</sub>	—	—	5	10	—	10	pF	

Test Circuit



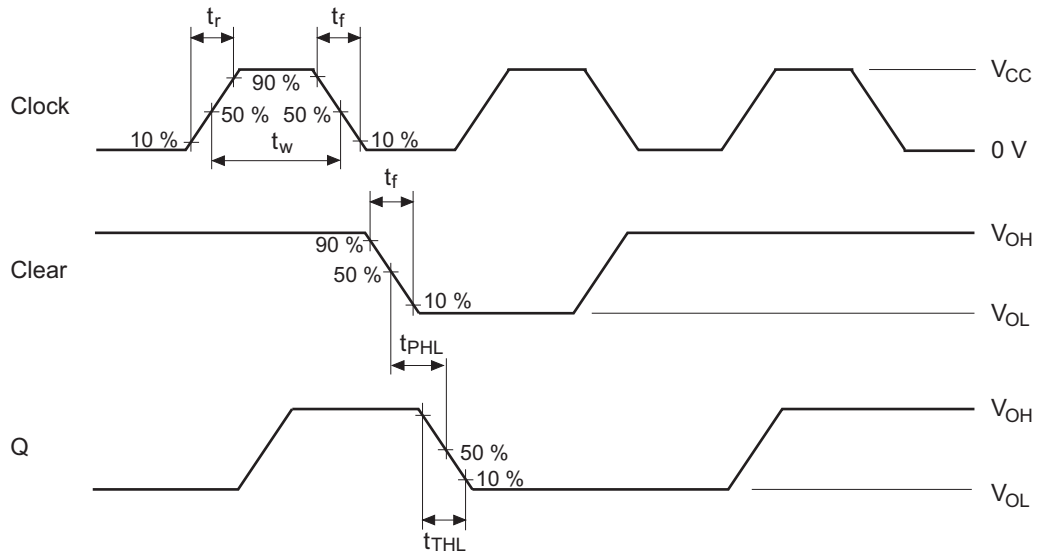
Waveforms

• Waveform – 1



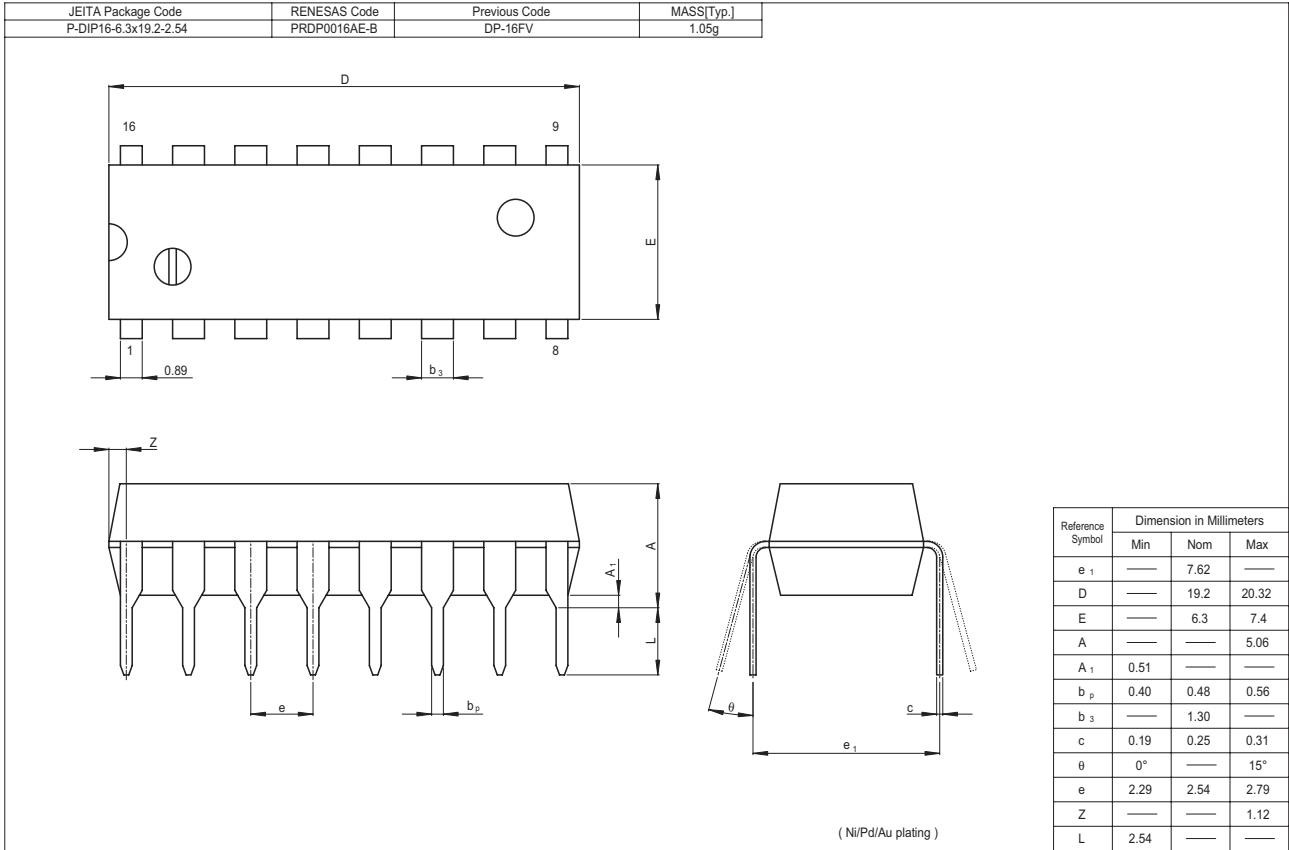
- Notes : 1. For right shift, measure QA at  $t_{n+1}$ , QB at  $t_{n+2}$ , QC at  $t_{n+3}$ , QD at  $t_{n+4}$ , respectively.  
 For left shift, measure QA at  $t_{n+4}$ , QB at  $t_{n+3}$ , QC at  $t_{n+2}$ , QD at  $t_{n+1}$ , respectively.  
 2. Input pulse :  $PRR \leq 1 \text{ MHz}$ ,  $Z_o = 50 \Omega$ ,  $t_r \leq 6 \text{ ns}$ ,  $t_f \leq 6 \text{ ns}$

• Waveform – 2



- Note : 1. Input pulse :  $PRR \leq 1 \text{ MHz}$ ,  $Z_o = 50 \Omega$ ,  $t_r \leq 6 \text{ ns}$ ,  $t_f \leq 6 \text{ ns}$

Package Dimensions





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